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Effects of the Lower Body Diode on the Ringing Characteristics of a Power Inverter

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Abstract

In a power inverter with both pull-up and pull-down transistors, the ringing that occurs on the highto-low and low-to-high transitions of the output voltage will be dependent on not only the equivalent circuit parameters of the transistors in the ringing current path, but also on whether or not the lower body diode (LBD) is conducting on the subsequent pulse. If the LBD is still conducting, the resultant ringing on the low-to-high transition will be stronger than if the LBD has stopped conducting, and its associated pole location will change.

Knowing the status of the LBD is critical to being able to track changes in device parameters due to aging or damage. If the LBD is conducting, then only the high-to-low transition can be used to track changes in device parameters; however, if the LBD is not conducting, either transition may be used.

1. Introduction

When an inverter circuit has both pull-up and pull-down transistors, some ringing will occur on both the high-to-low and low-to-high transitions of the output. This ringing is due to the resistance, capacitance, and inductance of a current loop on the output side of the inverter pair [1]. In the test bed circuit shown in Fig. 1, the high-side transistor is driven with a PWM signal. The period and duty cycle of the PWM are varied to examine the behavior of ringing under different operating conditions. Note that in this test circuit, the gate of Q2 is permanently tied low, causing Q2 to remain off at all times. The ringing current might follow the path shown in blue in Fig. 1.



Fig. 1. Example ringing current path for an inverter pair of MOSFETs.

This ringing characteristic is dependent upon the manner of operation. For example, in Fig. 1 when Q1 is on and Q2 is off, the output is in a high state; turning off Q1 results in a high-to-low transition. A transistor that is off is modeled differently from one that is on. For a transistor that has been switched on, the transistor can be approximately modeled as the resistance R_{ds} . For a transistor that is off, its equivalent model is the series combination of its output capacitance, C_{oss} , and resistance, R_{oss} . The LBD may be modeled as a current-dependent resistance. When the LBD isn't conducting, its equivalent resistance is very high. When LBD is conducting, its equivalent resistance is relatively low and is a function of the amount of current.

When the circuit of Fig. 1 is constructed, the loop shown in blue has an associated area on a circuit board resulting in a loop inductance. This loop inductance acts in conjunction with the transistor

resistance and capacitance to create ringing on V_o . If the LBD is still switched on during the low-tohigh transition, the resistance and capacitance of the lower transistor is in parallel with the LBD impedance. Full equivalent circuits for both low-to-high and high-to-low transition ringing are provided in Figs. 2 and 3.

2. Effect of the Lower Body Diode on Ringing

After a high-to-low transition of the output, the body diode of the lower transistor will be turned on for a period of time. The load inductance keeps the current flowing, but it can no longer be pulled through the high-side transistor so it is pulled up through the LBD and out through the load. The length of time the LBD continues to conduct is an important factor influencing the ringing characteristics. Fig. 2 shows the equivalent circuit of the ringing current loop for low-to-high transitions, while Fig. 3 shows the equivalent circuit for high-to-low transitions.

Note that the equivalent model for a transistor depends on whether or not the transistor is on. Also, note that, when the output voltage dips below the LBD turn-on voltage, the equivalent impedance of the lower transistor changes dramatically.



Fig. 2. Equivalent circuit for low-to-high transitions of V_{o.}

High-to-Low Transition of V_o High-Side FET (Off) $C_{oss,H}$ at $V_{DS,H} \approx 5 \text{ V}$ $R_{oss,H} \approx 5 \text{ V}$ $R_{oss,L} \approx 0 \text{ V}$ $C_{oss,L}$ at $V_{DS,L} \approx 0 \text{ V}$ LBDLow-Side FET (Off)

Fig. 3. Equivalent circuit for high-to-low transitions of V_{o.}

The LBD turns on immediately following a high-to-low transition. If the LBD continues to conduct when the subsequent low-to-high transition occurs, the resultant ringing will be much stronger than if the LBD had stopped conducting. This is largely due to the increased current that flows through the high-side transistor if it turns on while the LBD is still conducting. When the LBD is conducting, it can be modeled as a low, current-dependent resistance.

The pulse width of the PWM signal and the load impedance determine the maximum current that flows in the load. The time constant of the load determines how quickly the load current decays once the excitation of the PWM has been removed. If the duty cycle of the PWM is long enough that the LBD is still conducting when the next low-to-high transition occurs, then the resulting ringing will be stronger.

In the two plots in Fig. 4, various periods and duty cycles are shown. Here, both modes of ringing can be seen. In these plots, when the duty cycle is 5% or lower, the LBD has stopped conducting before the low-to-high transition occurs. At a 25% duty cycle, the LDB is still conducting when the low-to-high transition occurs. When the period is 25 μ sec (plot on the left), the low-to-high transition occurs while the LBD is still conducting. When the period is 200 μ sec (plot on the right), the low-to-high transition occurs after the LBD has turned off. Note that the ringing is much stronger and decays more rapidly when the LBD is still conducting during the low-to-high transition.



Fig. 4. Equivalent circuit for high-to-low transitions of V_o.

As expected, ringing on the low-to-high transitions and on the high-to-low transitions isn't affected equally by the status of the LBD. Low-to-high ringing changes depending on whether or not LBD is conducting. The LBD is always on following a high-to-low transition. The loop impedance is dominated by the high-side transistor capacitance, so the ringing is relatively consistent.

3. Time-Dependency of Ringing

Yet another factor to complicate ringing analysis is the fact that if the LBD is conducting, the frequency and damping of the ringing can change with time. This is due to the fact that the current through the LBD is changing with time, causing the equivalent resistance of the LBD to change as well. This changing resistance, which is in parallel with the resistance and capacitance of the low-side transistor, causes both the frequency and the damping of the ringing to change until the LBD has fully turned off.

For an average case of the time dependency of the ringing period, Fig. 5 shows how the period changes between the first few peaks until it gradually reaches a steady-state value. If these first few peaks are included in the ringing analysis, they can result in pole locations that might be falsely believed to represent device degradation.



Fig. 5. Time dependency of ringing period.

As the output voltage changes and causes the LBD to become reverse biased, the LBD begins to switch off. As the LBD switches off, there will be nonlinearity present in the ringing current loop. Until the LBD completely switches off, the frequency and damping of the ringing will continue to change. They will finally reach a steady state value when the LBD is fully off and the system has become linear. This phenomenon creates a problem with identifying the true pole position, and it increases the variance and spread of the pole plot.

4. Windowing to Account for Time-Dependence and Nonlinearity

Windowing is a procedure used to cut down a set of data to a manageable size in order for the data to be analyzed with the Matrix Pencil Method. It is also used to eliminate any nonlinear effects due to changes in device parameters during the first part of a ringing waveform. Windowing removes all data except for the ringing, and for this study, a windowed set of data usually consists of around 7000 data points. This number is a good compromise between speed and accuracy. Figs. 6 and 7 demonstrate the effects of shifting the window on pole location. Fig. 6 shows windows that start at both 5-samples after the peak and 30-samples after the peak.



Fig. 6. Example windowing start times.

Fig. 7 shows the effect of the window on the calculated pole locations. The high-to-low poles experienced virtually no change in location, while the low-to-high poles were widely scattered. The 30-sample peak offset significantly reduced the amount of scattering compared to the 5-sample offset.

For low-to-high transitions when the LBD is still conducting, the non-linear behavior makes it difficult to calculate a stable pole location. For this reason, the remainder of this study will focus on observing pole locations for low-to-high transitions only when the LBD has turned off prior to the transition.



Fig. 7. Resultant poles from different windowing start times.

5. Monitoring Changes in Transistor Parameters

Figs. 2 and 3 illustrate the different parameters that have an affect on the ringing after high-to-low and low-to-high transitions. Changes in these parameters can be tracked by monitoring the shift of the poles. As indicated by the plots in Fig. 8, pole locations are relatively stable and repeatable for low-to-high transitions when the LBD is not conducting. They are also relatively stable and repeatable for high-to-low transitions. Low-to-high ringing can be used to track changes in the low-side transistor parameters. High-to-low ringing can be used to track changes in the high-side transistor parameters.

The errant poles seen as red dots in the upper right plot of Fig. 8 are the result of the shorter pulse width and period of the waveform that produced these poles. The shorter pulse width and period caused the load current to decrease, and the ringing that these poles were extracted from was much weaker than the ringing that produced all other poles. This weaker ringing died out more quickly, dropping into the noise floor and increasing the numerical error in the calculation of the pole location.

6. Conclusion

In order to accurately describe the ringing of an inverter pair of transistors, you must know not only what transition you are looking at, but also whether the lower body diode is still conducting on the subsequent low-to-high transition of the output voltage. The LBD can cause a shift in the pole location if not properly accounted for.



Fig. 8. Resultant poles for different transitions and LBD statuses.

Ideally, measurements should be taken while the LBD is not conducting in order to get the most usable data from a particular measurement. If the LBD conducts during the subsequent pulse under nominal operating conditions, then the best solution might be to either switch to a known load or to adjust the duty cycle for a few pulses while measurements are taken. By ensuring that the LBD is off, the parameters that contribute to the ringing are well known and relatively stable.

Once the status of the LBD is known and any nonlinearity is accounted for, changes in circuit parameters (e.g. due to aging or imminent failures) can be tracked by looking for shifts in the pole locations.

References

[1] J. H. Hayes and T. Hubing, "Preliminary Investigation of the Current Path and Circuit Parameters Associated with the Characteristic Ringing in a MOSFET Power Inverter," *Clemson Vehicular Electronics Laboratory Technical Report: CVEL-13-041*, Jan. 16, 2013.