# ECE 429 / 629 Homework #5

1. Suppose we have a classic RISC five-stage integer pipeline. Assume all memory access take 1 clock cycle, and that a register read/write in the same clock cycle "forwards" through the register file. Show the timing diagram (using F,D,X,M,W) and compute the total number of cycles to execute the program below:

```
Loop:     LW   R1, 0(R2)
          ADDI R1, R1, 1
          SW   0(R2), R1
          ADDI R2, R2, 4
          SUB  R4, R3, R2
          BNEZ R4, Loop
```

   a. without any forwarding or bypassing hardware; branches are handled by flushing the pipeline
   b. with normal forwarding and bypassing hardware; branches are handled by predicting as not taken
   c. with normal forwarding and bypassing hardware with single-cycle delayed branch. Schedule the instructions to reduce the branch delay. You may reorder the instructions and modify the individual operands, but do not change the number of instructions or their opcodes.
2. Problem A.3 in the text
3. Problem A.4 in the text

Text: Hennessy and Patterson, *Computer Architecture: A Quantitative Approach*, 3rd edition, Morgan Kaufmann, 2003. (#1 adapted from A.1 in the text.)