PRINTED CIRCUIT BOARD POWER BUS DECOUPLING USING EMBEDDED CAPACITANCE

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Abstract - The purpose of decoupling capacitors on printed circuit boards is to meet the instantaneous current demands of high-speed active devices while minimizing power bus noise. Embedded capacitance is an alternative to discrete decoupling capacitors and is achieved by taking advantage of the natural capacitance between the power and ground planes. This paper investigates the electrical properties of boards manufactured with four different kinds of embedded capacitance. These boards have power-ground plane pairs separated by very thin materials with high dielectric constants. It is shown that some kinds of embedded capacitance work significantly better than standard decoupling schemes using discrete decoupling capacitors.

I. INTRODUCTION

Printed circuit board designs typically employ a number of decoupling capacitors connected to power and ground near the active devices. The purpose of these capacitors is to supply current in response to a sudden change in voltage and thereby help to stabilize the power bus voltage. Typical high-speed digital designs will have dozens or even hundreds of discrete decoupling capacitors. These capacitors take up space on the board and can reduce the reliability of the product in which they are used.

Embedded capacitance is an alternative to using discrete decoupling capacitors. Embedded capacitance takes advantage of the natural capacitance between the power and ground planes of a printed circuit board in order to stabilize the power bus voltage. By minimizing the spacing between planes and filling this space with materials that have a high dielectric constant, capacitances on the order of nanofarads per square centimeter can be achieved.

Electrical models available at the beginning of the project suggested that embedded capacitance materials would be capable of reducing power bus noise at frequencies well above the useful range of surface mounted capacitors. In fact, surface-mounted decoupling capacitors are known to be ineffective above a few hundred megahertz on boards with closely spaced power and ground planes [1]. However, there were concerns that the high-dielectric-constant materials used in boards with embedded capacitance might be ineffective at high frequencies or introduce new problems due to power bus resonances.

The results of the tests performed during the course of this project were very encouraging. All of the embedded capacitance materials did a good job of reducing power bus noise over the entire frequency range evaluated (up to 5 GHz). The materials with the thinnest dielectric layers were the most effective. For a given thickness, the materials with the highest dielectric constant worked best. One surprising observation was that all of the embedded capacitance materials tested dampened the resonances in the power bus significantly. The two thinnest materials effectively eliminated all power bus resonances.

This paper examines the electrical performance of embedded capacitance boards manufactured by four different companies. The work was sponsored by the National Center for Manufacturing Sciences (NCMS) Embedded Decoupling Capacitance (EDC) Project. NCMS is headquartered in Ann Arbor Michigan, USA. Several companies including board manufacturers and material suppliers participated in this project. Participants included:

- StorageTek
- Delphi Delco Electronics Systems
- Raytheon Systems
- 3M
- E.I. DuPont de Nemours Co., Inc.
- Litton Interconnect Technologies
- HADCO
- Merix Corporation
- University of Missouri-Rolla
- Penn State University
- National Institute of Standards and Technology
- Tobyhanna Army Depot

The materials tested are described in Table I. Additional information on these materials, including the results of mechanical and reliability tests of boards made with these materials, can be obtained from NCMS [2].

Table I - Materials Evaluated for this Study

Material	Supplier	Dielectric Composition	Dielectric Thickness
EC#1 BC2000™	HADCO (supplied by Polyclad)	FR-4 epoxy/glass	~ 50 μm 2.0 mils
EC#2 EmCap™	HADCO	Unsupported epoxy; ceramic powder filled	~ 100 μm 4.0 mils
EC#3 Kapton® HiK	DuPont	Unsupported polyamide; ceramic powder filled	~ 40 μm 1.6 mils
EC#4 C-Ply	3M	Unsupported epoxy; ceramic powder filled	~ 6 μm 0.25 mils

II. THE TEST VEHICLE

Fig. 1 shows a diagram of the board used to do the electrical testing. The board is 7.6 cm x 5.1 cm and contains eight CMOS clock drivers. A 50-MHz oscillator supplies a signal to the first clock driver. This device supplies 50-MHz clock signals to each of six other clock drivers. The outputs of these six clock drivers are terminated in capacitive loads. A seventh clock driver on the board was used for power current measurements and was not active for the tests described in this paper. On the boards designated as having discrete decoupling, there are 33 local 0.1-μF decoupling capacitors and one 22-μF bulk decoupling capacitor.

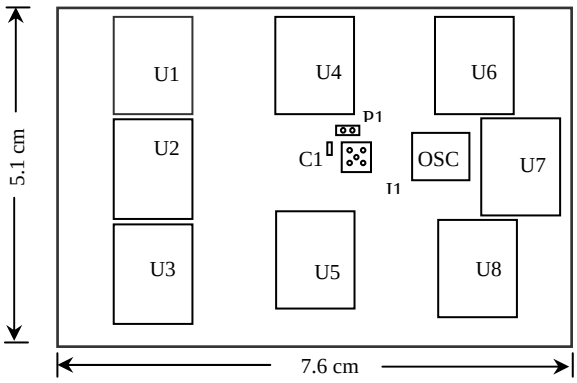

Fig. 1 - Layout of test boards.

All test boards discussed in this paper were 6-layer boards. Two of the inner layers were solid power and ground planes. An SMA coaxial connector (J1) and a 2-pin connector (P1) provided electrical access to the power bus structure. The center conductor of the SMA connector was connected to the power plane while the outer shield was connected to the ground plane through 4 vias. The 2-pin connector had one pin connected to the power plane and the other pin connected to the ground plane. Both of these connectors were mounted on the bottom of the board (Layer 6), while the rest of the components were mounted on the top of the board (Layer 1).

III. MEASUREMENT RESULTS

III.1 Input Impedance Measurements

Test boards with different embedded capacitance materials were evaluated using swept frequency measurements of the power bus input impedance. Input impedance is perhaps the best indicator of how "good" or "bad" a power bus is in terms of minimizing power bus noise voltage. Actual power bus noise measurements with active components as the source are highly dependent on the exact frequency and location of the source. Swept frequency measurements are more likely to capture any resonant peaks in the board's response. Since components look like relatively high-impedance sources, the noise voltage at any point on the board due to a component drawing current at that point is directly proportional to the board impedance at that point.

The power bus input impedance of these boards was measured using an HP8753D network analyzer. The SMA connector on the test board was connected to Port 1 of the network analyzer through a low-loss precision cable. A one-port calibration was performed to set the measurement plane to the end of the coaxial cable. Then a port extension was performed with a shorted SMA connector to extend the measurement plane to the plane of the board. S11 was measured and converted to input impedance. The measurements were performed between 30 kHz and 5 GHz.

Fig. 2 shows a plot of the magnitude of the measured power bus impedance at the location of the J1 connector for a standard FR-4 version of this board with no components mounted. For this board, the ground and power planes were located on layers 2 and 5 respectively. Signal traces were routed on layer 3. The spacing between the power and ground planes was approximately 500 μm. Note that below 300 MHz, the impedance resembles that of an ideal capacitor. The peak at 833 MHz represents the first resonant frequency of the power bus (TM10 mode). The peaks at 1.67 GHz (TM20 mode) and higher frequencies represent higher-order power bus resonances. These peaks in the power bus impedance are the frequencies at which noise on the power bus is likely to be highest.

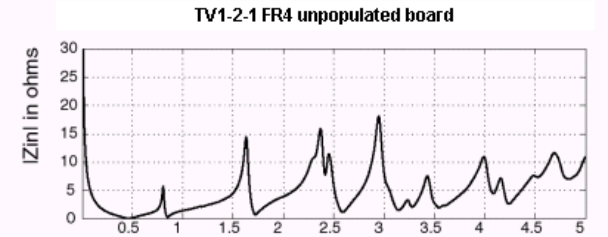

Fig. 2 - Measured power bus impedance of an unpopulated 500-µm FR-4 board.

Fig. 3 shows a plot of the measured power bus impedance for the same board with all of the components mounted except the 33 local decoupling capacitors. The spike below 200 MHz is due to the resonance between the inductance of the bulk decoupling capacitor and the interplane capacitance. Power bus resonances still dominate the impedance above 500 MHz although they are slightly damped and shifted relative to the unpopulated board.

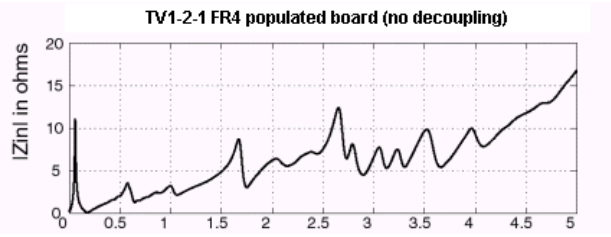

Fig. 3 - Measured power bus impedance of a populated 500-µm FR-4 board.

Fig. 4 shows that adding the 33 local decoupling capacitors reduces the impedance at low frequencies. However these capacitors have relatively little effect on the power bus impedance above 1 GHz.

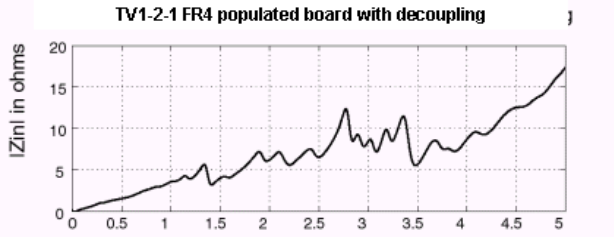

Fig. 4 - Measured power bus impedance of a 500-µm FR-4 board with decoupling.

Fig. 5 shows the measured impedance of a similar board with the BC2000 embedded capacitance. This board contains all the components except the 33 local decoupling capacitors. The ground and power planes in this board were located approximately 50 µm apart on layers 3 and 4 respectively. Signal traces were routed on layer 2. Note that the parallel resonance between the bulk decoupling capacitor and the interplane capacitance is still apparent, but the power bus resonances are significantly damped.

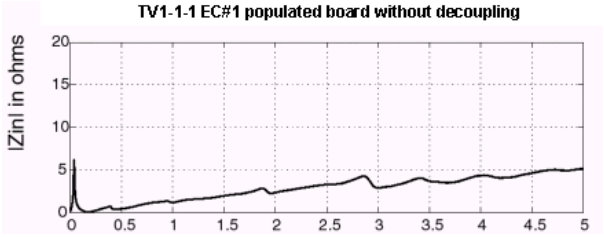

Fig. 5 - Measured power bus impedance of a 50-µm BC2000 board.

Fig. 6 shows the measured impedance of another board with embedded capacitance. This board employs the EmCap material, which has a relatively wide power-ground plane spacing (~100 µm), but it uses a dielectric with a relative permittivity approximately 8 times greater than standard FR-4 material.

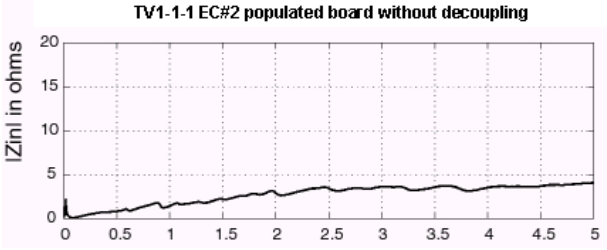

Fig. 6 - Measured power bus impedance of a 100-µm EmCap board.

Fig. 7 shows the measured impedance of a C-Ply board that combines a very thin plane spacing (~6 µm) with a high-dielectric constant material. Note that all resonances (including the parallel resonance with the bulk decoupling capacitor) are significantly damped. The power bus impedance is very low at all frequencies from 0.1 – 5.0 GHz. The slope in this curve is primarily due to the small amount of inductance associated with the probe's connection to the power bus (~150 pH).

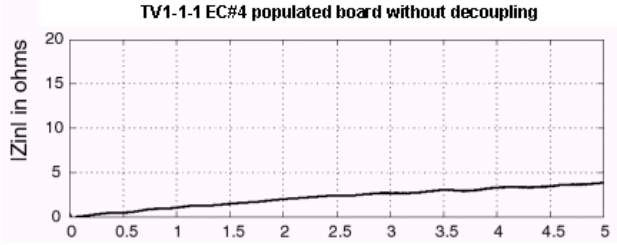

Fig. 7 - Measured power bus impedance of a ~6-µm C-Ply board.

The lack of significant power bus resonances in the embedded capacitance boards was initially a surprise. However, this observation is easily explained. Cavity resonances are dampened by electrical loss in the system. In this case there are four easily identifiable sources of loss: dielectric loss, copper loss, radiation loss and resistive loss in the attached components.

Formulas for copper loss are well documented [3,4]. For very thin dielectric layers, an approximate formula for the quality factor due to conductive losses in the top and bottom planes is given by,

$$Q_c \approx h/\delta \,. \qquad (1)$$

where h is the thickness of the dielectric and δ is the skin depth in the planes. A low Q-factor implies that a resonance is well damped. Equation (1) indicates that when the thickness of the dielectric is on the order of a skin depth in the copper planes, the copper loss alone is sufficient to completely damp any power bus resonances.

III.2 Power Bus Noise Measurements

With the boards operational, a Rohde & Schwarz FSEB30 spectrum analyzer was used to measure the power bus noise in three frequency bands. A 1-meter long SMA precision coaxial cable was used to connect the input port to the SMA jack on the populated test boards. The total power bus noise in the 0-1GHz band is plotted in Fig. 8 for each of the boards measured. The highest bar represents the FR-4 board without decoupling capacitors. The two lower black bars (labeled FR4w/d) are the FR-4 boards with the 33 local decoupling capacitors added. In this frequency band, the decoupling capacitors are more effective at reducing the power bus noise than 3 of the 4 embedded capacitance materials.

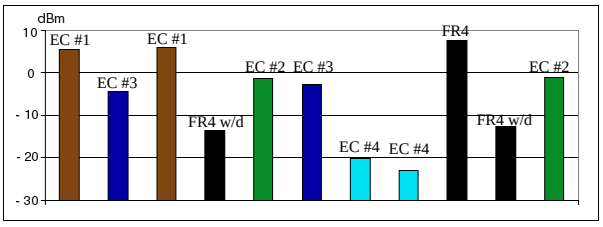

Fig. 8 - Measured power bus noise (1 MHz - 1 GHz).

Fig. 9 shows the measured power bus noise in the 1-3 GHz frequency band. In this frequency band, all of the embedded capacitance schemes are more effective than the discrete decoupling capacitors.

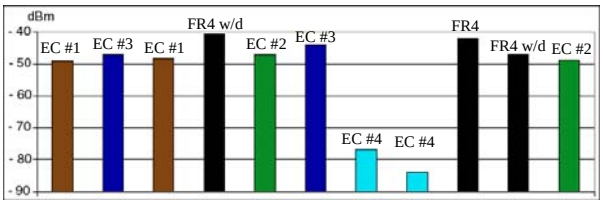

Fig. 9 - Measured power bus noise (1 GHz - 3 GHz).

Fig. 10 shows the measured power bus noise in the 3-5 GHz frequency band. Here also, all of the embedded capacitance schemes are more effective than the discrete decoupling capacitors. The C-Ply boards, which have a theoretical value of input impedance 14 dB - 24 dB lower than the other embedded capacitance boards, have the lowest levels of high-frequency power bus noise.

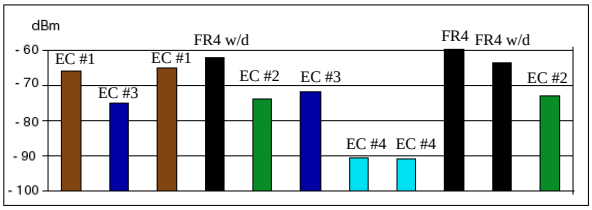

Fig. 10 - Measured power bus noise (3 GHz - 5 GHz).

IV. CONCLUSION

Embedded capacitance can be a very effective tool for reducing power bus noise. At frequencies above 1 GHz, discrete decoupling capacitors lose their effectiveness due to the inductance associated with their connection to the power bus. Embedded capacitance on the other hand is effective at frequencies well above 1 GHz.

Four types of embedded capacitance were evaluated in this study. All of them provided additional capacitance capable of supplying current to active devices on the board. At low frequencies, the current supplied by embedded capacitance is at least as high as the current supplied by discrete capacitors with the same total capacitance. At higher frequencies the current supplied by embedded capacitance is greater because the inductance of the connections to discrete capacitors limits the amount of charge they can supply in a very short time.

REFERENCES

[1] T. H. Hubing, J. L. Drewniak, T. P. Van Doren, D. M. Hockanson, "Power bus decoupling on multi-layer printed circuit boards," IEEE Trans. on EMC, vol. 37, no. 2, May 1995, pp. 155-166.

[2] *Embedded Decoupling Capacitance (EDC) Project - Final Report*. National Center for Manufacturing Sciences, 3025 Boardwalk Ann Arbor, Michigan 48108-3266.

[3] David M. Pozar, *Microwave Engineering*, New York, John Wiley & Sons, 1997, Ch. 6.

[4] Constantine A. Balanis, *Antenna Theory: Analysis and Design*, New York, John Wiley & Sons, 1997, Ch. 14.