Circuit Board Layout for Automotive Electronics

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What is Automotive Electronics?

- **Harsh environment**
- **Cost driven**
- **Weight driven**
- **Reliability is important**
- **10-year-plus life expectancy**
- **Low layer counts**
- **Many mixed signal designs**
- **(but, there are many exceptions)**

EMC Design Guideline Collection

Board Level – Trace routing

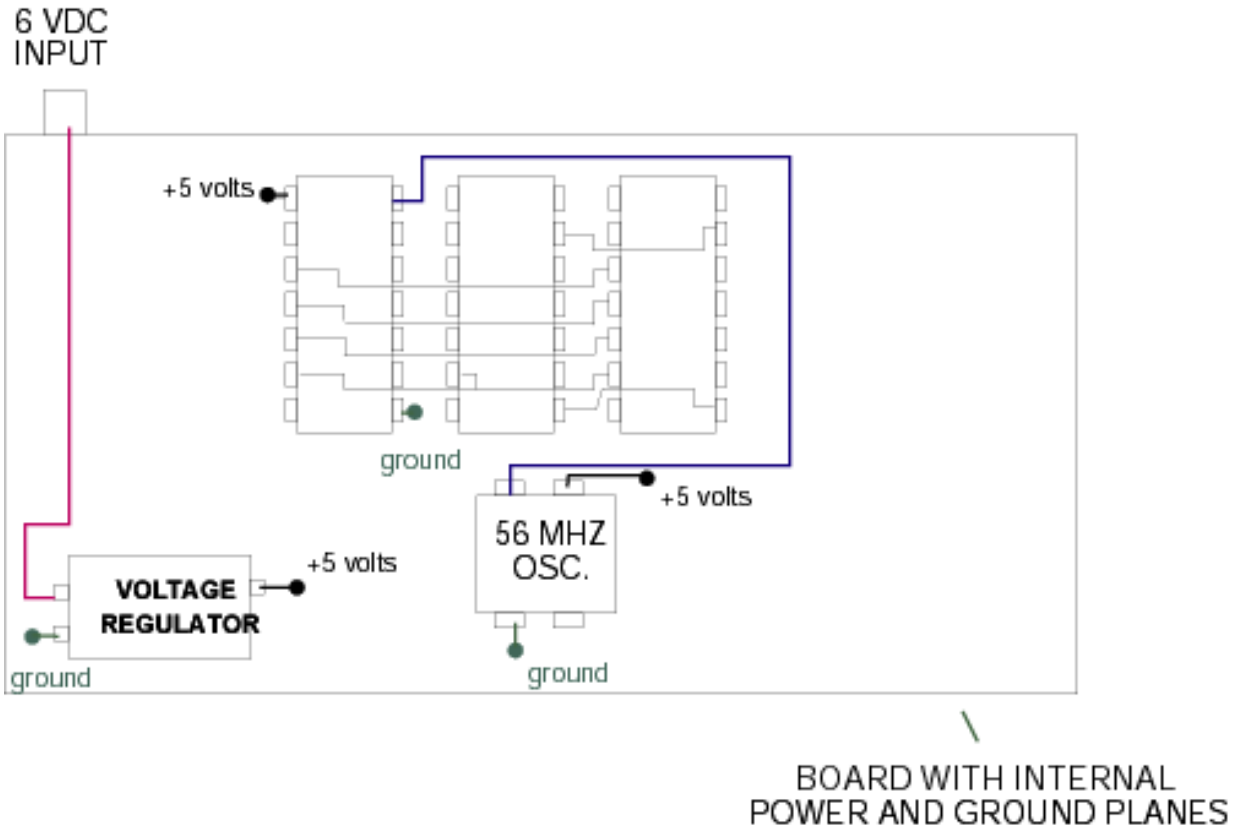
- No trace unrelated to I/O should be located between an I/O connector and the device(s) sending and receiving signals using that connector.
- All power planes and traces should be routed on the same layer.
- A trace with a propagation delay more than half the transition time of the signal it carries must have a matched termination.
- Capacitively-loaded nets must have a total source impedance equal to or greater than one-quarter of the line characteristic impedance or a series resistor must be added to meet this condition.
- Nets driven at faster than 1V/ns slew rate must have a discrete series resistor at the source.
- Guard traces should be used to isolate high-speed nets from I/O nets.
- Guard traces should be connected to the ground plane with vias located less than one-quarter wavelength apart at the highest frequency of interest.
- All power and ground traces must be at least three times the nominal signal line width. This does not include guard traces.
- If a ground or power separation is required, the gap must be at least 3 mm wide.
- Additional decoupling capacitors should be placed on both sides of a power or ground plane gap.
- Critical nets should be routed in a daisy chain fashion with no stubs or branches.
- Critical nets should be routed at least 2X from the board edge, where X is the distance between the trace and its return current path.
- Signals with high-frequency content should not be routed beneath components used for board I/O.
- Differential pairs radiate much less than single-ended signals even when the traces in the pair are separated by many times their distance above a ground plane. However, imbalance in the pair can result in radiation comparable to an equivalent single-ended signal.
- The length of high-frequency nets should be minimized.
- The number of vias in high-frequency nets should be minimized.
- On a board with power and ground planes, no traces should be used to connect to power or ground. Connections should be made using a via adjacent to the power or ground pad of the component.
- Gaps or slots in the ground plane should be avoided. They should ONLY be used in situations where it is necessary to control the flow of low-frequency (i.e. less than 100 kHz) currents.

http://www.cvel.clemson.edu/emc/tutorials/guidelines.html

Signal Routing and Termination

Identify Current Paths

Where does the 56 MHz return current flow?



Identify Current Paths

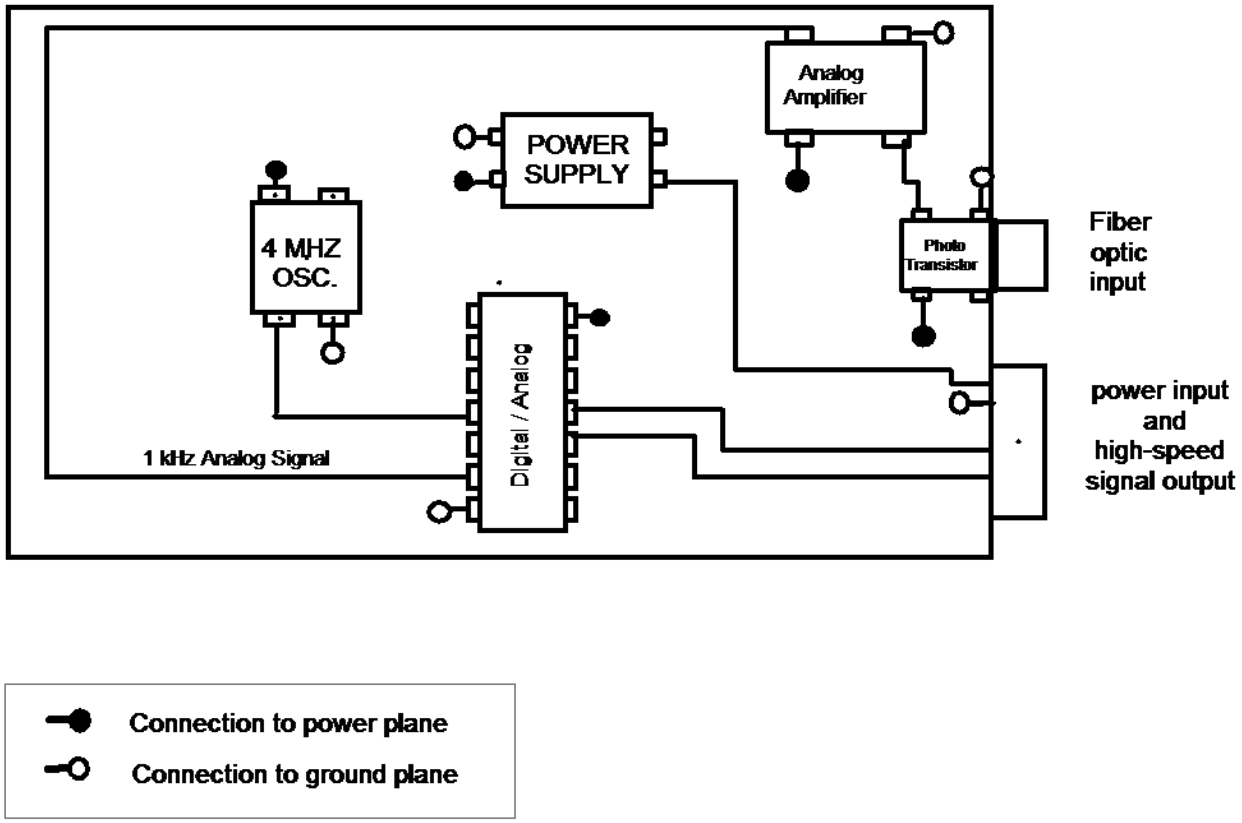
Current takes the path of least impedance!

> 100 kHz this is generally the path of least inductance

< 10 kHz this is generally the path(s) of least resistance

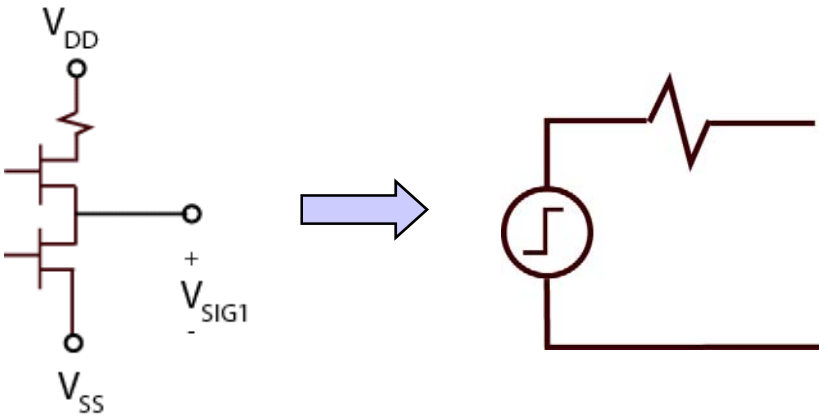
Identify Current Paths

Where does the 1 kHz return current flow?



Signal Termination

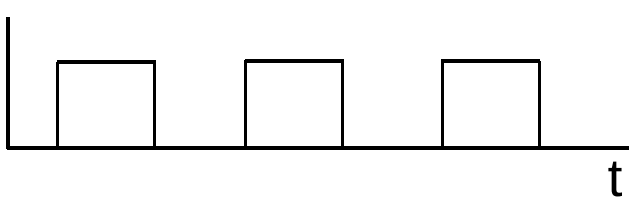
CMOS Driver Model

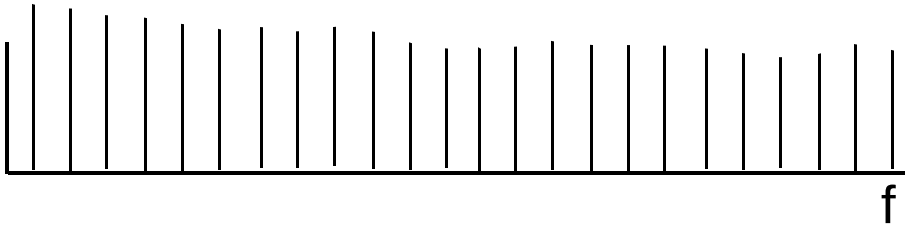


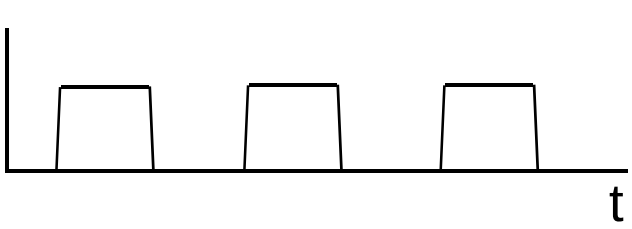
CMOS Input Model

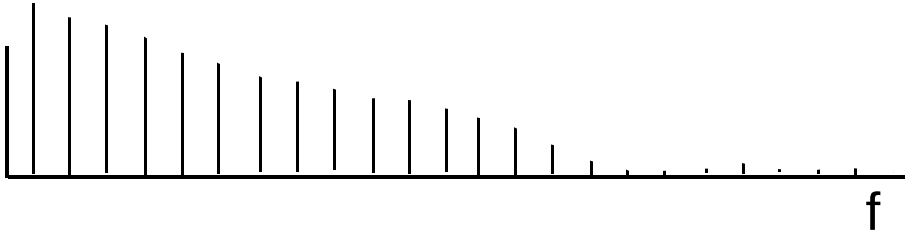
Signal Termination

Digital Signal Voltages





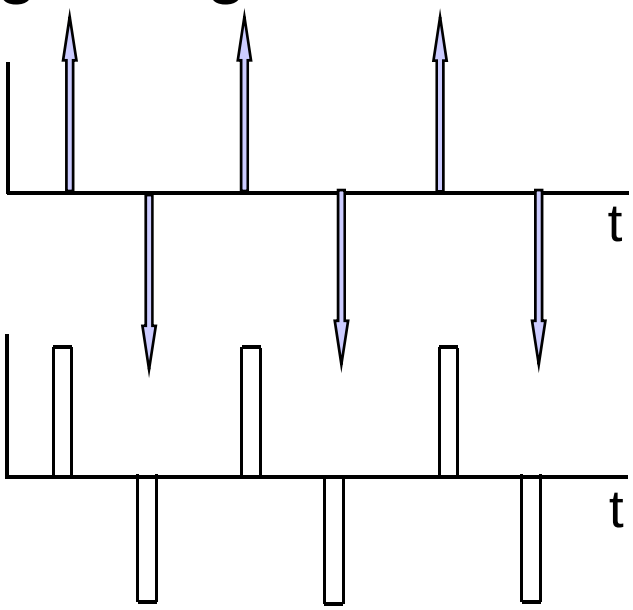


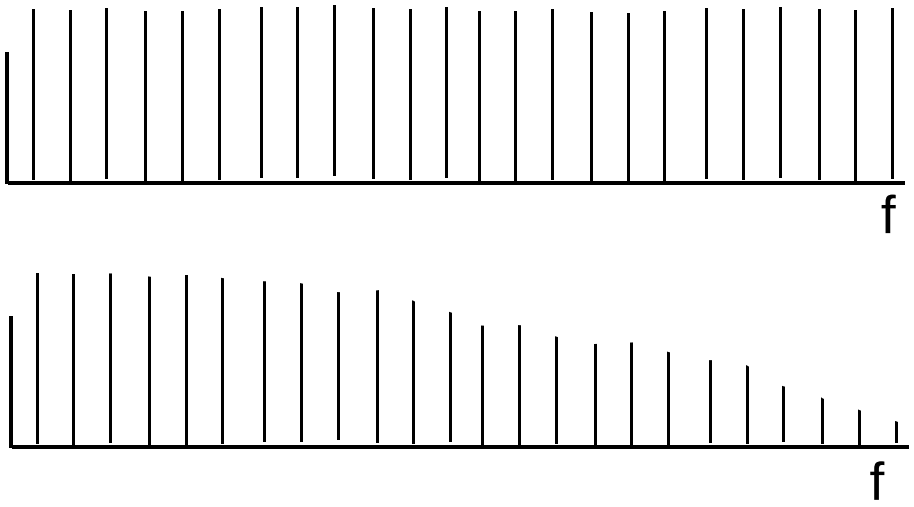


Control transition times of digital signals!

Signal Termination

Digital Signal Currents





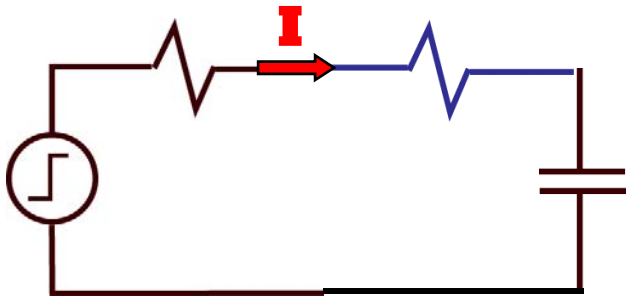
Control transition times of digital signals!

Can use a series resistor or ferrite when load is capacitive.

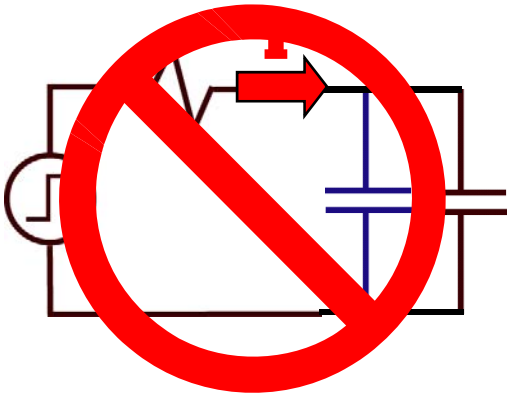
Use appropriate logic for fast signals with matched loads.

Signal Termination

Reducing risetime with a series resistor



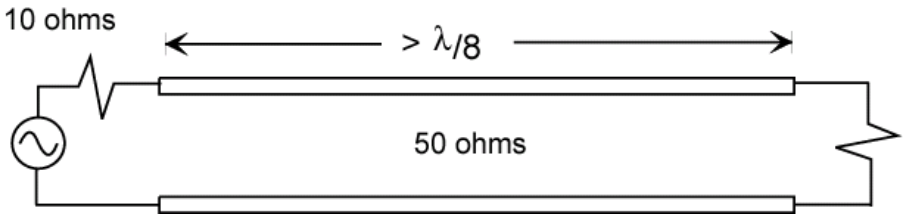
Reducing risetime with a parallel capacitor



Signal Termination

Eliminating ringing with a series resistor

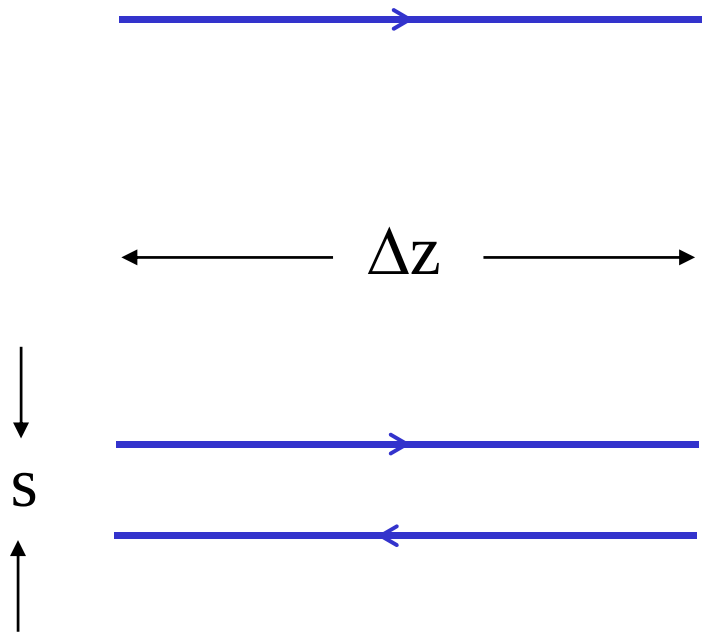
Matched terminations



Identifying the Unintentional Antennas on a Board

Identify Antennas

Common-Mode vs. Differential Mode



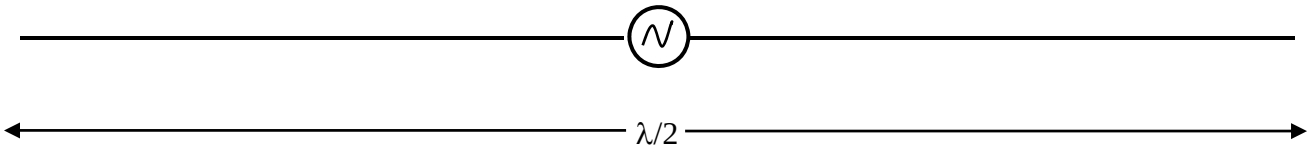
$$E_{max} = 1.26 \times 10^{-6} \frac{|I_c| f \Delta z}{r}$$

$$E_{max} = 1.32 \times 10^{-14} \frac{|I_d| f^2 s \Delta z}{r}$$

$$= 4 \times 10^{-6} \frac{|I_d| f \Delta z}{r} \left(\frac{s}{\lambda} \right)$$

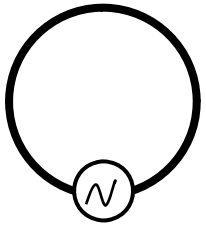
Identify Antennas

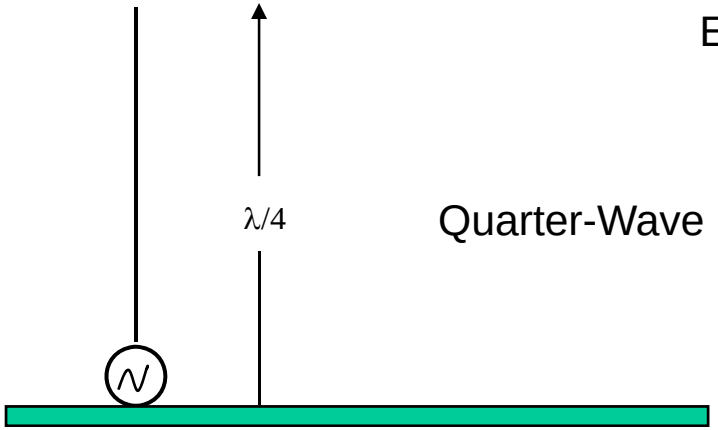
What makes an efficient antenna?



Half-Wave Dipole

Electrically Small Loop



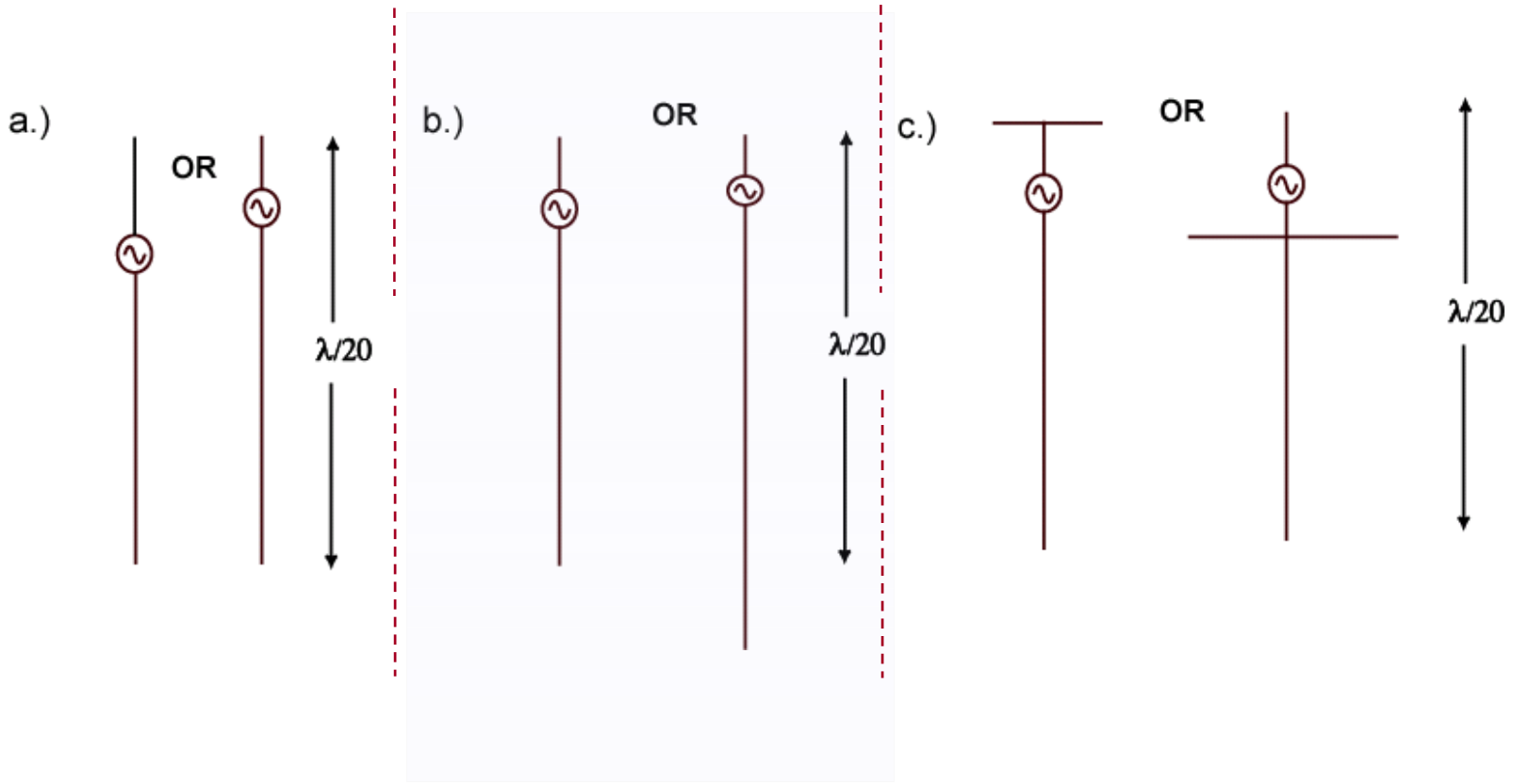


Quarter-Wave Monopole

- **Size**
- **Two Halves**

Identify Antennas

Design Exercise: Which is the more efficient antenna?



Identify Antennas

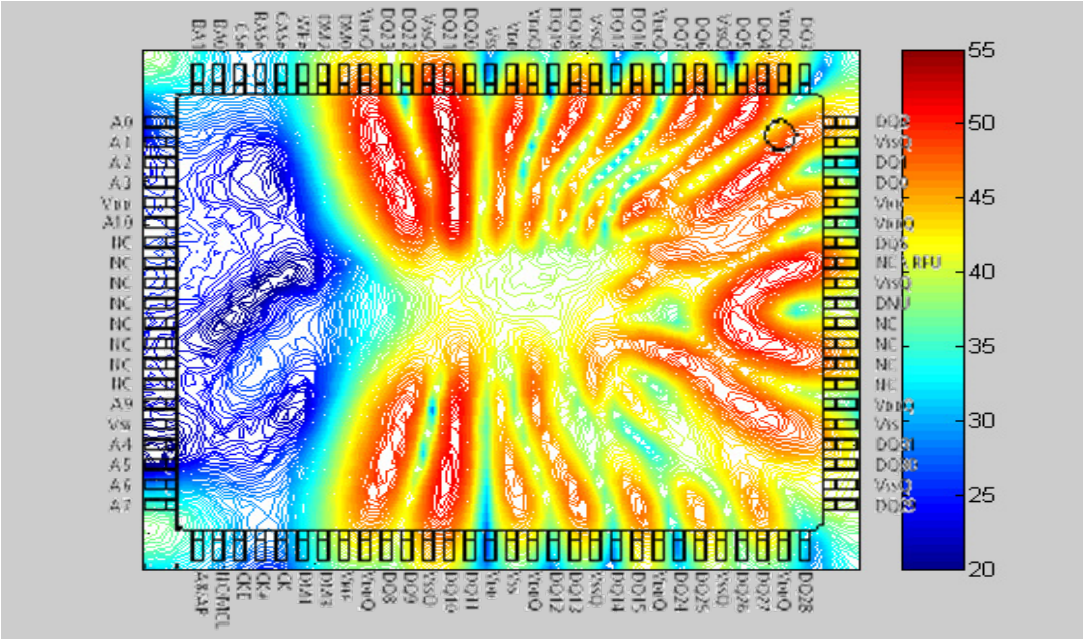
Good Antenna Parts		Poor Antenna Parts	
<100 MHz	**>100 MHz**	**<100 MHz**	**>100 MHz**
Cables	Heatsinks	Microstrip or stripline traces	Microstrip or stripline traces
	Power planes		
	Tall components	Anything that is not big	
	Seams in shielding enclosures		

Free-space wavelength at 100 MHz is 3 meters

Noise Sources and Coupling Mechanisms

Identify Sources

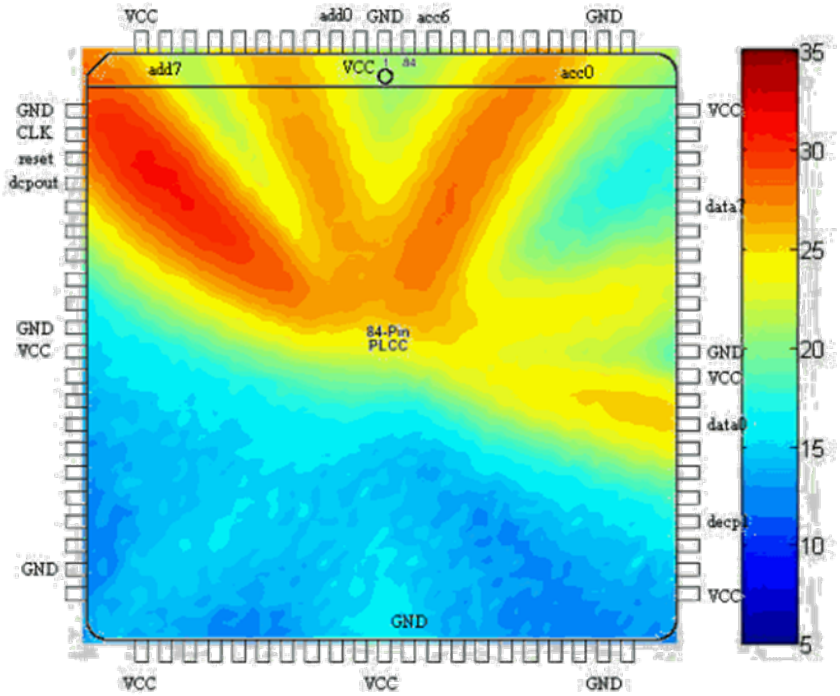
Active Devices (Power Pins)



For some ICs, the high-frequency currents drawn from the power pins can be much greater than the high-frequency currents in the signals!

Identify Sources

Noise on the low-speed I/O



For some ICs, significant high-frequency currents appear on low-speed I/O including outputs that never change state during normal operation!

Recognize Coupling Mechanisms

Noise can be coupled from a source to an antenna by one or more of three different coupling mechanisms:

Conducted

Electric field coupled

Magnetic field coupled

For printed circuit board analysis and design, it is convenient to express these coupling mechanisms in terms of voltage and current.

Recognize Coupling Mechanisms

Voltage Driven

Signal or component voltage appears between two good antenna parts.

Example:

$$V_s = 1 volt @ 500\,MHz$$

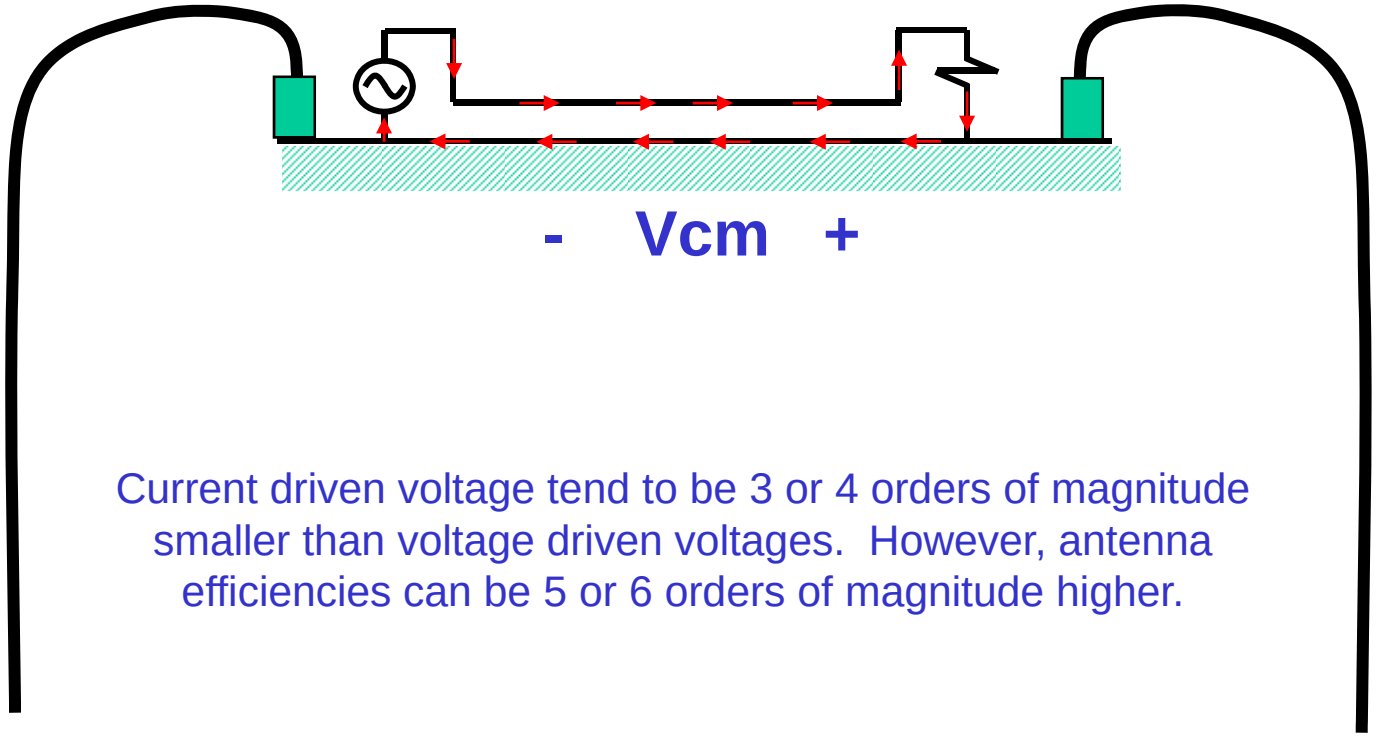
$$E_{rad} \approx 360\,mV/m @ 3 meters$$

More than 60 dB above the FCC Class B limit!

Recognize Coupling Mechanisms

Current Driven

Signal current loop induces a voltage between two good antenna parts.

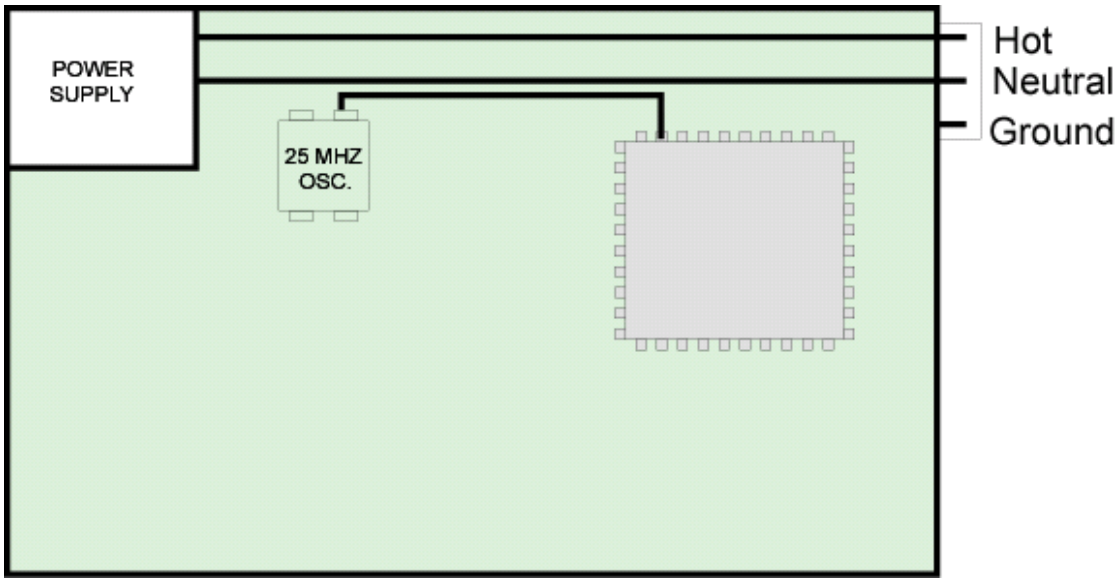


Current driven voltage tend to be 3 or 4 orders of magnitude smaller than voltage driven voltages. However, antenna efficiencies can be 5 or 6 orders of magnitude higher.

Recognize Coupling Mechanisms

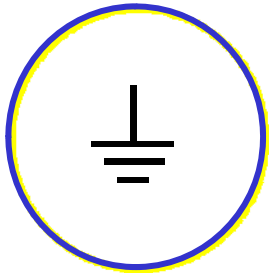
Direct coupling to I/O

Signals coupled to I/O lines carry HF power off the board.



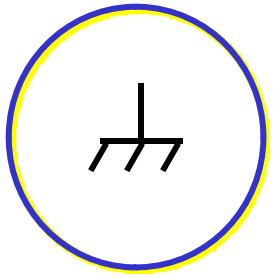
Circuit Board Grounding, Filtering and Shielding

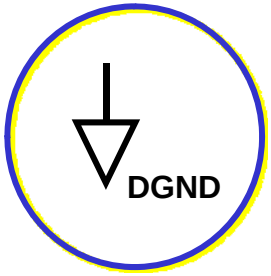
Ground vs. Signal Return



"Whenever I see more than one of these symbols on the schematic, I know there is [EMC] work for us here."

T. Van Doren





Ground vs. Signal Return

Most circuit boards should have  ground!

Why?

Conductors referenced to different grounds can be good antennas.

Signals referenced to two different grounds will be noisy (i.e. include the noise voltage between the two grounds).

Layouts with more than one ground are more difficult, require more space and present more opportunities for critical mistakes.

Excuses for employing more than one ground are generally based on inaccurate or out-dated information.

Ground vs. Signal Return

If grounds are divided, it is generally to control the flow of low-frequency (<100 kHz) currents.

For example,

Isolating battery negative (i.e. chassis ground) from digital ground

Isolating digital ground from analog ground in audio circuits.

This can be necessary at times to prevent common impedance coupling between circuits with low-frequency high-current signals and other sensitive electronic circuits.

DC Power Distribution and Decoupling

Conflicting Rules for PCB Decoupling

Use small-valued capacitors for high-frequency decoupling.

Locate capacitors near the power pins of active devices.

Use 0.01 μF for local decoupling!

Use capacitors with a low ESR!

Avoid capacitors with a low ESR!

Use 0.001 μF for local decoupling!

Run traces from device to capacitor, then to power planes.

Locate capacitors near the ground pins of active devices.

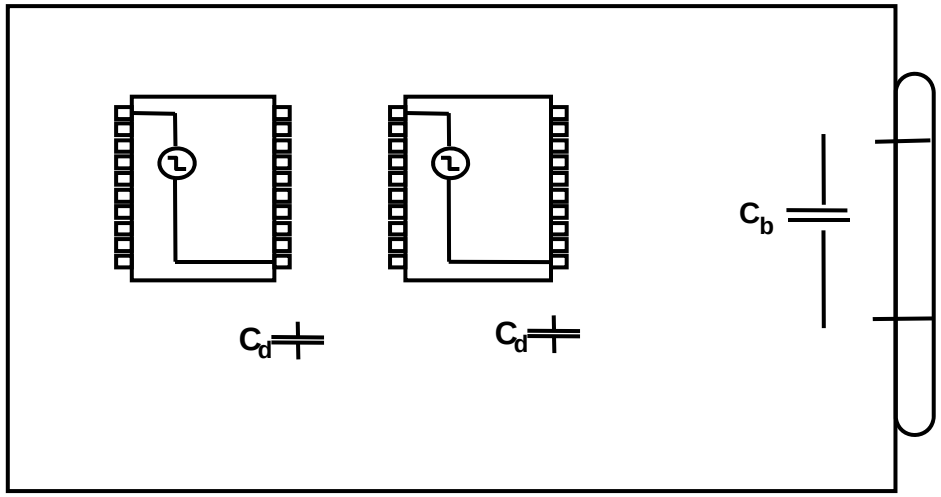
Location of decoupling capacitors is not relevant.

Never put traces on decoupling capacitors.

Use the largest valued capacitors you can find in a given package size.

Local decoupling capacitors should have a range of values from 100 pF to 1 μF!

Boards with Closely Spaced Power Planes



Power Distribution Model ~ (5 - 500 MHz)
Board with power and ground planes

For Boards with “Closely-Spaced” Planes

- **The location of the decoupling capacitors is not critical.**
- **The value of the local decoupling capacitors is not critical, but it must be greater than the interplane capacitance.**
- **The inductance of the connection is the most important parameter of a local decoupling capacitor.**
- **None of the local decoupling capacitors are effective above a couple hundred megahertz.**
- **None of the local decoupling capacitors are supplying significant charge in the first few nanoseconds of a transition.**

R69
D167
D176
C438
103
150
510
106
201

Power Bus Decoupling Strategy

With closely spaced (<.25 mm) planes

- size bulk decoupling to meet board requirements
- size local decoupling to meet board requirements
- mount local decoupling in most convenient locations
- don't put traces on capacitor pads
- too much capacitance is ok
- too much inductance is not ok

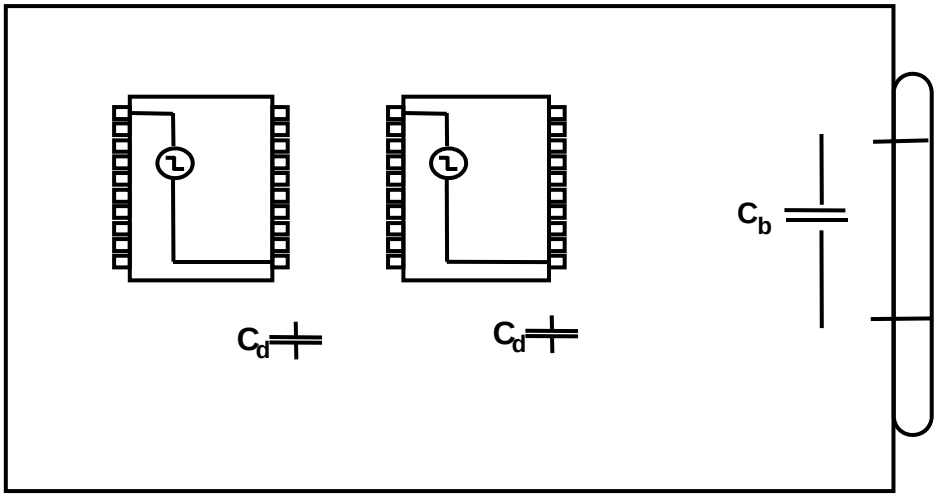
References:

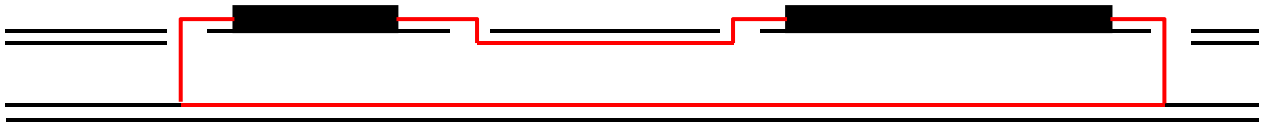
T. H. Hubing, J. L. Drewniak, T. P. Van Doren, and D. Hockanson, "Power Bus Decoupling on Multilayer Printed Circuit Boards," *IEEE Transactions on Electromagnetic Compatibility*, vol. EMC-37, no. 2, May 1995, pp. 155-166.

T. Zeeff and T. Hubing, "Reducing power bus impedance at resonance with lossy components," IEEE Transactions on Advanced Packaging, vol. 25, no. 2, May 2002, pp. 307-310.

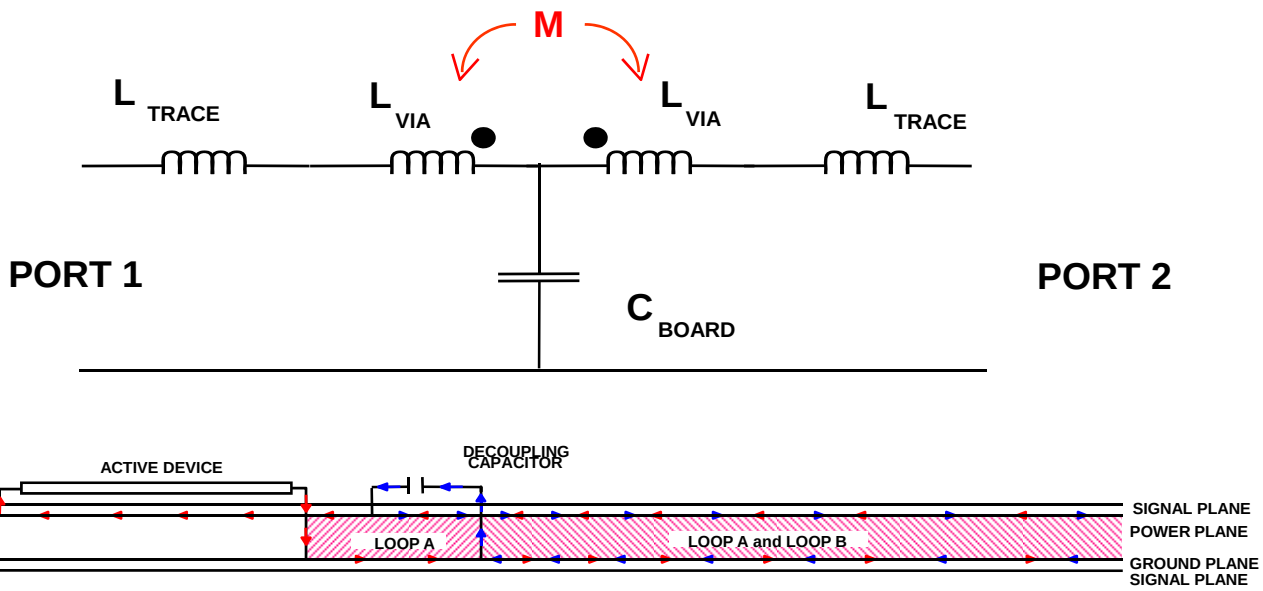
M. Xu, T. Hubing, J. Chen, T. Van Doren, J. Drewniak and R. DuBroff, "Power bus decoupling with embedded capacitance in printed circuit board design," IEEE Transactions on Electromagnetic Compatibility, vol. 45, no. 1, Feb. 2003, pp. 22-30.

Boards with Power Planes Spaced >0.5 mm



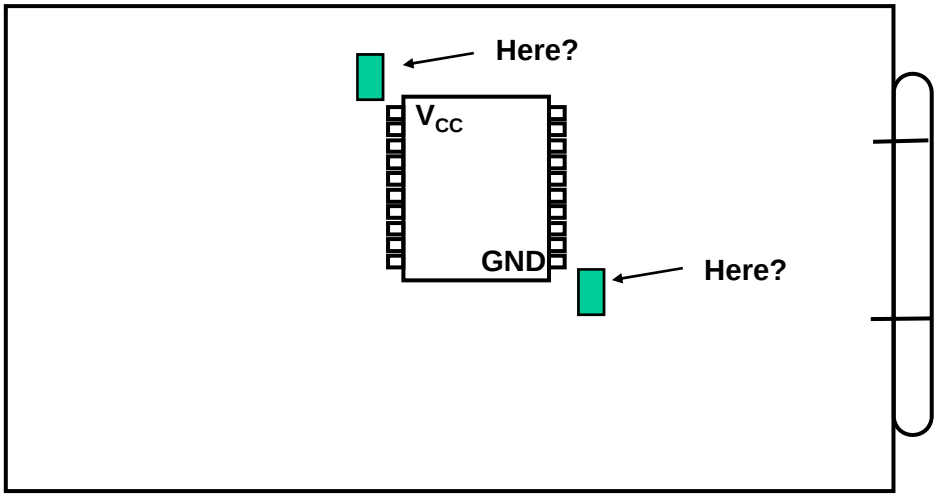


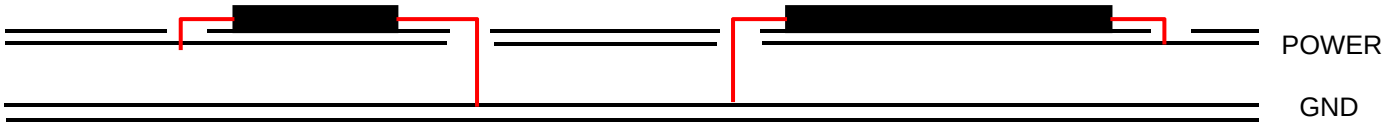
Boards with Power Planes Spaced >0.5 mm



On boards with a spacing between power and ground planes of ~30 mils (0.75 mm) or more, the inductance of the planes can no longer be neglected. In particular, the mutual inductance between the vias of the active device and the vias of the decoupling capacitor is important. The mutual inductance will tend to cause the majority of the current to be drawn from the nearest decoupling capacitor and not from the planes.

Where do I mount the capacitor?






U7B1
SMC
FDC37C677
A9731-A5491O
6C7727.1
©PHOENIX 1995 MK42
RP7C1
220
220
C7B1
C7C1
C7C2
R7C3
R7C1
R7C2
RP7C3
R7B2
U8C1

For Boards with “Widely-Spaced” Planes

- **Local decoupling capacitors should be located as close to the active device as possible (near pin attached to most distant plane).**
- **The value of the local decoupling capacitors should be 10,000 pF or greater.**
- **The inductance of the connection is the most important parameter of a local decoupling capacitor.**
- **Local decoupling capacitors can be effective up to 1 GHz or higher if they are connected properly.**

Power Bus Decoupling Strategy

With widely spaced (>.5 mm) planes

- size bulk decoupling to meet board requirements
- size local decoupling to meet device requirements
- mount local decoupling near pin connected to furthest plane
- don't put traces on capacitor pads
- too much capacitance is ok
- too much inductance is not ok

References:

J. Chen, M. Xu, T. Hubing, J. Drewniak, T. Van Doren, and R. DuBroff, "Experimental evaluation of power bus decoupling on a 4-layer printed circuit board," *Proc. of the 2000 IEEE International Symposium on Electromagnetic Compatibility*, Washington D.C., August 2000, pp. 335-338.

T. H. Hubing, T. P. Van Doren, F. Sha, J. L. Drewniak, and M. Wilhelm, "An Experimental Investigation of 4-Layer Printed Circuit Board Decoupling," *Proceedings of the 1995 IEEE International Symposium on Electromagnetic Compatibility,* Atlanta, GA, August 1995, pp. 308-312.

J. Fan, J. Drewniak, J. Knighten, N. Smith, A. Orlandi, T. Van Doren, T. Hubing and R. DuBroff, "Quantifying SMT Decoupling Capacitor Placement in DC Power-Bus Design for Multilayer PCBs," IEEE Transactions on Electromagnetic Compatibility, vol. EMC-43, no. 4, Nov. 2001, pp. 588-599.

Power Bus Decoupling Strategy

With no power plane

- layout low-inductance power distribution
- size bulk decoupling to meet board requirements
- size local decoupling to meet device requirements
- two caps can be much better than one
- avoid resonances by minimizing L

References:

T. Hubing, "Printed Circuit Board Power Bus Decoupling," *LG Journal of Production Engineering*, vol. 3, no. 12, December 2000, pp. 17-20. (Korean language publication) .

T. Zeeff, T. Hubing, T. Van Doren and D. Pommerenke, "Analysis of simple two-capacitor low-pass filters," IEEE Transactions on Electromagnetic Compatibility, vol. 45, no. 4, Nov. 2003, pp. 595-601.

Power Bus Decoupling Strategy

Low-impedance planes or traces?

- choice based on bandwidth and board complexity
- planes are not always the best choice
- it is possible to achieve good decoupling either way
- trace inductance may limit current to active devices

Planes widely spaced or closely spaced?

- want local or global decoupling?
- want stripline traces?
- lower impedances obtainable with closely spaced planes.

Strategies for Analog/Digital/Mixed-Signal PCB Layout

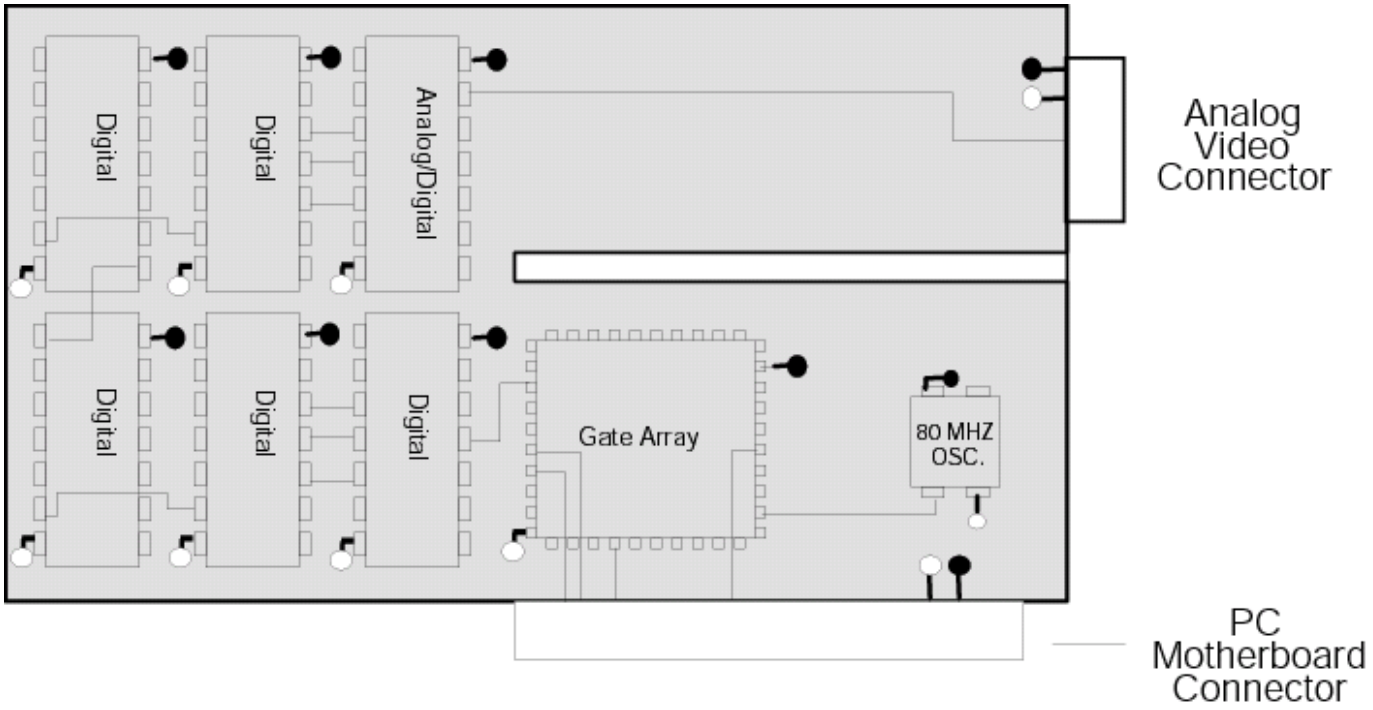
Mixed-Signal Designs

If you have analog and digital returns that must be isolated (to prevent common-impedance coupling):

- Route the returns on separate conductors
- Provide a DC connection at the one point (or in the one area) where the reference potential must be the same.
- This must include everyplace where a trace crosses the boundary between the analog and digital regions.

Mixed-Signal Designs

Example: How would you modify this design?



Design Guideline Review

Most important guidelines:

- Keep signal loop areas small
- Don’t locate circuitry between connectors
- Control transition times in digital signals
- Never cut gaps in a solid return plane

Summary

Don’t rely on design guidelines!

- Visualize signal current paths
- Locate antennas and crosstalk paths
- Be aware of potential EMI sources
- Use common sense!