

TECHNICAL REPORT: CVEL-10-019

Evaluation of Low-Inductance Capacitor Configurations for High Frequency Circuit Board Decoupling

Hocheol Kwak, Dr. Todd Hubing

Clemson University

September 26, 2010



Table of Contents

ABSTRACT	3
I. Introduction	4
II. Plate Orientation Effect on the Inductance of Conventional MLCCs	6
A. 2D modeling of horizontal and vertical plates	6
B. Modeling stacked plate pairs as blocks	7
C. 3D modeling for analyzing effective inductance	9
E. Effect of the dimensions of a single block on the effective inductance	11
III. Inductance Calculations for Advanced Packaging in High-Performance Computing Applic	ations
	14
A. Decoupling schemes for high-performance packaging	14
Resistance on-chip	16
Loop inductance off-chip	18
Loop inductance in top/bottom-side of package substrate	18
C. Inductance calculations for MLCCs on a packaging substrate	20
Loop inductance of two vias at different packaging levels	20
IV. New Capacitor Configurations for Advanced Packaging	23
A. Capacitive-stem capacitor	23
B. Modeling of effective inductance	24
C. Transfer function analysis of proposed capacitors	30
V. Conclusion	31
References	31



ABSTRACT

In high-speed circuits, the value of the inductance associated with a connection to a MLCC (Multi-Layer Ceramic Capacitor) is often more important than the nominal value of the capacitor. This paper has three main sections. The first section discusses the importance and the meaning of the connection inductance associated with MLCCs. The second section analyzes the effect of plate orientation in MLCCs. It demonstrates that vertically oriented plates have no more or less inductance than horizontally oriented plates when the overall dimensions of the plate stack are similar. The third section describes decoupling capacitance options at the various levels of a high-speed circuit (i.e. on-die, on-package and on-board). This section describes how the geometries at each level affect the relationship between connection inductance and resistance, and therefore determine the range of frequencies that decoupling at each level is likely to be effective.

The fourth section describes innovative low-inductance capacitor configurations. A capacitor having a stem that is designed to be inserted into a single, large-diameter via hole drilled in a printed circuit board is described, wherein the stem may have conductive rings for making the positive and negative connections to the printed circuit board power distribution planes. Inside the capacitive stem, current, or at least a portion thereof, may flow to the main body of the capacitor through low-inductance plates that are interleaved to maximize their own mutual capacitance and, therefore, minimize the connection inductance. Alternately, the capacitor may include a coaxial stem that forms a coaxial transmission line with the anode and cathode terminals forming the inner and outer conductors. Capacitive-stem capacitor configurations are described and their connection impedance is compared to that of standard surface-mounted capacitors.



I. Introduction

A decoupling capacitor acts as a low impedance source of current to minimize supply voltage fluctuations caused by the rapid switching of active devices. Typically, the decoupling capacitance for silicon processors is implemented in multiple stages ranging from large bulk capacitors physically located near regulated power supplies, to board-level capacitors that stabilize the voltage supply on the printed circuit board (PCB), to package-level decoupling incorporated on the processor package, and die-level capacitance located on the die itself. This decoupling network regulates the current moving through the system between the silicon die and the regulated power supply. The required response time of the decoupling capacitors decreases as the current moves towards the processor. The impedance of the power distribution bus versus frequency can be equated to the decoupling capacitor response time. At relatively low frequencies, a low impedance is achieved with high capacitance (i.e., low capacitive reactance). At relatively high frequencies, low impedance is obtained by using capacitors with a low connection inductance. In between these frequency ranges, there is a series resonance. At resonance, the impedance is equal to the equivalent series resistance (ESR) of the capacitor. Therefore, to make a capacitor work at the highest possible frequencies, it should have the lowest possible connection inductance.



Fig. 1. Simple RLC equivalent circuit of a capacitor and connection inductance loop of an MLCC mounted to PCB planes.

When considering the parasitics of bypass capacitors, a widely used simple model is a series R-L-C network, where C is the capacitance of the part, R is the Equivalent Series Resistance (ESR) and L is the connection inductance as illustrated in Fig.1. The capacitance may be frequency dependent, primarily due to a redistribution of the current at very high frequencies. The inductance is determined by the connection of the capacitor to the rest of the circuit as well as the geometry of the capacitor itself.



In a multi-layer ceramic capacitor (MLCC), the inductance can be slightly higher at low frequencies where the resistance in the copper plates forces the current to flow uniformly through all plates. At high frequencies, most of the current flows along the lowest inductance path and is concentrated on the lower plates. The parasitic inductance of MLCCs is becoming more and more important in the decoupling of high-speed digital systems. The relationship between the inductance and the ripple voltage induced on the DC voltage line is, $V=L\times di/dt$. The parasitic inductance results from the interaction of magnetic flux created by the electric current flow in and out of the device on a circuit board. The current path or loop includes not only the multilayer capacitor's internal electrodes and external termination, but also the power planes, vias, mounting pads and solder fillets of the substrate/packages. At very high frequencies and low connection inductances, the current path is not defined by the entire capacitor multilayered stack, but most of the current is confined to the lower internal electrodes as the path of least impedance for the current flow [1].



Fig. 2. Moving decoupling capacitors next to bare chip [3].

Over the past 10-12 years, decoupling capacitors have evolved into various types. This progress has been driven by the requirement to lower the inductance of power distribution systems to keep up with faster switching speeds and increased transistor density in silicon processors. The board pads and vias form closely spaced cancellation paths that support low inductance design strategies. When component companies characterize their devices, considerable care is taken to extract the influence of the test coupon to give a "part-only" ESL (Equivalent or Effective Series Inductance). However, inductance is a property of current loops and a low-inductance capacitor does not have a well-defined ESL independent of its connection to the board. The inductance of a mounted capacitor does not equal the sum of the connection inductance and the inductance internal to the



capacitor unless there is no mutual inductance between the two portions of the loop. For lowinductance capacitors, this mutual inductance is always significant, making published values for the ESL practically meaningless.

As illustrated in Fig. 2, high-frequency noise reduction in a power distribution bus requires moving the decoupling capacitance close to the bare chip. As packaging structures continue to evolve, opportunities to develop new, optimal, low-inductance decoupling capacitors will continue to present themselves.

II. Plate Orientation Effect on the Inductance of Conventional MLCCs

In high-speed circuits, the value of the inductance associated with a connection to an MLCC (Multiple-Layer Ceramic Capacitor) is often more important than the nominal value of the capacitor. ESL is a value often quoted in capacitor data sheets for comparing different capacitor designs. However, the actual connection inductance for small SMT (Surface Mount Technology) capacitors depends on several parameters that are not part of a typical ESL measurement. The actual high-speed performance of an SMT capacitor is generally unrelated to its nominal ESL. Capacitors that have the lowest published ESL may not be the best capacitors to use in a particular application. In this section, the effect of electrode (plate) orientation on the connection inductance of MLCC capacitors is investigated. It is shown that a single vertical plate has a higher inductance than a single horizontal plate when mounted over a board with a ground plane. However, as more vertically oriented plates are stacked side by side, the value of the self-inductance decreases significantly, whereas the inductance of horizontal plates that are vertically stacked is relatively independent of the number of plates in the stack. For large stacks, the overall width of the stack is the most significant parameter affecting the connection inductance. When the width and height of the stacked plates is the same, the effective inductance with either orientation is the same. Thus, capacitors with vertically oriented multiple plates do not inherently provide an advantage over capacitors with horizontally oriented multiple plates. The primary capacitor geometry parameters that affect the connection inductance are the plate stack width (which should be maximized) and the loop area associated with current flowing into and out-of the capacitor plates (which should be minimized).

A. 2D modeling of horizontal and vertical plates

Two-dimensional models were used to isolate the contributions of the plates from the contributions of the end caps to the overall connection inductance of typical MLCC geometries. These models are illustrated in Fig. 3.

<u>CVEL</u>

THE CLEMSON UNIVERSITY VEHICULAR ELECTRONICS LABORATORY



Fig. 3. Cross-sectional view of two-dimensional plate geometry.

The simulation of the self-inductance of a single plate over a ground plane was performed using a 0.4342 mm by 0.4342 mm plate located 0.0829 mm over a ground plane. The calculated inductance per unit length values were multiplied by a length of 0.94 mm (corresponding to a 0402 capacitor package) to give a value for the partial-inductance associated with the plates.

As the results in Table I indicate, the effective inductance of a vertically oriented single plate is significantly higher than that of a horizontally oriented plate. As the current spreads across the surface of the vertically oriented plate, the loop area formed between the plate current and the ground current increases. The horizontal plate provides the lowest inductance current path for a given height and plate surface area.

	Self-inductance (Plate)	Mutual-inductance (GND-to-Plate)	Loop inductance (SI – MI)
Horizontal plate	0.899 nH	0.772 nH	0.128 nH
Vertical plate	0.972 nH	0.750 nH	0.222 nH

Table I. Partial Inductance of a single plate (length = 0.94 mm)

The two top plots in Fig. 4 illustrate the magnetic field intensity and the bottom plots show the lines of magnetic flux for each configuration evaluated.

B. Modeling stacked plate pairs as blocks

Quasi-static models of the MLCC inductance require shorting the positive and negative electrodes together where the plates overlap. This allows the current to spread out over the plates in the same way that it would at high frequencies, while eliminating the capacitive reactance from the models. Plate pairs are represented as solid conducting "blocks" as illustrated in Fig. 5. The three key dimensions of the structure, w, t and l denote the width, thickness and length of the stacked plates respectively.



THE CLEMSON UNIVERSITY VEHICULAR ELECTRONICS LABORATORY



Fig. 4. Magnetic field intensity (top) and magnetic flux lines (bottom) for each plate orientation.



Fig. 5. Simplified inductance models for MLCCs.



Although the inductance of a single plate is higher when the plate is oriented vertically, this inductance decreases as we add more plates in parallel. Single horizontal plates have lower inductance, but stacking more plates on top of the first one has little effect on the high-frequency inductance. To illustrate this, we use the model in Fig. 6. The parameters of a 2D single block were varied to determine the effect of the plate stack size and orientation on the capacitor inductance. A block represents a set of internal electrodes forming the capacitor structure for high-frequency current flow. The ground conductor under the block is an ideal ground plane. The stack size (t for the horizontal blocks and w for the vertical blocks) was increased from 1 to 11 plate-pair thicknesses. A single plate-pair thickness was 0.0342 mm. The height of the block above the plane was 0.0829 mm.



Fig. 6. Parameter variations of single block MLCC model.

As shown in Fig. 7, the self-inductance of the vertically oriented block is much higher than that of the horizontally oriented block. As the number of blocks increases, the inductance of the vertically oriented blocks decreases significantly. However, the inductance of the horizontal blocks shows little change as the number of blocks increases.

C. 3D modeling for analyzing effective inductance

Fig. 8 illustrates a 3D model for an MLCC. It is not possible to quantify a meaningful inductance for this structure without specifying a test fixture that completes the current loop. Therefore, a 3D structure for extracting effective inductance was defined. The structure consisted of a two-layer printed circuit board with an input port and a capacitor mounting port as illustrated in Fig. 8.





Fig. 7. Partial self-inductance values by the stack size.



Fig. 8. Top and side views of 3D model for an MLCC mounting fixture.



Commercial simulation software (Ansoft Q3D ExtractorTM) was to determine the effect of the stack size on the effective inductance. The AC frequency was set to 1 GHz. The number of blocks was varied from 1 to 11 with a slight dielectric gap between adjacent blocks in both orientations as illustrated in Fig. 9. The stack order was from bottom to top for the horizontal orientation and from right to left for the vertical orientation.



Fig. 9. Three-dimensional view of multiple block MLCC model.

The effective inductance of a vertically oriented block found to be higher than that of a horizontally oriented block just as it was in the 2D simulation results. As the number of blocks increased so that the outer dimensions of the stacks were the same, the effective inductances approached the same value for both block orientations as shown in Fig. 10.

E. Effect of the dimensions of a single block on the effective inductance

This process was repeated without the dielectric gaps between blocks as illustrated in Fig. 11. The effective inductance of a single block was analyzed as a function of the parameters t or w. The stack size was incremented in 0.02-mm steps, with the final dimension denoted as t_e or w_e .





Fig. 10. Effective inductance values by the number of blocks.



Fig. 11. Parameter variations of 3-dimensional single block MLCC model.



As shown in Fig. 12, the results mimic the results obtained with the dielectric between each block. For the horizontal orientation, as the height, t, increased, the effective inductance varied little. For the vertical orientation, the effective inductance decreased as the width of the stack increased.



Fig. 12. Effective inductance values by the step size of plate geometry.

The results in presented indicate that a vertically oriented single plate has a higher inductance than a horizontally oriented single plate. The simulation of multiple plates indicates that as more vertically oriented plates are stacked to increase the overall width of the capacitor, the value of the capacitor's inductance decreases. Stacking horizontal plates vertically has relatively little effect on the inductance, since most of the high-frequency current flows only on the lower plates. The inductance of the plate stack is primarily a function of the width and height of the stack and relatively independent of the plate orientation. Therefore, MLCC designs with vertically oriented plates do not necessarily provide an advantage over designs with horizontally oriented plates in terms of providing the lowest possible connection inductance.



III. Inductance Calculations for Advanced Packaging in High-Performance Computing Applications

Effective decoupling is crucial for the optimum performance of the power distribution network in an electronic system. As component-packaging technologies evolve enabling tighter integration and faster performance of electronic systems, it is essential to develop better decoupling strategies. This section describes several new or proposed packaging structures and evaluates the connection inductance associated with possible decoupling locations. As expected, connections made on the chip tend to have a lower inductance than connections made on the package; and connections made on the package tend to have a lower inductance than connections made on the board. This illustrates the importance of providing decoupling capacitance as close to the chip as possible in order to maximize the effective bandwidth of the power distribution network.

Power bus decoupling issues in electronic systems are shifting from the printed circuit board to the component packaging. This trend is being driven by the miniaturization of electronic systems and the shift of the package manufacturing process to the IC foundry level. Traditional wire bonding technology is steadily being replaced by area array (bump) interconnections and threedimensional silicon integration technologies.

The evolution of advanced packaging techniques is being driven by two electronic device platforms; mobile communication applications with an emphasis on miniaturization, and computing applications with an emphasis on high performance. High-density integration is required for both platforms. Ultimately, the roadmap of both platforms calls for the implementation of SOC (System-on-Chip) or SOP (System-on-Package) structures including; 3D chip stacks, silicon carrier packaging, silicon interconnection or bonding, copper-to-copper stud bonding and integrated decoupling capacitors [5].

Advanced packaging includes wafer-level and 3D stacked ICs, as well as traditional packaging technologies [6]. Vertical interconnection technology for different packaging levels is evolving from traditional wire bonding and flip-chip bumping to wafer-level packaging and copper-to-copper bonding. Key design parameters for power bus decoupling of advanced packaging structures can be categorized depending on the location or type of decoupling capacitor. Decoupling capacitors can be discrete, singulated or distributed. They can be individual local capacitors or global arrays.

A. Decoupling schemes for high-performance packaging

Table II shows key design parameters affecting the decoupling capacitor connection inductance at different interconnection levels. Typically, the vertical scaling dimensions become smaller as the interconnections go from the PCB level to the IC level.

Table II. Key design parameters by interconnection levels



Interconnec	tion level	Key design parameters	Vertical scaling	
DCD	trace	w (width), t (thickness), l (length)	mm	
FCD	via	d (diameter), h (height), s (distance)	~ 11111	
BGA	bump	d (diameter), p (pitch; I/O pitch)	~ 500µm	
	trace	w (width), t (thickness), l (length)		
Package substrate	aora via	d (diameter), h (height; S_PG), s	~ mm	
	core via	(distance; d_mutual)		
Flip chip	µ-bump	d (diameter), p (pitch; I/O pitch)	~ 100 µm	
Silicon substrate	through-silicon	d (diameter) h (height) s (distance)	50~300 um	
Silicon substrate	via	<i>a</i> (diameter), <i>n</i> (neight), s (distance)	50~500 μm	
	chip	W (width), L (length)	~ 10 µm	
IC	through-silicon	d (diameter), h (height; h_tvs), s	. 10 um	
IC.	via	(distance; d_tvs)	~ 10 µm	
	Cu-to-Cu bond	d (diameter), p (pitch; I/O pitch)	~ µm	
Decoupling		w (width), h (SMT height; h_decap),		
	MLCC	l (length; l_decap)	Variable	
capacitoi		p (terminal pitch)		



Fig. 13. Formulas for loop inductance of common circuit geometries [24].



The following sections describe key design parameters for several packaging structures with the decoupling capacitor located on-chip, off-chip, and on the top or bottom of the carrier. Formulas for calculating the inductance and resistance of circuit board configurations are provided in Fig. 13.

Fig. 14 illustrates five possible locations for the decoupling capacitors in a high-performance package; stacked on chip, stacked on Si-carrier, top side of package substrate, bottom side of package substrate, and embedded in the package substrate. The current paths, including the dominant factors affecting the loop inductance, are indicated for each location.



Fig. 14. Possible locations of decoupling capacitors for high-performance packaging.

As illustrated in Fig. 14, the 'stacked-on-chip' location is closest to the source and permits the lowest possible connection inductance. A typical inductance calculation for a 'stacked-on-chip' decoupling capacitor is determined by modeling the current path as a pair of vias between two solid planes. This model is reasonable because the on-chip grids that connect to the vias are relatively wide and contribute little to the overall path inductance. For example, suppose that the radius of the through-silicon vias is 5 µm, the distance between adjacent vias is 50 µm, and the height of a die is about 200 µm. Via inductances associated with these vias can be calculated using the formula in Fig. 13. In this case, the connection inductance would be 92 pH. The via resistance would be $R = 2h/\sigma\pi r^2 = 89 \text{ m}\Omega$. In this case, the inductance would be more important than the resistance at frequencies above 150 MHz.

Resistance on-chip

A decoupling capacitor placed within a die is referred to as an on-chip decoupling capacitor. The loop area to be considered when calculating the inductance includes the on-chip decoupling capacitor, power/ground metal and the circuit being decoupled. The loop area should be minimized



to reduce the resistance as well as the inductance of the connection. In many cases, the resistance of the connection overwhelms the inductance ($R > j\omega L$).



Fig. 15. On-chip decoupling capacitor in power/ground metal grid.

For example, a rectangular loop of wire in a 0.13- μ m process might have a total length of 20 μ m and a width of 5 μ m. Assuming that the wire thickness was 1 μ m and the conductivity of the copper was 5.7 x 10⁷ S/m, the resistance of the wire loop would be 35 m Ω . The inductance of the same loop would be approximately 1.5 pH. Therefore, the resistance would be more important than the inductance at all frequencies below 3.7 GHz.







Loop inductance off-chip

As illustrated in Fig. 16, the decoupling capacitor can also be stacked on the die, placed on the top or bottom side of a silicon carrier substrate, or even embedded in the silicon substrate using TSV (through-silicon via) technology to connect the switching gates to the decoupling capacitor. For these 'off-chip' locations, the interconnections should be close to the circuit being decoupled in order to minimize the loop area.

Inductance instead of resistance is more likely to be the key parameter in an off-chip configuration. For example, if through-silicon vias have a length of 300 μ m, a diameter of 70 μ m and a spacing of 100 μ m, the loop inductance of the vias would be 63 pH; whereas these same vias would only have about 0.9 m Ω of resistance. Therefore, at frequencies above 2.3 MHz, the inductance would dominate.

Loop inductance in top/bottom-side of package substrate

Design strategies for mounting decoupling capacitors on either side of the package substrate can be divided into two cases depending on the distance between the power planes of a multi-layer package substrate [7].



Fig. 17. Current loops in the top side of package substrate.

On circuit boards with closely spaced power planes, ~ 0.3 mm or less, the location of the local decoupling capacitors is not critical. To minimize the connection inductance, all local decoupling capacitors should be mounted on the face of the board nearest to the planes. Capacitors should be connected directly to the planes without using traces. Vias should be in or adjacent to the capacitor mounting pads as close to each other as possible. When a chip and decoupling capacitor are both mounted on the top side of the package substrate, the inductance of the loop can be expressed as the

<u>CVEL</u>

THE CLEMSON UNIVERSITY VEHICULAR ELECTRONICS LABORATORY

sum of the inductances of the two half-loops above the top plane and the inductance of the loop between the planes. (Note that it is the absence of any mutual inductance that allows us to simply add the two partial inductances of these half-loops.)

When the spacing between the planes is less than ~ 0.3 mm, the inductance of the loop between the planes tends to be small relative to the connection inductance above the planes. When the spacing between the planes is greater than ~ 0.5 mm, the inductance between the planes is no longer negligible. In fact, by placing the vias that carry current to and from the lower plane near each other, it is possible to take advantage of the mutual inductance between these vias to force the current to be drawn from the decoupling capacitor rather than the planes. This reduces the noise on the power planes [7]. Therefore, when the planes are >0.33 mm apart, it is important to locate the decoupling capacitors near the source.

When the capacitor is mounted on the same side of the board as the device it is decoupling, it can share the via connecting to the lower plane with the active device. When the capacitor is on the opposite side of the board, the calculation of the inductance is done using the same formulas used when the capacitor is on the same side as the active device. However, the currents flowing on the vias in between the planes are now being drawn from different planes. The rules for locating the decoupling capacitors are the same, except it is no longer possible to share the via that carries current between the planes. Therefore, the active device and the capacitor should each have their own vias connecting to the planes (i.e. they should not share vias).



Fig. 18. Current loops in the bottom side of package substrate.

B. Inductance calculations for MLCCs on a packaging substrate

Loop inductance of two vias at different packaging levels

Table III shows the inductance of two vias between planes at different interconnection levels and typical values of capacitance available at each of these levels. Fig. 19 illustrates this trend schematically.

Packaging level	Via types	Vertical scaling, h (µm)	s (µm)	r (µm)	L (nH)	С	Operating Frequencies
PCB	PTH	1200	1000	150	0.5	2.2 μF	72 kHz -320 MHz
Package Substrate	Core via	800	75	125	0.3	0.1 μF	1.6 MHz - 530 MHz
Si-Carrier	TSV	300	100	35	0.06	0.01 μF	160 kHz - 2.6 GHz
IC	TSV	200	100	5	0.2	0.01 μF	160 kHz – 800 MHz

Table III. Typical capacitance and loop inductance of two vias by different packaging levels



Fig. 19. Equivalent circuit diagrams by different packaging levels.

Note that the connection inductances tend to get lower as we locate the decoupling capacitors nearer the source. This suggests that capacitors within the packaging structure nearer the source will be effective at higher frequencies as illustrated in Fig. 19.



The capacitance available limits the low-frequency effectiveness of the decoupling. The connection inductance limits the high frequency effectiveness. For a given target impedance, we can calculate the range of frequencies at which a given capacitor is expected to be effective,

$$\frac{1}{2\pi \left| Z_{t \arg et} \right| C} < f < \frac{Z_{t \arg et}}{2\pi L} \tag{1}$$

The operating frequencies for a target impedance of 1 ohm are in the last column of Table III. These are typical values, however in many applications, the target impedance will be different from 1 ohm and the effective frequency range of the various package levels will vary accordingly.



Fig. 20. An example of advanced packaging for high-performance computing application.

Fig. 20 illustrates an example of a package structure in a high-performance computing application. The stacking order from the bottom up is the printed circuit board, then the package substrate (organic interposer), and finally the silicon-carrier package and possibly stacked dies. The possible interconnection technologies are solder bump, flip chip bumping, through-silicon vias and copper-to-copper bonding. Multi-layer decoupling capacitors may be mounted on or in the circuit board, on or in the interposer, or between the stacked dies. Fig. 20 illustrates how the vertical scaling reduces as one moves from the bottom to the top of the geometry.





Fig. 21. Inductance loops for possible locations of the decoupling capacitors on a package.

Fig. 21 illustrates how two 1608 decoupling capacitors would typically be located on the top or the bottom of a packaging substrate. We can determine which position has the lower connection inductance by using simple analytical formulas for determining the connection inductance [24].

In the case of the top-side location, the total connection inductance is equal to the sum of the loop inductances denoted as $L2_top$, $L3_top$, L3' and $L3_source$. In the case of the bottom-side location, the total connection inductance is equal to the sum of $L2_bottom$, $L3_bottom$, L3''', L3''' and L_source . If there is no metal plane on the signal layer adjacent to the decoupling capacitor, $L2_top$ and $L3_top$ must be considered one loop instead of two separate loops. Even though the $L2_top - L3_top$ loop is not rectangular, a good estimate of the inductance can be obtained by approximating the loop as a rectangle with an equivalent area.

Location	Total inductance (nH)	L2_top (bottom) (nH)	L3_top (bottom) (nH)	<i>L</i> 3' (nH)	<i>L</i> 3'' (nH)	<i>L</i> 3''' (nH)
On the Top side	0.12	0.1	0.01	0.01	-	-
Bottom side	0.43	0.1	0.01	0.01	0.01	0.30

Table IV. Inductance calculation of the illustrated packaging structure (l > 5h, h << a, w >> h)

In the top-mounted case, the total connection inductance $(L2_top + L3')$ is about 0.12 nH compared to 0.43 nH $(L2_bottom + L3'' + L3''')$ on the bottom. In this case, the decoupling capacitor located on the top side has a lower connection inductance than the capacitor on the bottom



side. The difference is primarily due to the inductance associated with the loop area between the inner planes, L3'''.

Power bus decoupling inductance for high performance packaging in computing applications is decided primarily by the loop area formed by the current path from the switching device to the decoupling capacitor and to a lesser extent by the effective radius of the connecting conductors. The spacing between the power and ground layers in the packaging substrate, the height of through-silicon vias in the silicon carrier substrate and the solder ball diameter for flip-chip bumping are all key factors when calculating connection inductance. Another important factor is the horizontal distance between vias carrying current to and from the decoupling capacitor. Vias should be placed close to each other to reduce the inductance of the path.

IV. New Capacitor Configurations for Advanced Packaging

New packaging technologies for system-on-chip (SOC) and system-in-package (SIP) structures allow engineers to design faster, more tightly integrated electronic devices that require new approaches for providing adequate decoupling capacitance. Fortunately, SOC and SIP packaging technologies open the door to a wide range of new decoupling options. Each option has its own merits and presents its own set of challenges. Selecting the best decoupling option involves a cost/performance trade-off. As performance demands increase and the costs of new packaging techniques come down, we can expect to see a variety of new decoupling schemes rise in popularity. The following sections describe a few possible decoupling schemes for advanced packaging technologies.

A. Capacitive-stem capacitor

The greatest contributor to the connection inductance of capacitors mounted on printed circuit boards (PCBs) or interposers is often the loop formed by the vias that carry current between the MLCC and the printed circuit board power planes. This inductance can be minimized by adding more interconnecting vias or locating the vias as close as possible to one another, but it is still generally on the order of a nanohenry. Fig. 22 shows a capacitor design that eliminates the traditional via-loop area. This capacitor has a stem with metal rings for making the positive and negative connections to the PCB planes. The stem drops into a single large-diameter via hole drilled in the PCB. Inside the stem, the current is carried to the main body of the capacitor through low-inductance plates that are interleaved to maximize their own mutual inductance and therefore minimize the connection inductance.

<u>CVEL</u>

THE CLEMSON UNIVERSITY VEHICULAR ELECTRONICS LABORATORY



Fig. 22. Cross-sectional view of a ringed-stem capacitor mounted in PCB/package.

Fig. 23 shows the three-dimensional geometry of the ringed-stem capacitor. Possible variations of this capacitive stem design based on the ringed stem capacitor include:

- 1. A capacitor with circular horizontal rings but the rings are only metallic in 90° arcs on opposite sides.
- 2. A capacitor with a rectangular stem that has positive connection terminals on two opposing sides and negative connection terminals on the remaining two sides. This capacitor design also can be divided into two variations by plate orientation. This design and the one above facilitate easy soldering, since vertical shearing of solder cannot short the connection.
- 3. A capacitor with a coaxial stem that connects to both planes.
- 4. A capacitor with a cylindrical or rectangular stem that has no head. This capacitor could be embedded in the board and does not require space above the surface of the board.

B. Modeling of effective inductance

In order to compare the low-inductance performance of the proposed ringed-stem capacitor with that of conventional MLCC, a full-wave simulation was performed. As illustrated in Fig. 24, the test configuration consisted of a two-layer printed circuit board with an input port having a source and sink and an MLCC mounting port in the left side. The size of the MLCC is $1.0 \text{ mm} \times 0.5 \text{ mm} \times 0.5$ mm. The test board for the ringed-stem capacitor has a single large-diameter via hole drilled in the PCB for a stem with metal rings. The diameter of the drilling via hole is a_2 as illustrated in Fig. 27. The capacitor structure of the main body was simplified to a single block as described in Fig. 5, Section II.

<u>CVEL</u>



Fig. 23. 3D geometry of ringed-stem capacitor.



Fig. 24. Test configuration for effective inductance simulation.



Fig. 25 shows the equivalent circuit of a conventional MLCC and the proposed ringed-stem capacitor. The ringed-stem capacitor includes a capacitive stem that is designed to extend into a printed circuit board and make connections with two or more power distribution planes. In addition, the ringed-stem includes multiple interleaved low-inductance plates. The metal bands may extend at least partially around the outside of the capacitive-stem. In the equivalent circuit, the stem is represented as a capacitance C_2 , in parallel with capacitor C_1 .



Fig. 25. Equivalent circuit of effective inductance loop: conventional MLCC (left), ringed-stem without electrode (middle), and ringed-stem (right).



Fig. 26. Test board dimensions (L×W×H).



Table V shows the effective inductance at 1 GHz derived from Q3D Extractor TM simulations. The effective inductance of a proposed ringed-stem MLCC without plates is significantly higher than that of a conventional MLCC. The effective inductance of ringed-stem MLCC is slightly higher than that of a ringed-stem MLCC without plates. This shows that the stem, designed to reduce or eliminate the traditional via-loop, contributes to the connection inductance.

As the board size increases, the effective inductance of the connection loop decreases. As the board size approaches that of case 3, the effective inductance becomes less dependent on the board size.

Test board dimension		Conventional MI CC	Ringed-stem MLCC		
$(L \times W \times H)$		Conventional MILCC	w/o plates	w/ plates	
Case 1	2.81×1.74×0.2 mm	471.1 pH (0.47 nH)	275.9 pH (0.28 nH)	232.9 pH (0.23 nH)	
Case 2	3.31×4.2×0.2 mm	432.8 pH (0.43 nH)	232.5 pH (0.23 nH)	185.3 pH (0.19 nH)	
Case 3	6.58×7.8×0.2 mm	430.3 pH (0.43 nH)	227.6 pH (0.23 nH)	175.4 pH (0.18 nH)	

Table V. Effective inductance for three test board sizes

Table VI shows the effective inductance value for two test board heights. Doubling the height, increases the effective inductance.

Height of board (stem) (H) Conventional MLCC		Conventional MI CC	Ringed-stem MLCC		
			w/o plates	w/ plates	
Case 1	0.2 mm	430.3 pH (0.43 nH)	227.6 pH (0.23 nH)	175.4 pH (0.18 nH)	
Case 2	0.4 mm	636.2 pH (0.64 nH)	399.6 pH (0.40 nH)	333.8 pH (0.33 nH)	

Table VI. Effective inductance for two test board heights $(6.58 \times 7.8 \times \text{H mm})$

Fig. 27 shows how an MLCC and a ring-stem capacitor connect to the power planes of the test board. Table VII shows the dependence of the effective inductance on the diameter of the MLCC power via. The effective inductance is lower for larger diameter vias. Additionally, the connection at the test port contributes to the effective inductance. A solid rectangular block connection to the power plane at the test port has contributes less to the inductance than the three via connection illustrated.

Table VII. Effective inductance by the diameter of via $(6.58 \times 7.8 \times 0.2 \text{ mm})$

		· · · · · · · · · · · · · · · · · · ·	
Conventional MLCC	Power via connection at test port		
Diameter of via (a1)		2 via connection	Whole connection
		5 via connection	$(0.3 \times 1.4 \text{ mm})$
Case 1	0.10 mm	430.3 pH (0.43 nH)	429.1 pH (0.43 nH)
Case 2	0.21 mm	399.2 pH (0.40 nH)	373.1 pH (0.37 nH)
Case 3	0.42 mm	179.4 pH (0.18 nH)	154.5 pH (0.15 nH)

<u>CVEL</u>

THE CLEMSON UNIVERSITY VEHICULAR ELECTRONICS LABORATORY



Fig. 27. Via connection of conventional MLCC (top) and test port (bottom)

Table VIII shows how the diameter of the stem of the proposed ringed-stem capacitor affects the effective inductance. As the diameter of the stem increased, the effective partial inductance of the ringed-stem capacitor decreased. The ringed-stem capacitor with electrodes (plates) in the stem has less inductance than the capacitor without electrodes.

Ringe M	ed-stem LCC	Power via connection at test port						
Diamet	er of stem	3 via co	3 via connection Whole connection					
(a_2)		w/o plates	w/ plates	w/o plates	w/ plates			
Case 1	0.21 mm	0.28 nH	0.21 nH	0.25 nH	0.18 nH			
Case 2	0.42 mm	0.22 nH	0.18 nH	0.18 nH 0.20 nH 0.15 nH				

Table VIII. Effective inductance for two stems diameters (6.58×7.8×0.2 mm)

The simulation results from Table V to VIII show how the connection's effective inductance is dependent on each segment forming the current loop. The wider and shorter each segment is, the smaller the overall loop inductance will be. Additionally, this data shows that the proposed ringed-stem capacitor performs better than a capacitor connected to power planes through a traditional via connection.



Fig. 28. Via connection of ringed-stem capacitor (top) and test port (bottom)



Fig. 29. Evaluation configuration and equivalent circuit model for insertion loss.



C. Transfer function analysis of proposed capacitors

The purpose of decoupling capacitors is to stabilize the voltage on the power bus. The magnitude of the transfer function between two ports at different locations on the planes is an indication of how well the decoupling is performing. Lower values indicate better performance. The $|S_{21}|$ for a standard MLCC and ringed-stem MLCC as illustrated in Fig. 25 was calculated using the model in Fig. 29 and the full-wave simulation tool, HFSSTM. In an equivalent circuit for this configuration, the stem of ringed-stem MLCC is represented as a smaller capacitor in parallel with the larger capacitance of the MLCC.

Fig. 30 shows the simulation results for three types of MLCC: a conventional MLCC, a ringedstem MLCC without plates and a normal ringed-stem MLCC. The equivalent circuit of the stem, as shown in Fig. 30, is represented as a series R-L-C circuit in parallel with the circuit representing the MLCC. Due to the lower overall mutual inductance, the resonance frequency of the ringed-stem capacitor is at a higher frequency than that of the conventional MLCC. At frequencies above the self-resonance of both capacitors, the insertion loss of the ringed-stem MLCC is 10 dB higher than that of the conventional MLCC. Above the frequency where the stem plate resonates, the performance of the ringed-stem MLCC with plates in the stem is 2–3 dB better than that of the ringed-stem MLCC without electrodes.



Fig. 30. Full-wave simulation responses for the proposed capacitors.



V. Conclusion

Power bus decoupling inductance for high performance packaging in computing applications is dependent on the size of the conductors forming the current path from the switching device to the decoupling capacitor and the overall loop area. Advanced packaging geometries employing stacked silicon wafers, through-silicon vias, new organic and ceramic substrates, micro-bumps and other unique structures provide unique opportunities for implementing novel low-inductance decoupling schemes employing multilayer ceramic capacitors (MLCCs). Section II of this report discussed the effect of plate orientation in MLCCs and concluded that plate orientation does not have a significant effect on the connection inductance of an MLCC of given dimensions. Section III outlined the relative significance of die-level, package-level and board-level decoupling. This section showed that higher frequency decoupling is easier to achieve close to the die level, while lower frequency decoupling is easier to achieve further from the die.

Section IV describes "ringed-stem" capacitors that reduce connection inductance by moving some of the capacitance between the planes of a power distribution bus. The improvement in connection inductance was demonstrated using 2-D and 3-D simulations.

References

- [1] Steve Weir, "Bypass capacitor inductance, data sheet simplicity to practical reality," TeraspeedConsulting Group LLC.
- [2] Steve Weir, "Impact of PCB stack-up and capacitor via design in power distribution design," presentation to the Santa Clara Valley chapter of the *IEEE EMC Society*, Feb. 2006.
- [3] "PCB power supply noise tackled," Nikkei Electronics, Sep. 2003
- [4] Hocheol Kwak, H. Ke, B. Lee, and T. Hubing, "Plate orientation effect on the inductance of multi-layer ceramic capacitors," *Proc. of the 16th Topical Meeting on Electrical Performance* of Electronic Packaging, Atlanta, Georgia, Oct. 2007, pp. 95-98.
- [5] John U. Knickerbocker, Chirag S. Patel, "Three dimensional silicon integration using fine pitch interconnection, silicon processing and silicon carrier packaging technology," *IEEE 2005 Custom Integrated Circuits Conference*, Sep. 2005, pp. 659-662.
- [6] Philip Pieters, Eric Beyne, "3D wafer level packaging approach towards cost effective low loss high density 3D stacking," *7th International Conference on Electronics Packaging Technology*, Aug. 2006, pp. 1-4.
- [7] Todd Hubing, "Effective strategies for choosing and locating printed circuit board decoupling capacitors," *Proceedings of the 2005 IEEE International Symposium on EMC*, vol. 2, pp. 632–637, Aug. 2005.
- [8] Hocheol Kwak, H. Ke, B. Lee, and T. Hubing, "Inductance calculations for advanced packaging in high-performance computing," *IEEE International Symposium on EMC*, Detroit, MI, Aug. 2008.



- [9] T. M. Zeeff, T. H. Hubing, T. P. Van Doren, and D. Pommerenke, "Analysis of simple twocapacitor low-pass filters," *IEEE Trans. Electromagn.Compat.*, vol. 45, no. 4, pp. 595–601, Nov. 2003.
- [10] Theodore M. Zeeff, Andrew Ritter, Todd H. Hubing, and Thomas Van Doren, "Analysis of a Low-Pass Filter Employing a 4-Pin Capacitor," *IEEE Trans. Electromagn. Compatibility*, vol. 47, no. 1, pp. 202–205, Nov. 2005.
- [11] T. Hubing, Hocheol Kwak and H. Ke, "Capacitive-Stemmed Capacitor," U.S. Patent 61/143581, Jan. 9, 2009.
- [12] B. H. Lee, M. C. Park, Hocheol Kwak, H. Ke and T. Hubing, "Semiconductor integrated circuit chip, multilayer chip capacitor and semiconductor integrated circuit chip package," U.S. Patent, No. 069576-0440, Nov. 13, 2008/P10-2009-0055615, Jun. 22, 2009, Korea.
- [13] Hocheol Kwak, T. Hubing, "New capacitor configurations for advanced packaging," CVEL-08-005, Jan. 2008.
- [14] Hocheol Kwak, T. Hubing, "An overview of new semiconductor packaging technologies and trends," CVEL-07-001, Mar. 2007.
- [15] Andrew P. Ritter and Roberto N. Garrafa, "Low inductance land-grid array decoupling capacitors," *IMAP*, 2006.
- [16] J.U. Knickerbocker, P.S. Andry, "Development of next generation system-on-package (SOP) technology based on silicon carriers with fine-pitch chip interconnection," *IBM Journal Res. & Dev.* vol.49, no. 4, Jul. 2005.
- [17] Larry E. Mosley, "Capacitor impedance needs for future microprocessors," *CARTS USA*, pp. 193-203, Apr. 2006.
- [18] Tadahiro Kuroda, "System LSI: Challenges and opportunities," *IEICE Transactions Electron.*, vol. E89-C, no.3, Mar. 2006.
- [19] Knighten, J., B. Archambeault, J. Fan, G. Selli, L. Xue, S. Connor, J. Drewniak, "PDN design strategies: II. Ceramic SMT decoupling capacitors – Does location matter?" *IEEE EMC Society Newsletter*, Issue No. 208, Winter 2006, pp. 56-67.
- [20] Sudhaker Bobba, Tyler Thorp, "IC power distribution challenges", *IEEE/ACM International Conference on Computer Aided Design*, pp. 643–650, Nov. 2001.
- [21] Jun Fan, Member, James L. Drewniak, James L. Knighten, Norman W. Smith, Antonio Orlandi, Thomas P. Van Doren, Todd H. Hubing, and Richard E. DuBroff, "Quantifying SMT decoupling capacitor placement in DC power-bus design for multi-layer PCBs", *IEEE Trans.* on Electromagn. Compat., vol. 43, no. 4, pp. 588-599, Nov. 2001.
- [22] Chen Wang, Jingkun Mao, G. Selli, Shaofeng Luan, Lin Zhang, Jun Fan, D. Pommerenke, R. E. DuBroff, J. L. Drewniak, "An efficient approach for power delivery network design with closed-form expressions for parasitic interconnect inductance," *IEEE Trans. on Adv. Packag.*, vol. 29, no.2, pp. 320-334, May 2006.



- [23] Todd H. Hubing, T.P Van Doren and J. L. Drewniak, "Identifying and quantifying printed circuit board inductance," *Proc. of the 1994 IEEE International Symposium on EMC*, pp. 205-208, Aug. 1994.
- [24] T. Zeeff, "Estimating the connection inductance of a decoupling capacitor," *UMR EMC Laboratory Technical Report*, TR01-1-030, University of Missouri-Rolla, Jun. 2001.
- [25] Richard K. Ulrich, Advanced Electronic Packaging, Second Edition, John Wiley & Sons, 2006.
- [26] Rao R. Tummala, Fundamentals of Microsystems Packaging, McGraw-Hill, 2001.
- [27] H. B. Bakoglu, Circuits, Interconnections, and Packaging for VLSI, Addison-Wesley, 1990.
- [28] E. E. Davidson, "Electrical design of a high speed computer packaging system," *IEEE Trans.* on Computers, Hybrids and Manufacturing Technology, vol. 6, no. 3, Sep. 1983.
- [29] Istvan Novak, "A black-box frequency dependent model of capacitors for frequency domain simulations," *DesignCon East*, 2005.
- [30] Istvan Novak, "Inductance of bypass capacitors: How to define, how to measure, how to simulate," *DesignCon East*, 2005.
- [31] Andrew P. Ritter, "Low inductance land grid array decoupling capacitors," IMAPS, 2006.
- [32] Clayton R. Paul, "Effectiveness of multiple decoupling capacitors," *IEEE Trans. on Electromag. Compat.*, vol. 34, no. 2, May 1992.
- [33] Steve Weir, "Bypass filter design considerations for modern digital systems, a comparative evaluation of the big "V", multi-pole, and many pole bypass strategies," *DesignCon East*, 2005.
- [34] Aicha Elshabini, Gangqiang Wang, "Future trends in electronic packaging," SPIE, 2006.
- [35] "Advanced technologies for high performance systems", *Intel Technology Journal*, 2005, Available at: http://developer.intel.com/technology/itj/index.htm.