CVEL

THE CLEMSON UNIVERSITY VEHICULAR ELECTRONICS LABORATORY

# TECHNICAL REPORT: CVEL-11-029

# EMI Source Modeling of the John Deere CA6 Motor Driver

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# Executive Summary

This report provides a summary of the primary results obtained from the Balanced Power Inverter Project at Clemson University, which is funded by John Deere's participation in the National Science Foundation Industry/University Cooperative Research Center for Electromagnetic Compatibility. Specific results that are of particular significance include:

1. The development and simulation of basic source models for the CA6 inverter including values for significant parasitic parameters.
    a. SVPWM driving scheme requires isolation of DC link from frame ground to prevent common-mode currents from returning on the frame.
    b. Passive balancing should be effective at frequencies above a few MHz.
    c. Active balancing simulations suggest that this could be an effective low-cost solution for kHz – MHz frequencies.
    d. Moving heatsink from the drain to the source of the high-side MOSFETs is another possible solution.
2. The evaluation of a low-cost passive balancing network for reducing EMI due to common-mode emissions at frequencies above a few megahertz as implemented in the CA6 power inverter.
    a. The basic concept for this network was described in a previous report [1].
    b. Initial results indicate a reduction on the order of 5 dB for peak frequencies, but this is expected to improve with optimization of network design.
    c. Equation for selecting component values – (Page 24).
    d. Equation for calculating power dissipated in balancing network – (Page 25).
    e. Guidance for selecting component types – (Pages 24 - 25).
3. The modeling and simulation of the 60-MHz ringing on the phase voltage observed in the CA6 inverter.
    a. Measurements and simulations indicate the resonance is within the MOSFET and involves the reverse recovery (body) diode.
    b. Overall impact on common-mode emissions from the CA6 inverter appears to be minor, but this will be investigated further.

The report also summarizes the status of the project as of October 1, 2011 and outlines the future directions of this research.

# 1. Introduction

This report provides a summary of the primary results obtained from the Balanced Power Inverter Project at Clemson University, which is funded by John Deere's participation in the National Science Foundation Industry/University Cooperative Research Center for Electromagnetic Compatibility. The primary goal of this project is to provide a cost sensitive (i.e. without ferrites) production solution to reduce conducted and radiated electromagnetic emissions to levels that will allow Class A and Class B inverters to pass EN14982 / CISPR12.

The Clemson investigators have identified the primary source of these emissions as the conversion of differential motor-drive voltages to common-mode currents returning on the frame ground of the vehicle. They have proposed to eliminate these currents by making the motor drivers electrically balanced. Three methods for accomplishing this have been proposed and are being evaluated:

1. To reduce radiated emissions at frequencies above 30 MHz, a passive balancing network is proposed that will make an unbalanced driver appear to be balanced at high frequencies.
2. To reduce conducted emissions at frequencies below 30 MHz, an active balancing circuit is proposed that drives the frame ground relative to the DC link ground with a voltage that compensates for the known imbalances in the motor driver.
3. To reduce common-mode emissions at all frequencies, a balanced heatsink structure where the heatsink is capacitively coupled to the phase side of both the high-side and low-side MOSFETs is proposed.

This report describes each of these methods as defined and implemented to date. Section 2 describes the CA6 inverter provided by John Deere and how it is modeled as an EMI source. This section also explains the origin of the 60-MHz ringing observed in the phase voltage waveforms. Section 3 describes and evaluates the passive balancing network built into the CA6 inverter. Section 4 summarizes the results of this project to date and discusses the next steps in this research.

Two additional technical reports [1, 2] resulting from this project were published in the spring of 2011. A companion technical report [3] discussing the relationship between damped oscillations in the time domain and the bandwidth of resonances in the frequency domain is being published with the same date as this report.

# 2. CA6 Inverter Source Modeling

The subject of the modeling and measurements in this report is a prototype CA6 inverter provided by John Deere. The CA6 inverter is a 48-volt, 3-phase motor driver employing 20 kHz space vector pulse width modulation (SVPWM).

## 2.1 CA6 Working States

The MOSFET switching pattern in a normally functioning CA6 inverter results in a continuously rotating space vector. However to aid in the modeling and analysis, the inverter provided by John Deere is programmed to operate in selected, non-varying states. The MOSFET switching patterns correspond to fixed vector angles ('a' in Fig. 2-1) in the space vector complex plane. The vector length, which corresponds to the steady state output current, can be adjusted. The choice of states and adjustment of the phase output current is achieved by switches on the control box shown in Fig. 2-2.

Switches A, B and C in Fig. 2-2 are used to select the inverter state. The six operational combinations the three switch positions and their corresponding states are listed in Table 2-1. Note that in all six states, one of the three phases has no DC current flowing in it. Switch D adjusts the net DC

current flowing in the other two phases by increasing the time between phase switching events, which has the effect of increasing the vector length in Fig. 2-1. All measurements and analyses in this report were made in one of the six states listed in Table 2-1 with a particular phase current set.

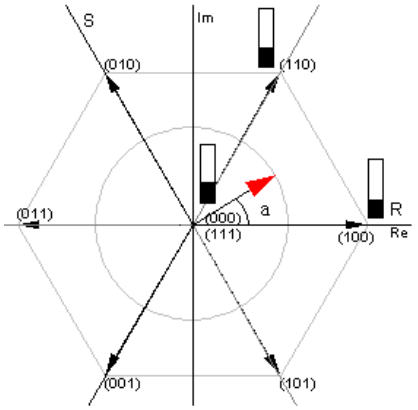
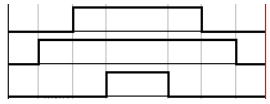
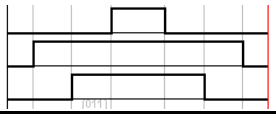
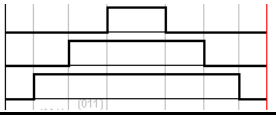
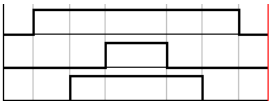



Fig. 2-1. Space vector diagram.


Fig. 2-2 Control box switches.

Table 2-1. Inverter working states.

| State | Switches | | | Phases Current * | | | Space vector angle 'a' | MOSFETs switching * |
|---|---|---|---|---|---|---|---|---|
| | C | B | A | A | B | C | | |
| 1 | 0 | 0 | 1 | + | ~ | - | π/6 |  |
| 2 | 0 | 1 | 0 | ~ | + | - | π/2 |  |
| 3 | 0 | 1 | 1 | - | + | ~ | 5π/6 |  |
| 4 | 1 | 0 | 0 | - | ~ | + | 7π/6 |  |
| 5 | 1 | 0 | 1 | ~ | - | + | 3π/2 |  |
| 6 | 1 | 1 | 0 | + | - | ~ | 11π/6 |  |
| * | + : Current leaving inverter<br>- : Current entering inverter | | | | | | Three pulses show the 'on' time of high side MOSFETs. Top to bottom: Phase A B C | |

## 2.2 MOSFET switching events

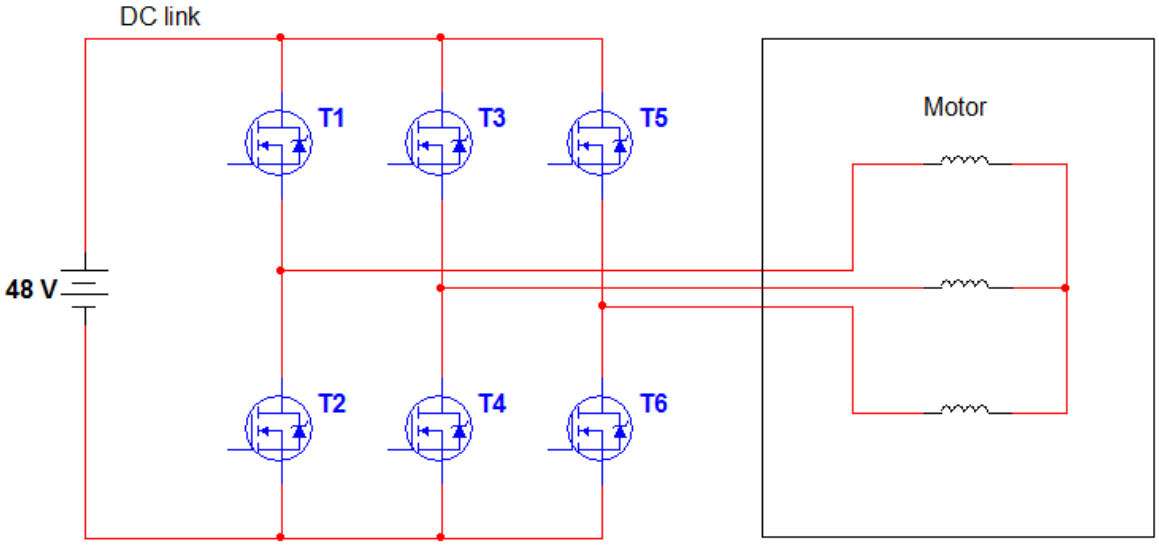



Fig. 2-3. MOSFET motor interface.

Fig. 2-3 shows a simplified representation of the switching interface between the 48-volt DC supply and the motor. Each phase wire connects to 2 MOSFETs, a high-side MOSFET (T1 T3 T5) and a low-side MOSFET (T2 T4 T6). The two MOSFETs corresponding to any one phase can't be turned on at the same time. One of them is always turned off before the other is turned on. The short period between one turning off and the other turning on is called the *dead time*. During the dead time, current flows through the body diode of the MOSFET that just opened. For example, consider State 1 (CBA 001) in Table 2-1. The three phase voltages rise and fall in the sequence shown in Fig. 2-4.

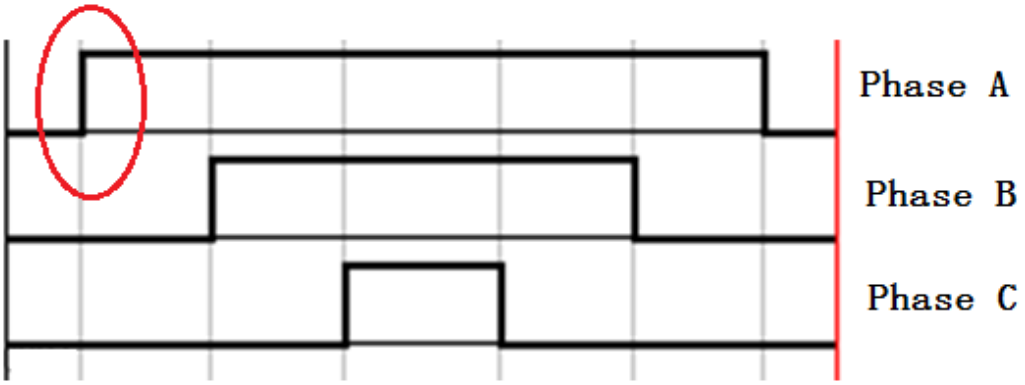



Fig. 2-4. Phase voltages rising sequence.

The measured Phase A voltage (relative to the 0-volt supply rail) is shown in Fig. 2-5. The red and cyan curves show the low-side and high-side MOSFET gate voltages, respectively. After the low-side MOSFET starts to turn off, there is a 200 ns delay before the high-side MOSFET turns on. During that time, current flows through the low-side MOSFET's body diode due to the motor inductance. As a result, the Phase A voltage drops to approximately -1 volt as indicated in Fig. 2-6. Note that once the high-side MOSFET turns on, the Phase A voltage rises from 0 to 50 V in less than 30 ns. This high dv/dt is the main source of the common mode current on the 3 phase wires.

Fig. 2-5 exhibits a 60-MHz ringing associated with the rising voltage waveform. A similar ringing is also observed during the falling voltage. The cause and effect of this ringing is described in Section 2.5 of this report.

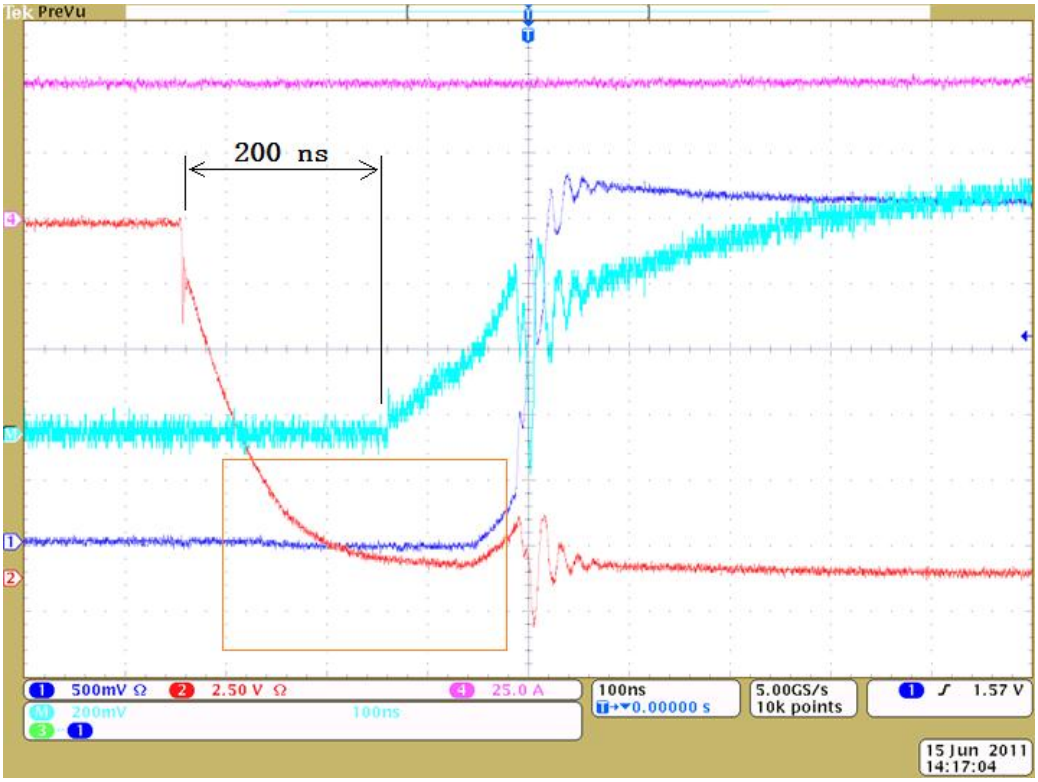



Fig. 2-5. Phase A rising event.

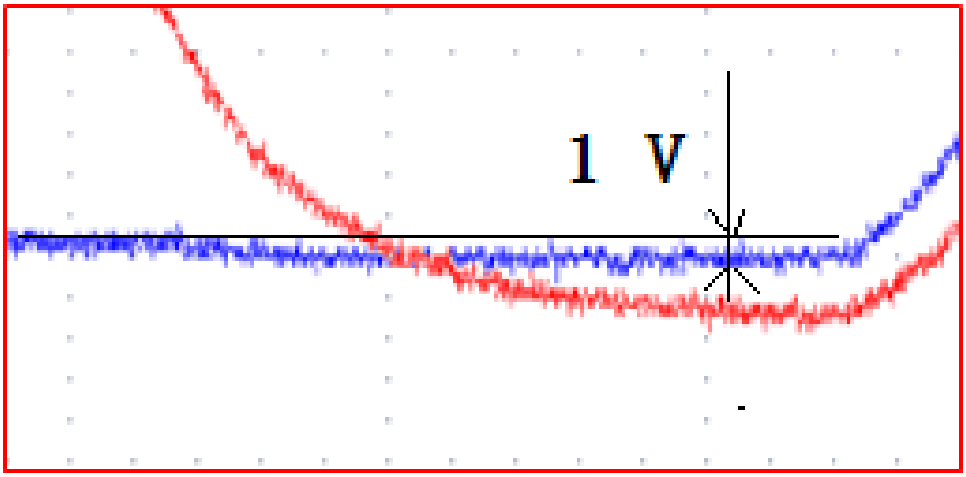



Fig. 2-6. Voltage while MOSFET body diode is conducting.

## 2.3 Common mode current due to high dv/dt

*Test setup*

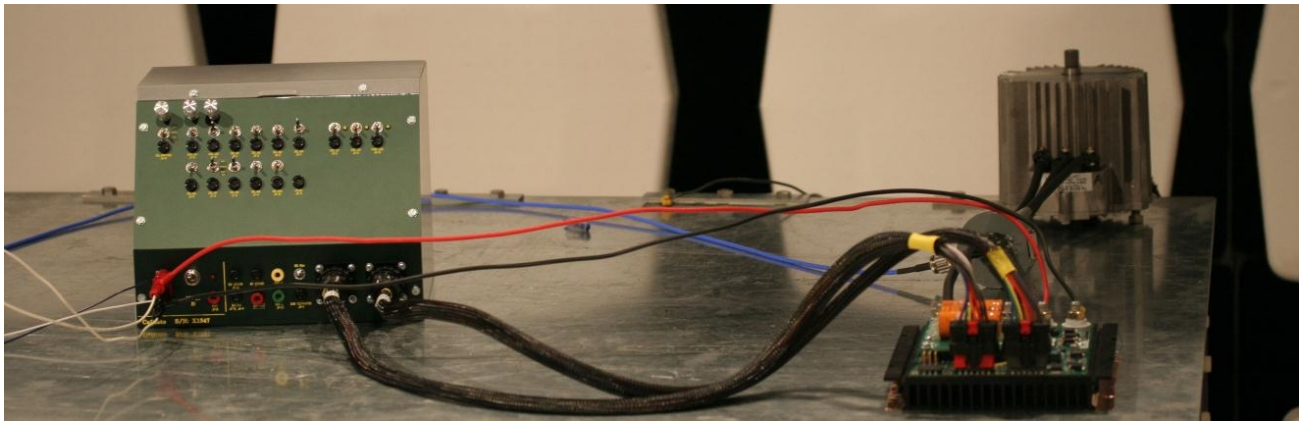


Fig. 2-7 Test setup

In this section, measurements and analyses are based on a test setup similar to the one shown in Fig. 2-7. The metal case of the motor is screwed to the table's metal surface. The anodized coating on the bottom of the inverter case is sanded off and the case is connected to the metal table top with copper tape. The three phase wires (not seen in the figure) are stretched horizontally about 7 cm above the surface of the table. The controller box and wires between the controller box and inverter are not fixed on the table. Measurements show that their position does not significantly affect the CM current on the 3 phase wires.

*Coupling path*

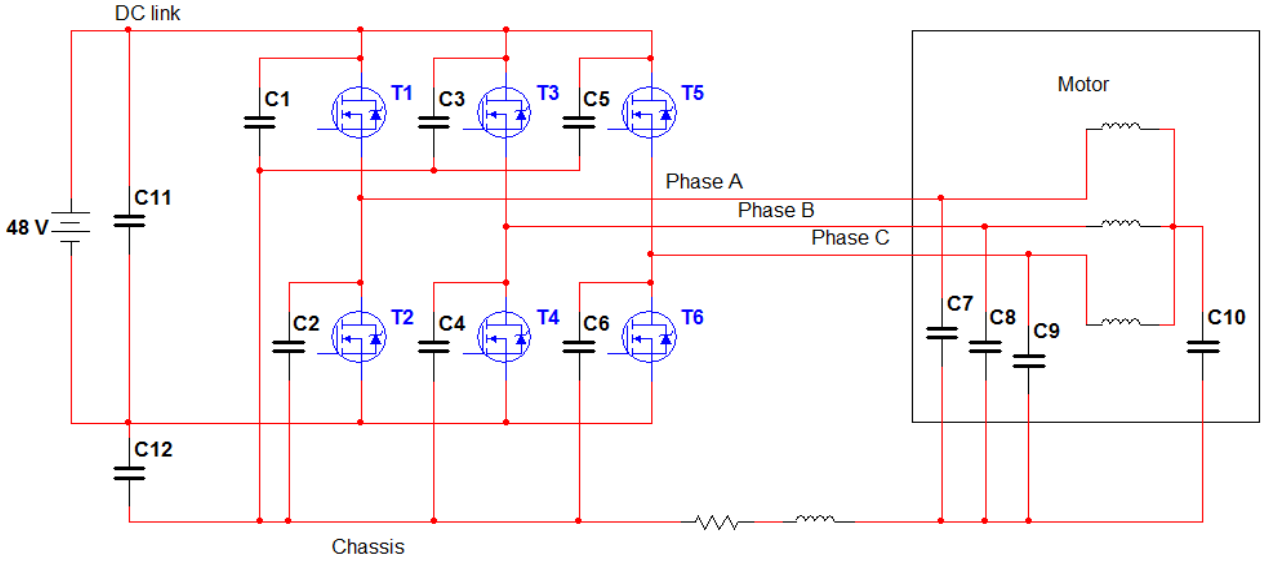



Fig. 2-8. Parasitic capacitance model.

Fig. 2-8 shows a simple equivalent circuit representation of this test set-up. C1 to C6 are the parasitic capacitances from the MOSFET drains to the heatsink/chassis. C7 to C10 are parasitic capacitances from motor windings to the chassis. C11 is the DC decoupling capacitor. The capacitances from the phase wires to the chassis are relatively small compared to C1 to C10 and are not included in the model.

Taking the CBA 001 state T1 turning on event for example; T2, T3, T5 are open, T4 and T6 are considered shorted. If the DC source impedance is high (i.e. a constant current source) and we ignore C11, the current route due to dv/dt at Phase A to DC 0-volts can be simplified to the circuit in Fig. 2-9.

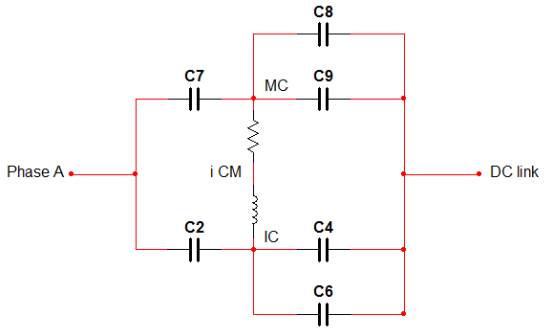



Fig. 2-9. dv/dt current route w/o C11.

Point MC and Point IC represent motor chassis and inverter chassis respectively. The current flowing between MC and IC is equal to the common-mode current on the 3 phase wires. From Fig. 2-9, it is clear that current only takes the MC-IC route when there is a potential difference between MC and IC. If C7=C8=C9 and C2=C4=C6, MC and IC will have same potential, so the dv/dt will not produce a common-mode current on the phase wires. On the other hand, dv/dt at the phase side and electrical imbalance at either the motor or the inverter will generate common mode current on the phase wires.

## *Decoupling capacitor effect*

If the source impedance is low and C11 is taken into consideration, Fig. 2-9 should be modified as shown in Fig. 2-10.

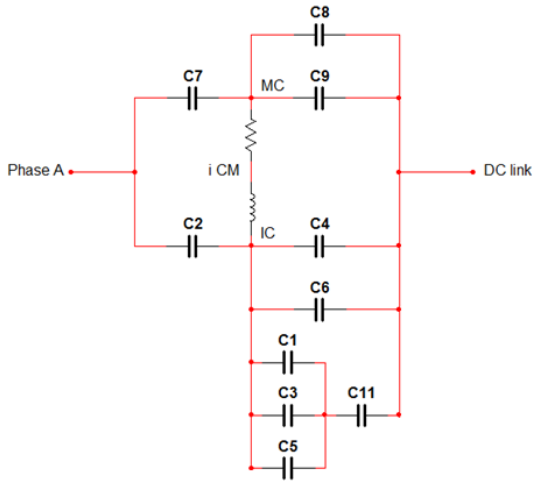



Fig. 2-10. dv/dt current route w/ C11.

C11 is much larger than the parasitic capacitances and can be viewed as being shorted at high frequencies. Now, even if C7=C8=C9 and C2=C4=C6, the potential at MC and IC will be different resulting in common-mode current. Even if we set C2=1/2(C1+C3+…+C6), the common-mode current would only be eliminated for this particular state. In other states, the balance would be lost, so it is not possible to completely balance a 3-phase inverter with a low-impedance DC source by passively matching parasitic impedances. Practical solutions to this problem are discussed in Section 3.3.

*CA6 inverter parasitic capacitance estimation*

A more complete model of the power inverter switching circuitry in the CA6 inverter (Fig. 2-11) includes the drain to source capacitances of the MOSFETs and the parasitic capacitance between MOSFET source and chassis. These values are approximately 10.5 nF and 0.2 nF respectively. The source-to-chassis capacitance is approximately 1.5 nF. The 4.5 nF represents the three 1.5 nF drain-to-chassis capacitances of T1, T3 and T5. The 0.6 nF represents the 3 source-to-chassis capacitances of T2, T4 and T6. The 1.7 nF represents the parallel combination of the 1.5 nF and 0.2 nF. The 10.5 nF capacitances don't affect the above analyses since they exist only between phase and DC.

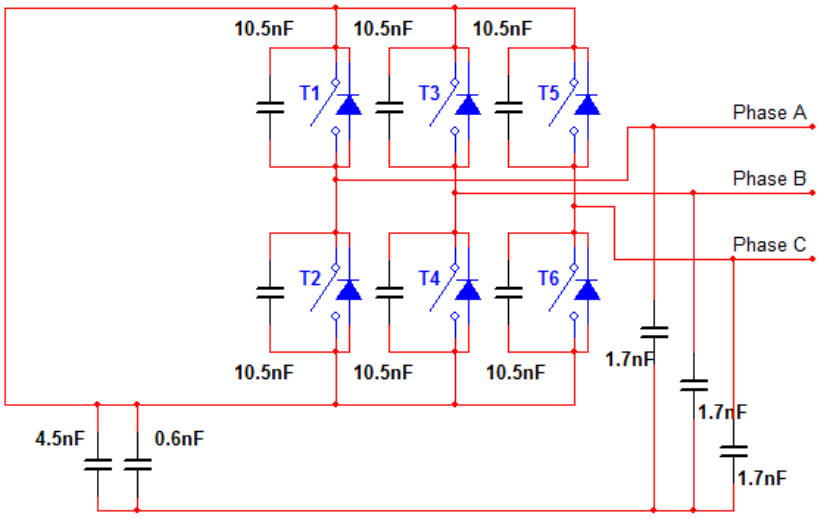



Fig. 2-11. CA6 Parasitic capacitance estimation.

## 2.4 CA6 common mode current time domain measurement

Time-domain measurements were made of the common-mode current flowing on the three phase wires using a Tektronix MSO 4104 oscilloscope. Phase voltages were monitored using a customized voltage probe consisting of a 1-kΩ resistor in series with the center conductor of a 50-Ω coaxial cable as shown in Fig. 2-12. The resistor prevents the 50-Ω input of the scope from overloading the circuit while significantly increasing the bandwidth of the measurement. The 1-kΩ resistor forms a voltage divider with the 50-Ω input of the scope, so the actual voltages are 21 times the measured values. The common-mode current was measured with a Fischer Custom Communications F-33-1 current probe around all three phase wires. This probe has a usable frequency range from 10 kHz – 250 MHz.

Fig. 2-12. Customized voltage probe.

The measured results for the inverter in the CBA 100 state are plotted in Figs. 2-13 and 2-14. The blue curves are the Phase A voltages. The cyan curves are the Phase B voltages. The purple curves are the Phase C voltages. The measured common-mode current is indicated by the green curves, while the red curve in Fig. 2-14 shows the FFT of the common-mode current.

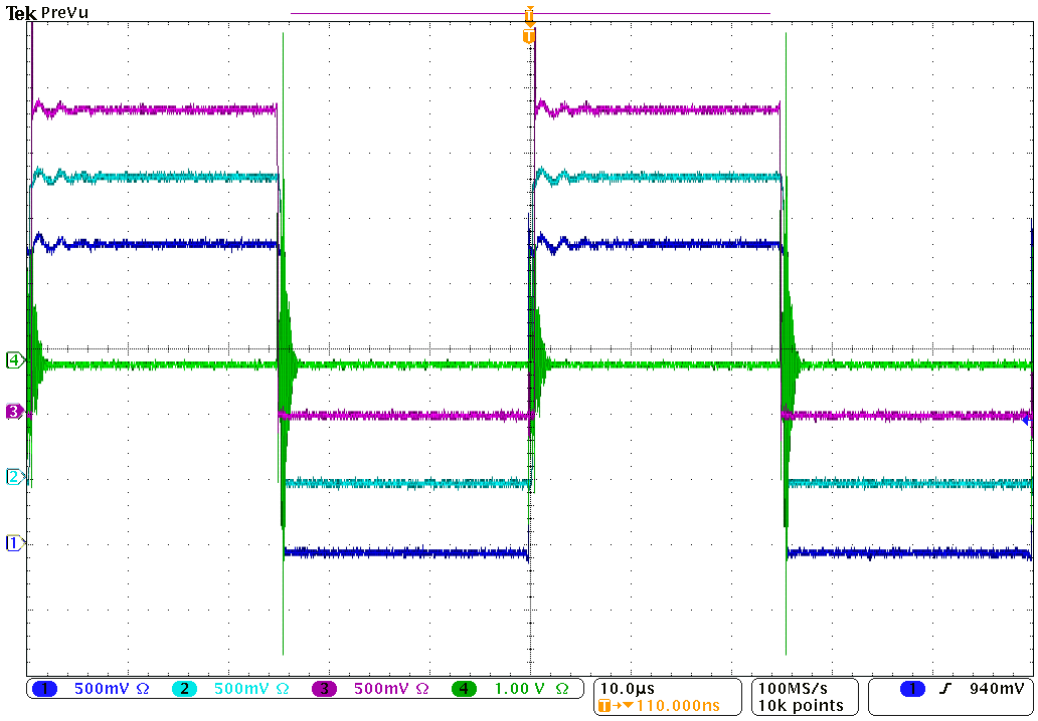



Fig. 2-13. Common mode current in time domain.

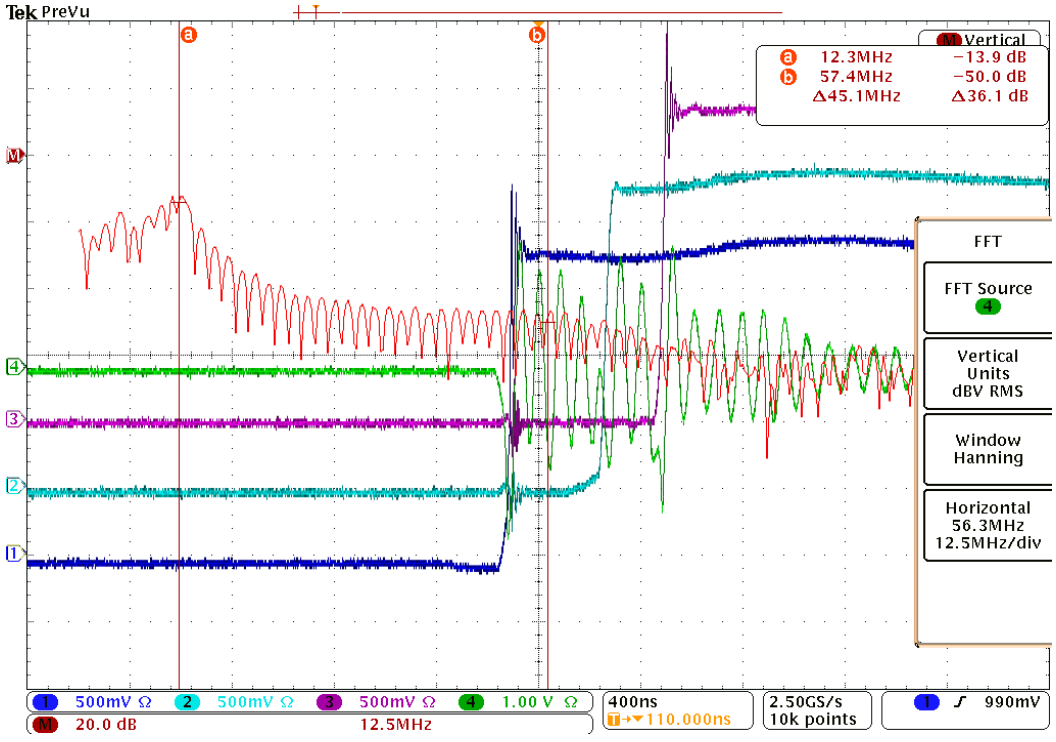



Fig. 2-14. Common mode current in time domain zoomed in with FFT.

As shown in Fig. 2-14, the common-mode current spikes during each switching event and rings at a frequency of approximately 12 MHz. 12 MHz corresponds to the resonance of the common-mode current path through the phase wires and motor and returning on the ground plane. To demonstrate this, another measurement was made with longer phase wires. Fig. 2-15 shows a test setup with 1.3-meter phase wires (instead of the original 0.5-meter wires). As indicated in Fig. 2-16, the ringing frequency of the common-mode current shifts from 12 MHz to 7 MHz. Since the wire-chassis loop inductance is approximately proportional to the wire length, we would expect a 260% increase in the wire length to reduce the resonant frequency to 60% of its original value as observed.

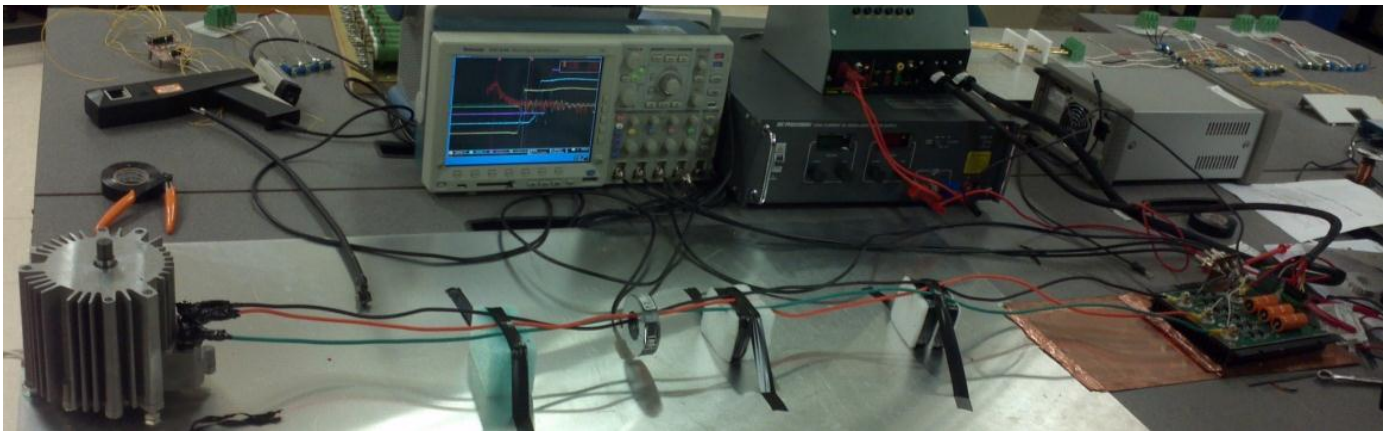


Fig. 12-15. Test setup for extended phase wires.

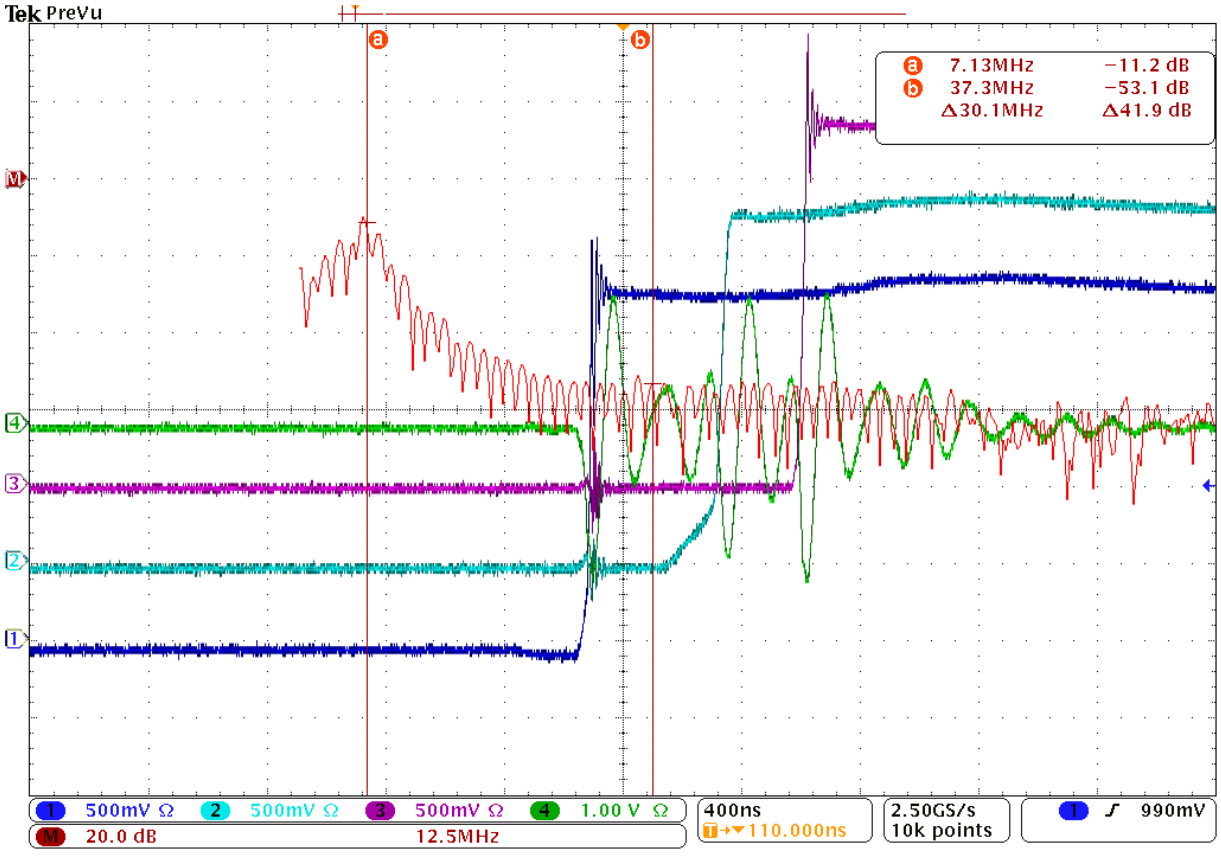



Fig. 2-16. Common mode current in time domain with extended phase wires.

## 2.5 Investigation of the 60 MHz ringing

The 60 MHz ringing in the measured phase voltages was consistently observed under a variety of measurement conditions. The ringing frequency was independent of the phase wire length or load, but the magnitude of the ringing in any particular phase wire was clearly correlated with the magnitude of the current in that phase wire. Fig. 2-17 and Fig. 2-18 show the measured voltages on Phase A (Blue) when the phase current (Pink) is 25 Amps and 75 Amps, respectively. For these measurements, the inverter was in the CBA 100 state. The voltages were measured using the customized 1-kΩ probes described previously. The current was measured using a Tektronix TPO 150 current probe (DC – 20 MHz bandwidth).

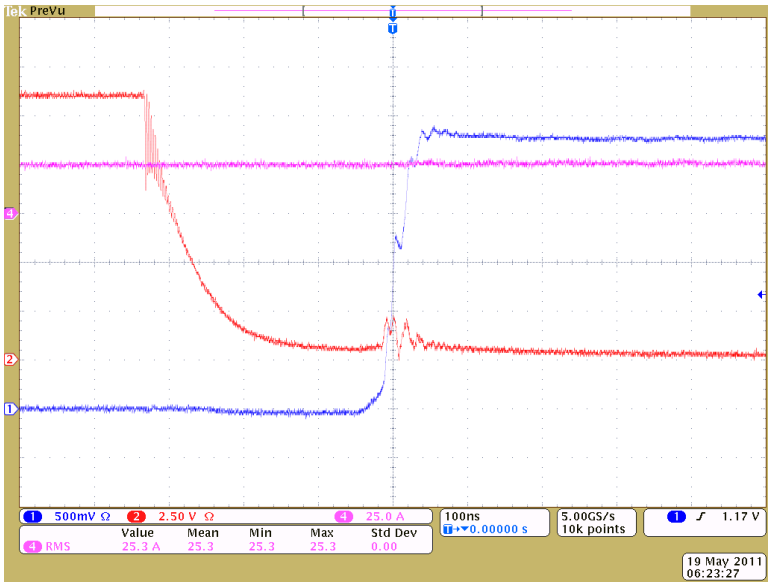



Fig. 2-17. Ringing on Phase A with 25-A current.

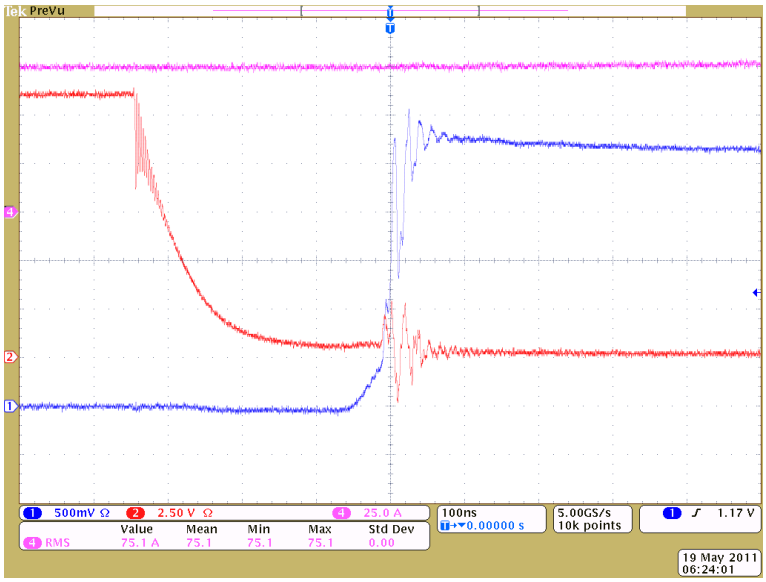



Fig. 22-18. Ringing on Phase A with 75-A current.

## *Investigation of the phase wires and motor*

The test above was repeated with the extended length phase wires and no shift in the ringing frequency was observed indicating that the inductance associated with these wires was not a factor in this ringing. The motor was replaced with the resistive load shown in Fig. 2-19 and no shift in the ringing frequency was observed.

Fig. 2-19. Resistive load used to replace the motor.

## *Investigation of MOSFET gate voltages*

In Fig. 2-5, the 60 MHz ringing is also observed on both high-side and low-side MOSFET gate voltages. However, when there is little current flowing through the phase, the ringing in the gate voltages disappears. It is likely that the observed ringing on the gate voltages is noise coupled from the ringing on phase voltages. In Fig. 2-5, it is clear that the gate voltage does not start to ring until the drain-source current is turned on.

## *Investigation of low-side MOSFET body diode*

The fact that the ringing is not affected by the phase wires or the motor suggests that an RLC loop on the inverter board is the source. A resonance at 60 MHz would be consistent with a capacitance on the order of nanofarads ringing with a loop inductance on the order of nanohenries. Also, from the shape of the time-domain waveform (i.e. counting the number of observable oscillations), the approximate Q-factor associated with this resonance is about 5. Thus the loop's resistance is estimated to be on the order of 10 to 100 milliohms. These parameters suggest the possibility that the ringing occurs within the MOSFET package and/or its low-inductance connection to the power bus.

## *Verification*

The following tests were done see if the MOSFET drain-to-source capacitance might be the capacitance involved in the 60-MHz ringing described above. A 1-μF SMD capacitor was added in parallel with the drain-source pins of the Phase A low-side MOSFET (Fig. 2-20). Comparing the ringing in the measured phase voltage without the capacitor (Fig. 2-21) to the ringing in the measured phase voltage with the capacitor (Fig. 2-22), it is observed that the ringing frequency shifts from 60 MHz to 4 MHz. According to the datasheet (see Fig. 2-24), the IPB039N10N3 power MOSFET has approximately 1 to 6 nF of drain-to-source capacitance for drain-to-source voltages of 0 – 50 volts. Therefore, adding 1 μF should shift the resonance frequency of the RLC circuit by a factor of about 14. This agrees with the measurement shown in Fig. 2-22 very well.

Fig. 2-23 shows a similar result obtained with a 0.1 µF SMD capacitor. The ringing frequency with this capacitor in place is about 10 MHz. This is again very close to the expected shift.

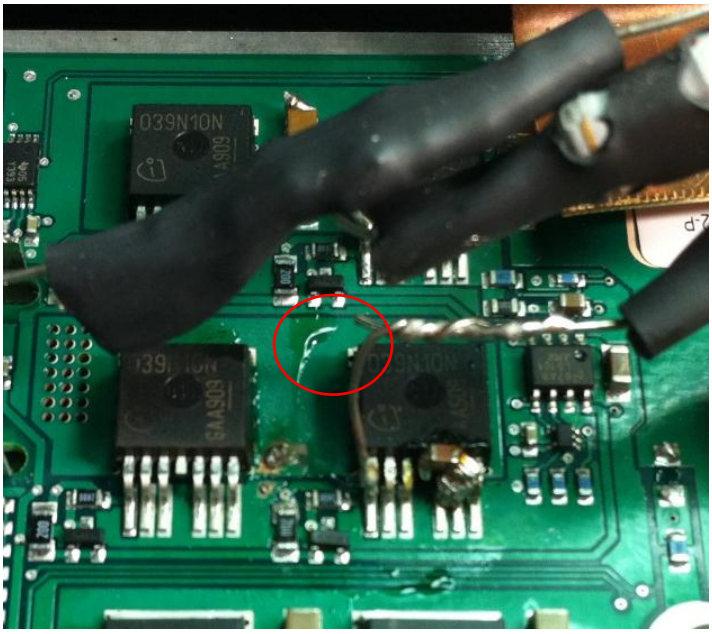



Fig. 2-20. SMD Capacitor added to MOSFET.

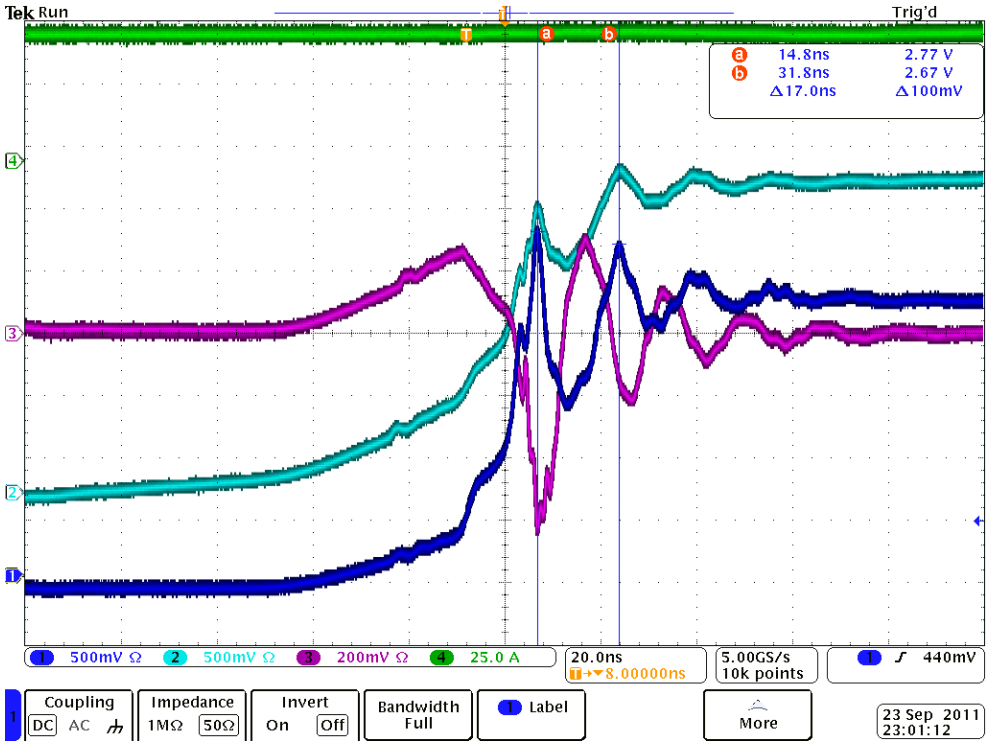



Fig. 2-21. Ringing frequency without add-on capacitor.

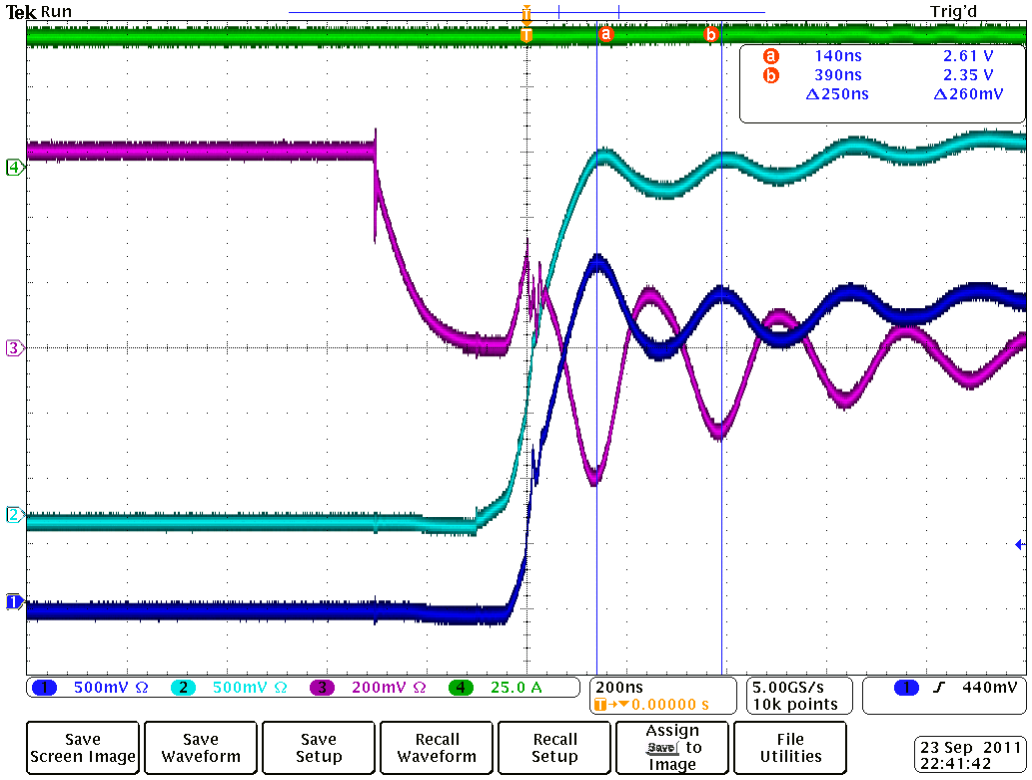



Fig. 2-22. Ringing frequency shifted on Phase A with SMD 1uF capacitor.

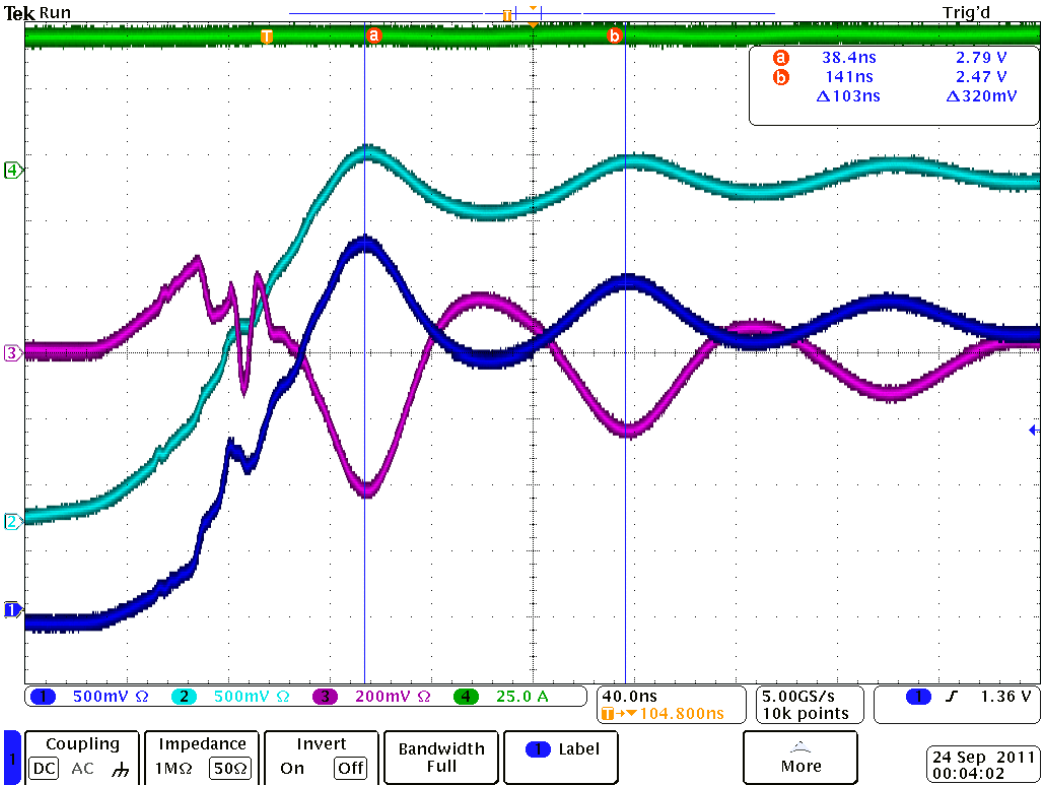



Fig. 3-23. Ringing frequency shifted on Phase A with SMD 0.1uF capacitor.

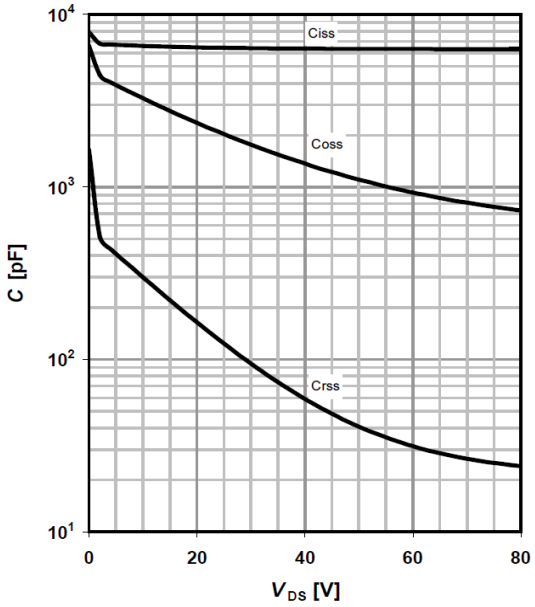



Fig. 2-24. Typical capacitances of IPB039N10N3 (From datasheet).

*SPICE simulation.*

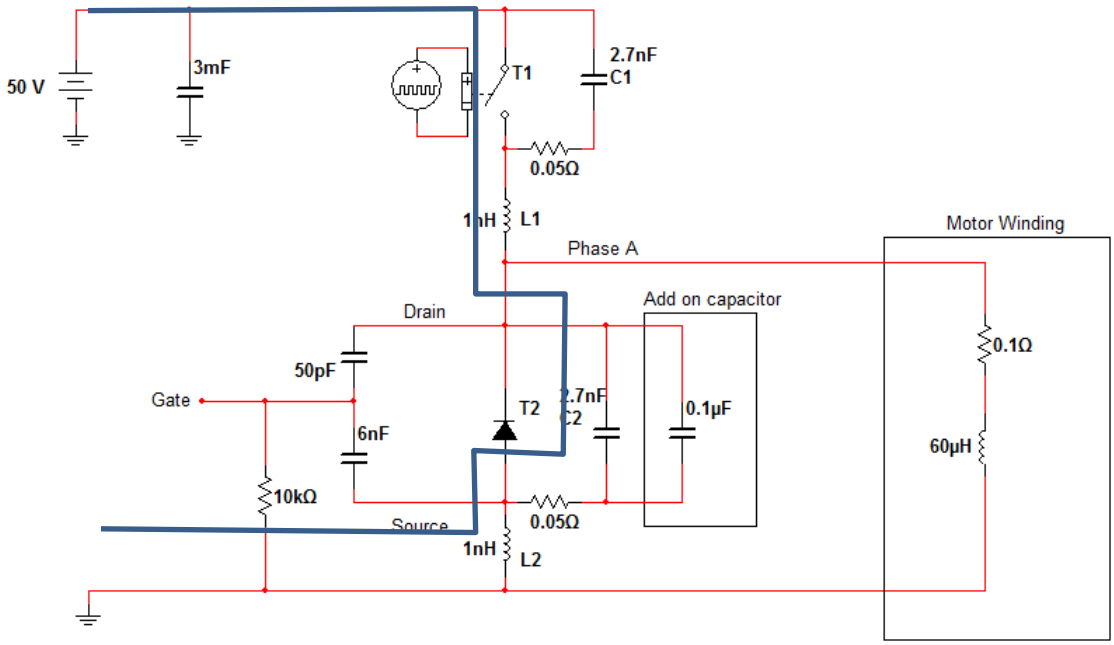



Fig. 2-25. SPICE simulation of ringing on Phase A.

Fig. 2-25 shows an equivalent circuit with all the key parasitics that produce the 60-MHz ringing. T1 and T2 represent the high- and low-side MOSFETs, respectively. T2 is open with only the freewheel diode carrying the current while T1 is controlled by an ideal switch. When T1 closes, the diode in T2 will turn off suddenly and current to the motor will be supplied through T1. When T1 opens, the current will keep flowing to the motor through the diode in T2. The blue current path forms a parallel LC circuit with C2 and L1+L2. The values of gate to drain capacitance Cgd and gate to source capacitance Cgc are obtained from Fig. 2-24 at $V_{ds}$ = 50 V. Ringing observed in the gate voltage is coupled through those two capacitances. Fig. 2-26 shows the simulation results without the

add-on capacitor. The blue curve is the Phase A voltage, green is the gate voltage, and red is the phase current.

The simulation results show that the magnitude of the ringing in the phase voltage increases as the phase current rises. The ringing frequency in Fig. 2-27 is 59 MHz. (L1 and L2 are tuned to ring with C2 at that frequency). The gate voltage is 180 degrees out of phase, which agrees with Figs. 2-21 and 2-23. With a 0.1 μF capacitor added as shown in Fig. 2-25, the ringing frequency shifts to 10 MHz (Fig. 2-28). This agrees with the measured results in Fig. 2-23.

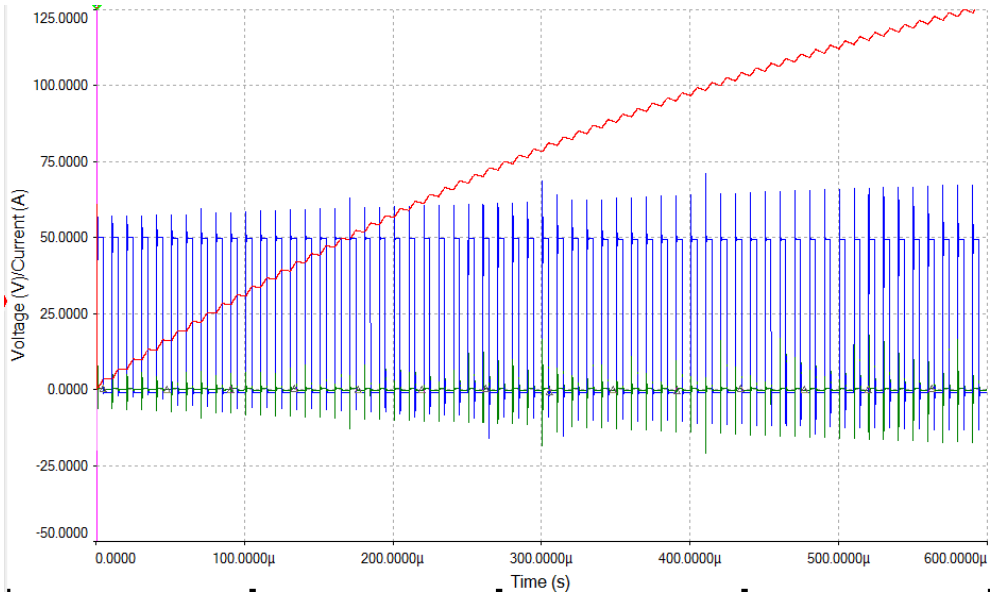



Fig. 2-26. Simulation result w/o add-on capacitor.

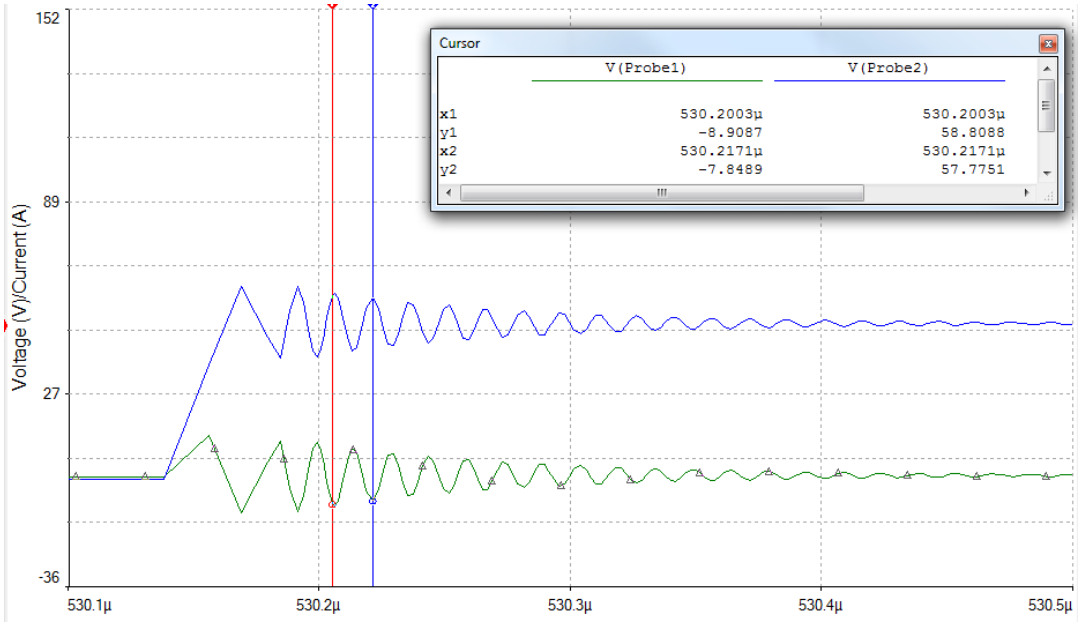



Fig. 2-27. Zoomed in simulation result w/o add-on capacitor.

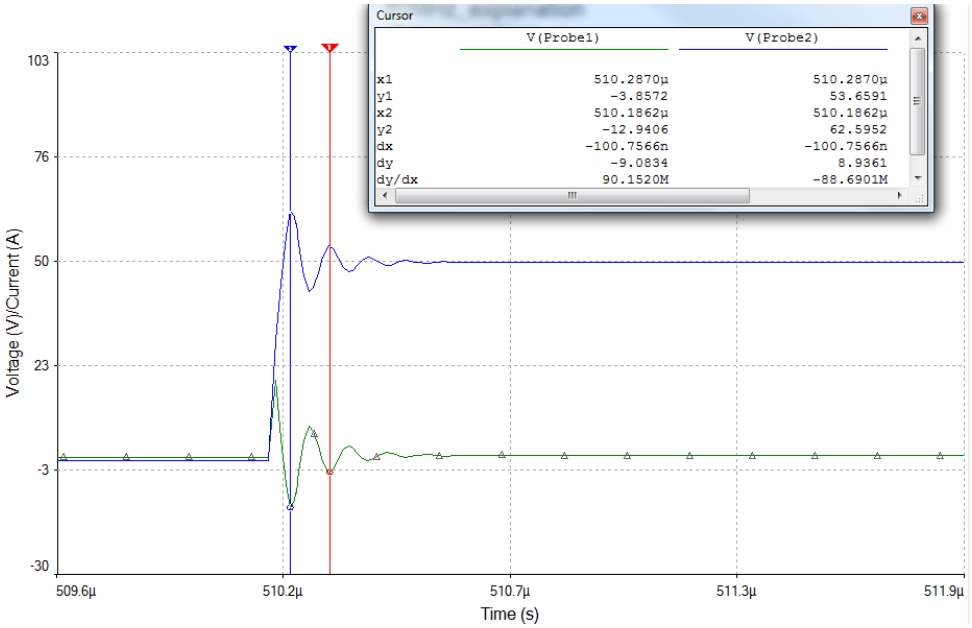



Fig. 2-28. Zoomed in simulation result w/ add-on capacitor.

## 2.6 The influence of the 60 MHz ringing on the common mode current

### *Q-factor and ringing*

As indicated earlier, the Q-factor of the 60 MHz ringing is about 5. This estimate is made by counting the number of the peaks that occur before the ringing magnitude decays to 5% of its original peak value [1]. The Q-factor can also be approximated as the resonant frequency divided by the 3-dB bandwidth in the frequency domain. A Q-factor of 5 is thus a relatively broad hump in the frequency domain. As indicated in the plot of the measured common-mode phase current in Fig. 2-29, the 60-MHz ringing appears to contribute little to the overall amplitude. The effect of this ringing on radiated emissions from a resonant structure will be investigated in the near future.

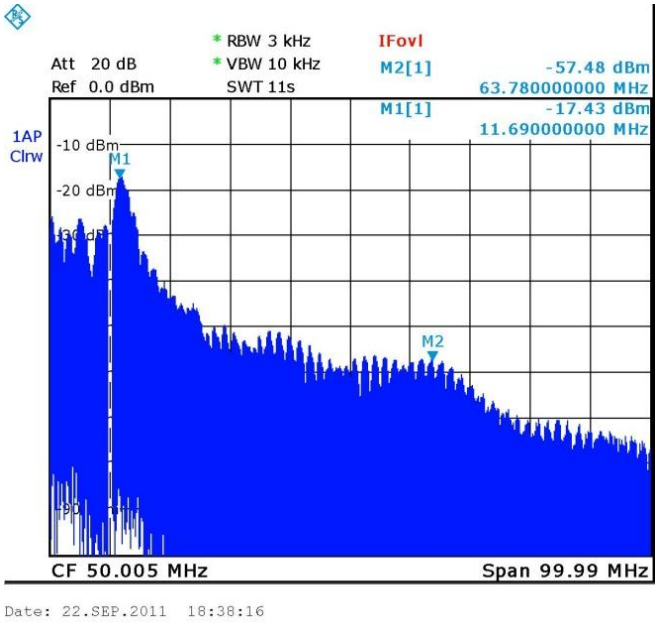



Fig. 2-29. Measure common mode current showing broad hump at 60 MHz.

## 2.7 Methods for reducing the common mode current

### *Minimizing drain-to-source parasitic capacitances of high-side MOSFETs*

As shown in Fig. 2-8, if we can eliminate C1, C3, C5, and C12 and keep the other parts balanced, the differential-mode phase switching will not produce common-mode noise currents. C1, C3 and C5 are the parasitic capacitances from the drains of the high-side MOSFETs to the heatsink (chassis). C12 is the parasitic capacitance from the ground plane of the board to the heat sink. One way to significantly reduce these capacitances is to have the source of each of the high side N-channel MOSFETs be thermally coupled to the heat sink rather than the drain. An alternative but less electrically efficient way would be to use P-channel devices for the high side MOSFETs and have the drains be thermally connected to the heat sink. The former concept is currently being tested with an inverter board that is designed so that the source terminals of the high side MOSFETs are connected by thermal vias to large thermal pads on the bottom layer of the board that are capacitively and thermally connected to the heat sink. Additionally, capacitances from the ground and power planes of this board to the chassis are minimized. A prototype board being used for this investigation is shown in Fig. 2-30.

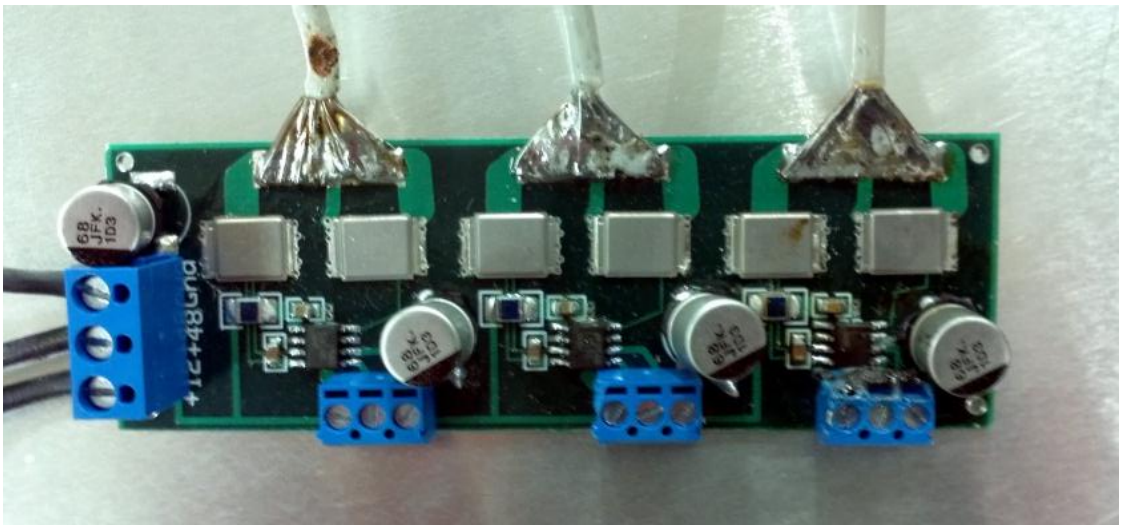


Fig. 4-30. Prototype board used to evaluate alternative MOSFET configurations.

### *Driving inverter chassis relative to 0-volt supply conductor*

Another way to prevent differential switching voltages from producing common-mode noise current is to actively compensate for the imbalances in the driver circuitry by driving the 0-volt ground on the circuit board relative to the frame ground of the vehicle. An active feedback circuit is being developed that employs a wide-band, high slew-rate amplifier as shown in Figs. 2-31 and 2-32. Active balancing schemes show great promise for reducing common-mode currents up to several MHz. At higher frequencies, passive balancing appears to be the best low-cost solution. Passive balancing is described in the next section.

### *Isolating the DC link from frame ground*

Noting that most SVPWM modulation schemes intentionally put a common-mode voltage on the phase wires relative to the DC 0-volt reference, the DC inputs should always be isolated from frame ground to prevent common-mode currents from flowing on the frame. Currents returning on the frame do not contribute to the motor torque, but they can contribute to power loss and noise issues.

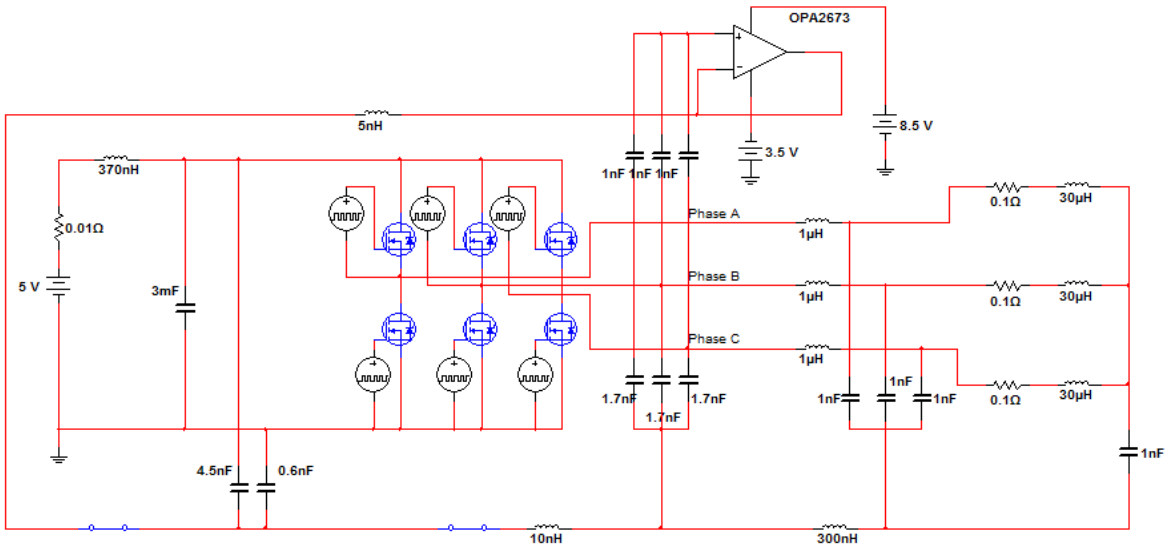



Fig. 2-31. Active balancing scheme.

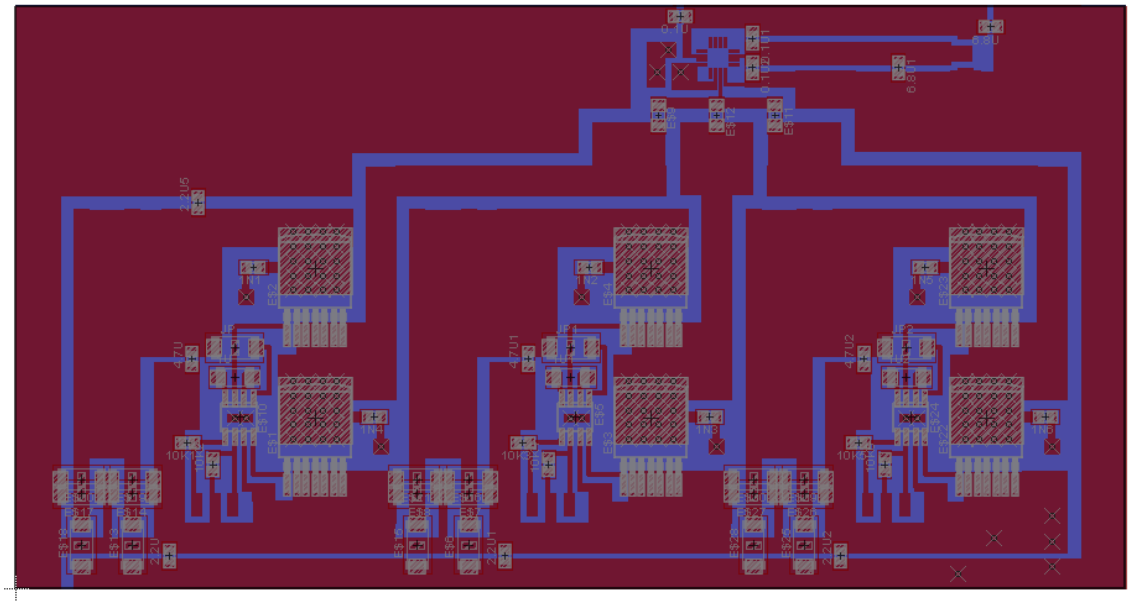


Fig. 2-32. Active balancing test board layout.

In a SPICE simulation of the circuit in Fig. 2-31, the MOSFETs are switching with the pattern of the CBA 001 state at 20 kHz. The common-mode current on the phase wires is plotted in Figs. 2-33 and 2-34. A 30 dB reduction of the CM current from DC to 10 MHz is achieved. Above 30 MHz the CM current increases slightly due to the bandwidth and slew-rate limit of the op-amp. These results are promising, but there is still more work to be done before a practical, low-cost solution is developed.

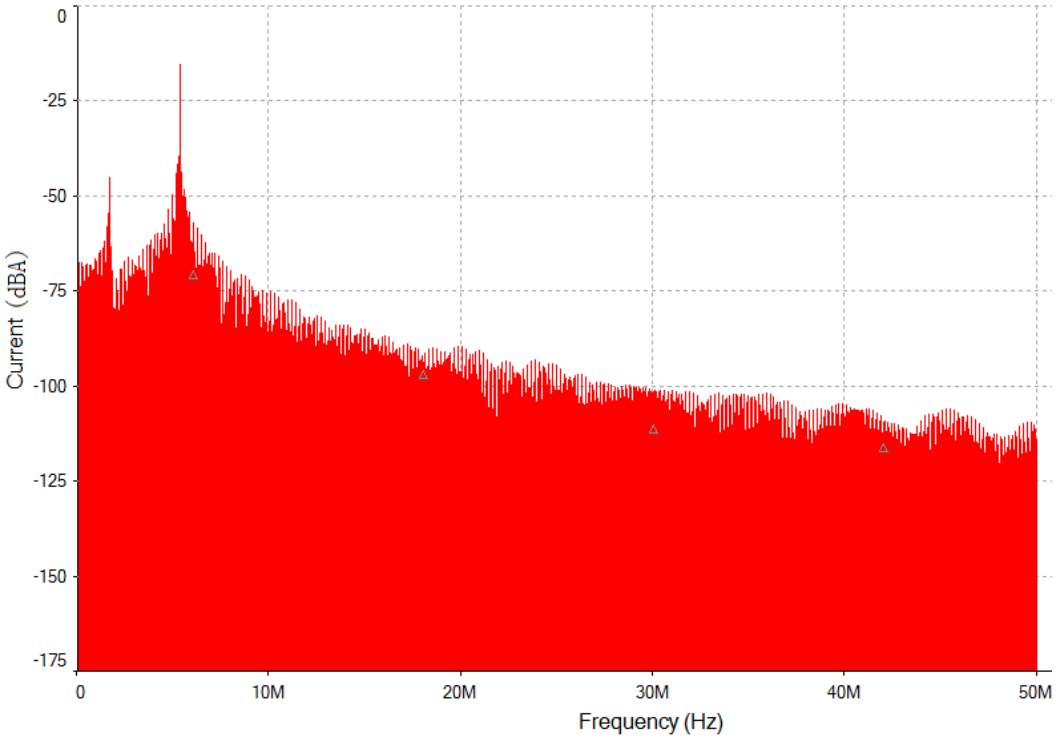



Fig. 2-33. Simulation of CM current w/o active balancing.

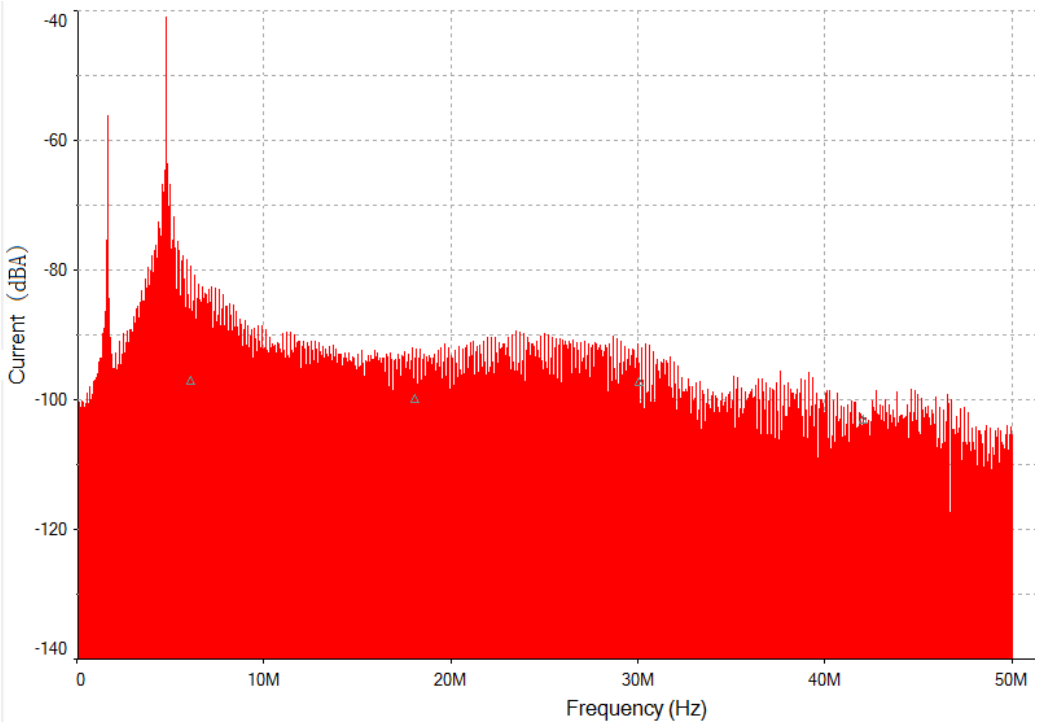



Fig. 2-34. Simulation of CM current w/ active balancing.

# 3. Passive Balancing Network

## 3.1 Overview

The development of a passive balancing network for 3-phase motor drivers was the subject of an earlier report [1] describing work done with a motor driver provided by John Deere. The main idea behind the balancing network is that differential signals (like those driving a 3-phase motor) can only be converted to common-mode noise (like the motor drive currents returning on the vehicle frame) at places where there is a change in the "electrical balance" of the structure [1, 2, 4-7]. Electrical balance is defined as the relative impedance of each conductor in a circuit to a reference ground. In the case of the John Deere motor driver, the motor and the cables were relatively balanced at all frequencies of interest. The motor driver, on the other hand, has impedances to frame ground that change significantly as the motor operates. The difference between the motor driver's balance and the motor/cable assembly balance cause motor drive voltages to induce common-mode currents on the vehicle frame.

At frequencies from 20 kHz to a few MHz, the motor-driver is unbalanced by design. However, it is possible to reduce the noise produced above 10 MHz by making the high-frequency impedances to ground exactly the same on all three phases at the point where the motor driver connects to the three phase wires. This can be accomplished with a resistor and capacitor in series connecting each phase wire to frame ground as illustrated in Fig. 3-1.

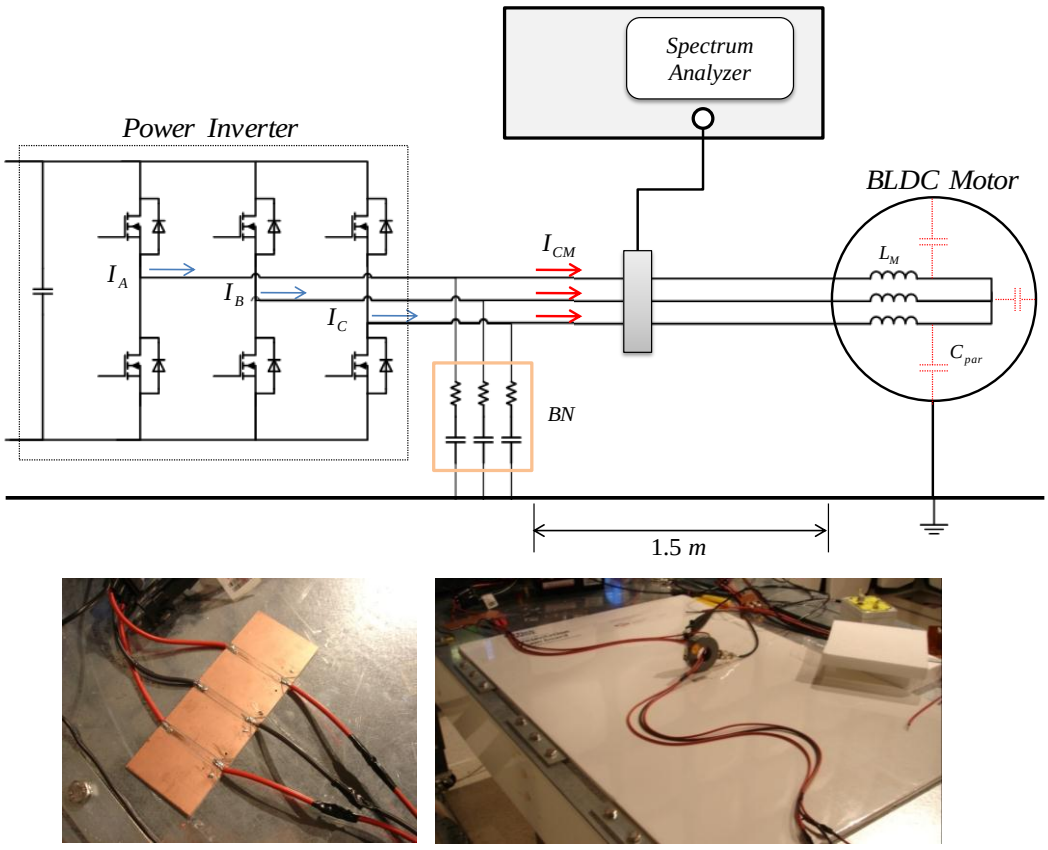



Fig. 3-1. Schematic representation of a passive balancing network (in gold box above) and photos of a prototype implementation used for preliminary evaluations.

## 3.2 Choosing R and C

The values of R and C are chosen to have a cutoff frequency just below the frequencies at which electrical balance is required, but well above the operating frequencies of the motor drive. At high frequencies, the capacitors are essentially short circuits and the impedance to frame ground is determined by the resistor value.

- The resistor value must be low relative to the impedance of the power inverter at the frequencies of interest. Adding inductance to the phase wires between the power inverter MOSFETs and the balancing network can help to ensure that the resistor value is lower than the power inverter impedance at high frequencies. It is also helpful to reduce the capacitance between the DC link conductors and the frame ground.
- The resistance must be high relative to the impedance associated with the inductance of balancing network's connection to the frame ground. Otherwise, imbalances in the inductance values will overwhelm the balancing effect of the RC circuit, especially at resonances associated with the network capacitance and the connection inductance.

If the motor driver is laid out on a multi-layer PCB, and chassis ground is available as a solid plane under the phase wire connections, the connection inductance can be as low as 5 nH (using short traces and direct connections to the plane). At frequencies below 100 MHz, this is about 30 ohms or less of impedance. Therefore, choosing a resistor with a value of 50 ohms should provide a reasonably stable impedance below 100 MHz. Lower values will not work as well at the high end of the frequency range, but may provide better isolation from the power inverter at the lower end of the frequency range.

Once a resistor value has been chosen, the capacitor value should be selected to provide an appropriate cut-off frequency. For example to obtain a cut-off frequency of about 3 MHz, the appropriate value of C would be:

$$\begin{aligned} C &= \frac{1}{2\pi R(f_{cut-off})} \\ &= \frac{1}{2\pi(50\,\text{ohms})(3\,\text{MHz})} \\ &\simeq 1000\,\text{pF} \end{aligned} \tag{1}$$

While the exact values of R and C are not critical, it is important that each of the three branches of the balancing network have the same values. Therefore components with relatively precise tolerances (e.g. 1%) should be chosen and they should be laid out with exactly the same trace and via geometry. The capacitors must have a voltage rating equal to or greater than the DC link voltage and must not be polarized. NPO ceramic multilayer capacitors are preferred for their tight tolerances and stability with temperature.

To calculate the rated power of the resistors, it is observed that the resistors only carry significant current during the phase transitions. The maximum current through one of these resistors during any transition is,

$$I_{\max} = C\frac{\delta v_{\max}}{\delta t} \approx C\frac{V_{phase}}{t_r} \tag{2}$$

where $V_{phase}$ is the DC link voltage and $t_r$ is the 10- 90% transition time of the phase voltage waveform. There are two transitions per switching cycle, so the energy dissipated in one switching cycle is,

$$\text{Energy/cycle} = 2t_r \left(I_{\max}\right)^2 R = 2RC^2 \frac{V_{phase}^2}{t_r} \tag{3}$$

The average power dissipated is the energy dissipated per cycle times the switching frequency in cycles per second. Therefore, the average power dissipated by the resistor when the full phase voltage appears across the balancing network is,

$$P_{ave} = 2 f_{PWM} RC^2 \frac{V_{phase}^2}{t_r} \tag{4}$$

For example, the CA6 inverter has a DC link voltage of 48 volts, a switching frequency of 20 kHz, and a phase voltage risetime of approximately 50 ns. A balancing network with R = 50 Ω and C = 1 nF would dissipate an average power of,

$$\begin{aligned} P_{ave} &= 2 f_{PWM} RC^2 \frac{V_{phase}^2}{t_r} \\ &= 2(2x10^4 \text{ Hz})(50\,\Omega)(10^{-9} \text{ F})^2 \frac{(48 \text{ V})^2}{(60x10^{-9} \text{ sec})} \\ &= 80 \text{ mW} \end{aligned} \tag{4}$$

Generally, quarter-watt or half-watt resistors will be fine for most low-voltage inverters. Composite resistors are preferred over metal-film resistors, because they will generally have a lower inductance and a greater immunity to transients on the phase wires.

## 3.3 CA6 Inverter Measurements

*Test Setup*

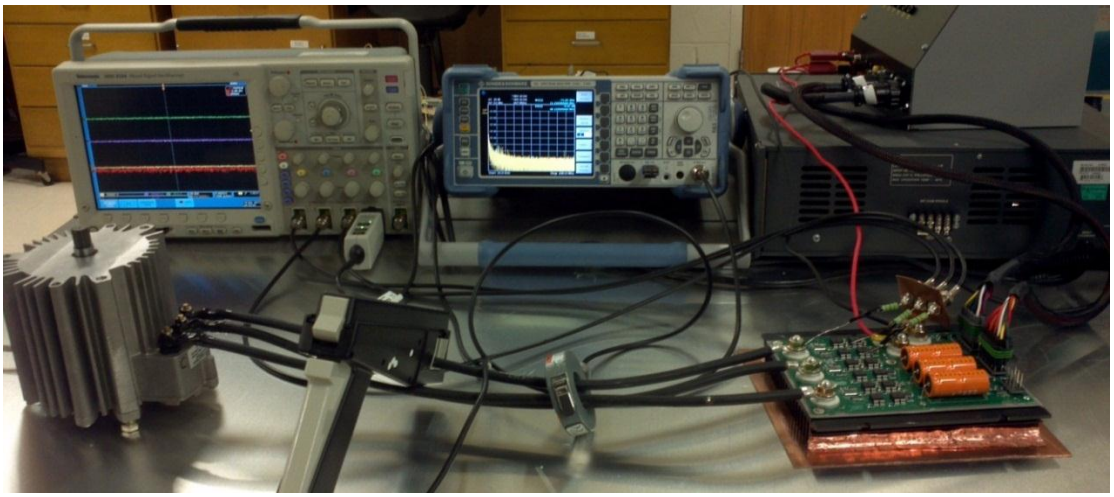


Fig. 3-2. CA6 inverter test setup.

As shown in Fig. 3-2, the John Deere CA6 inverter and motor were placed on a metal ground plane and connected by three 60-cm phase wires approximately 7 cm above the plane. A BK Precision high current regulated power supply provided 48 volts to the CA6 inverter input on the right side of the figure. Common-mode current measurements were made with the Fischer Custom Communications F-33-1 current probe clamped around all three phase wires and connected to the Rohde and Schwarz FSL

spectrum analyzer in the center of the figure. Individual phase currents were monitored with a Tektronix TPO 150 current probe connected to the Tektronix MSO 4104 oscilloscope shown on the left.

### *Test procedure*

The control box was used to select each of the 6 possible inverter states. Knob D (Fig. 2-2) was used to set the average current on the active phases to be 50 amps as measured by the TPO 150 current probe. In each state, the common-mode current was measured using the F-33-1 current probe and the spectrum analyzer. For reference, the noise floor (i.e. common-mode current measurement with inverter powered off) is shown in Fig. 3-3. The measured common-mode currents for the inverter in each state are plotted in Fig. 3-4 with balancing networks on each of the three phases and the two DC inputs. Generally, the common-mode current in each state exhibits a peak around 12 MHz with an amplitude within a few dB of -20 dBm (or approximately 4.5 mA).

Fig. 3-5 shows the measured common-mode current in each state for the inverter with the balancing networks removed from the two DC inputs. Fig. 3-6 shows the measured common-mode current in each state for the inverter with the balancing networks removed from the two DC inputs and the Phase A output. Fig. 3-7 shows the measured common-mode current in each state for the inverter with all balancing networks removed.

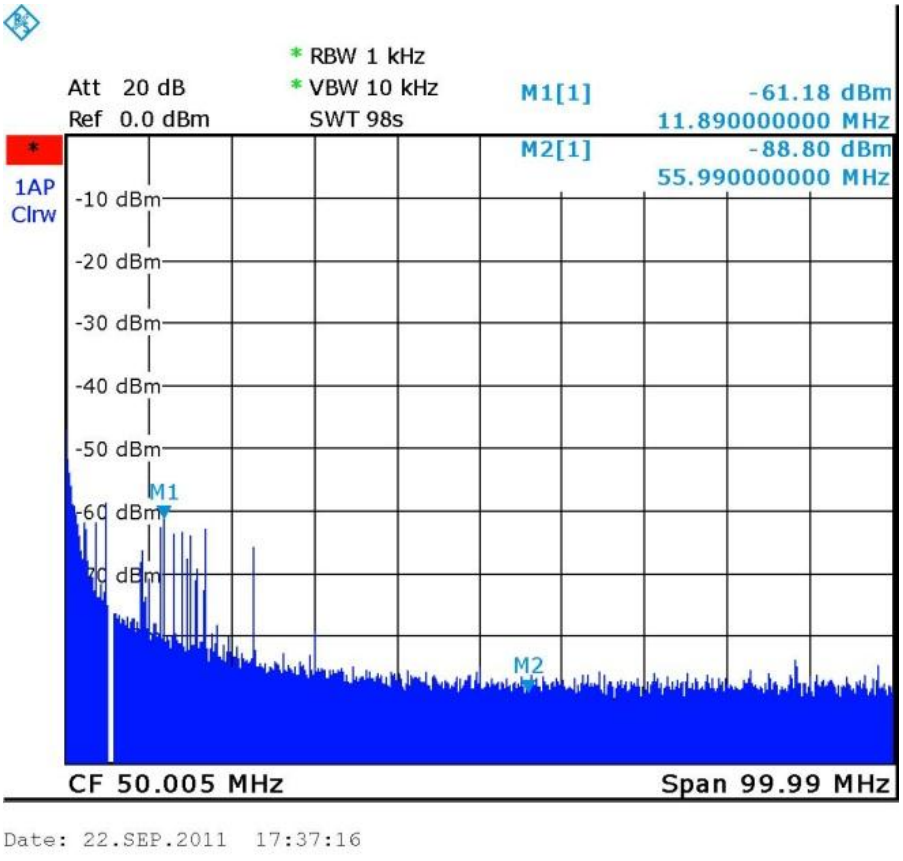



Fig. 3-3. Common-mode current measurement noise floor.

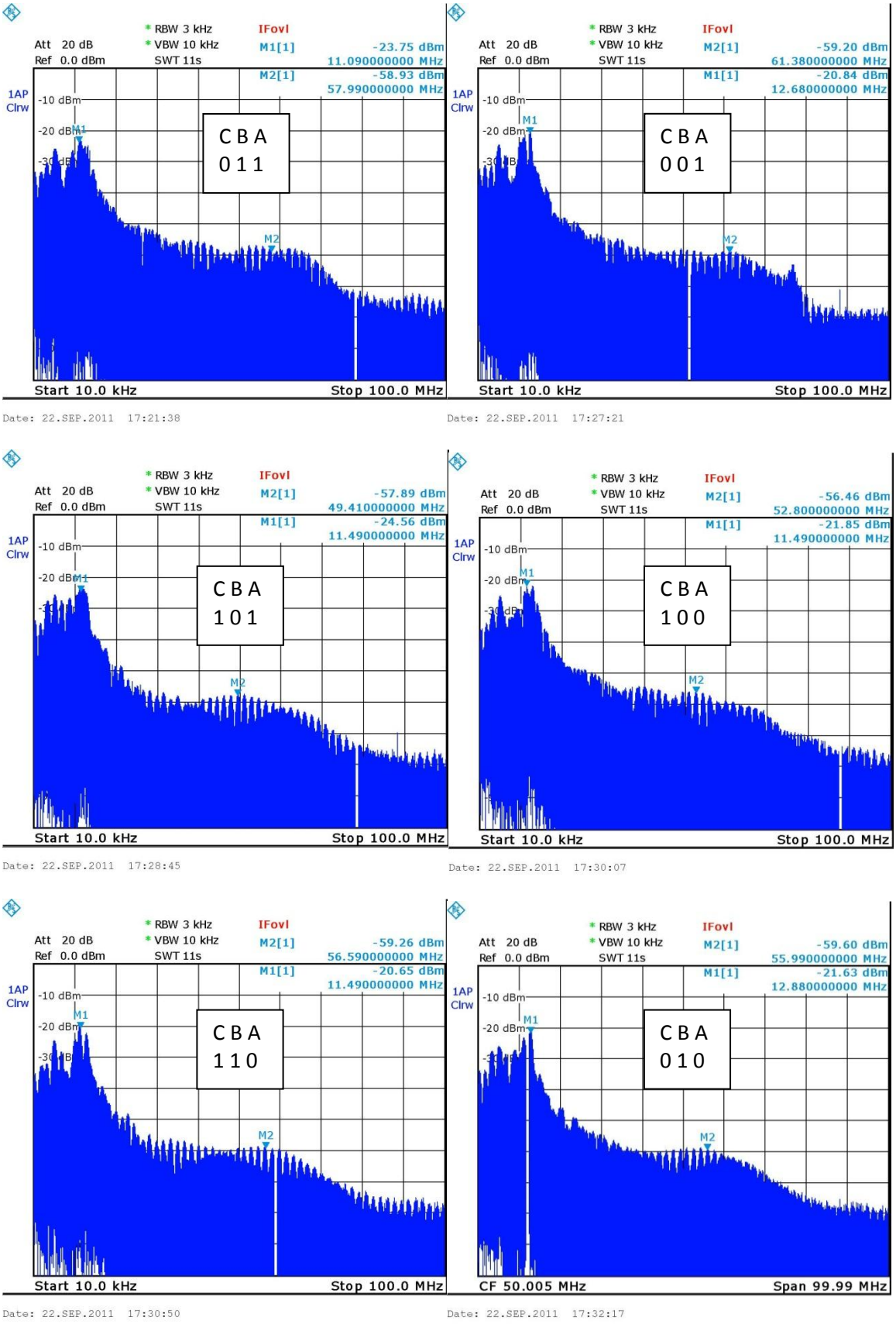



Fig. 3-4. Measured common-mode current w/ BN on both DC and phase terminals.

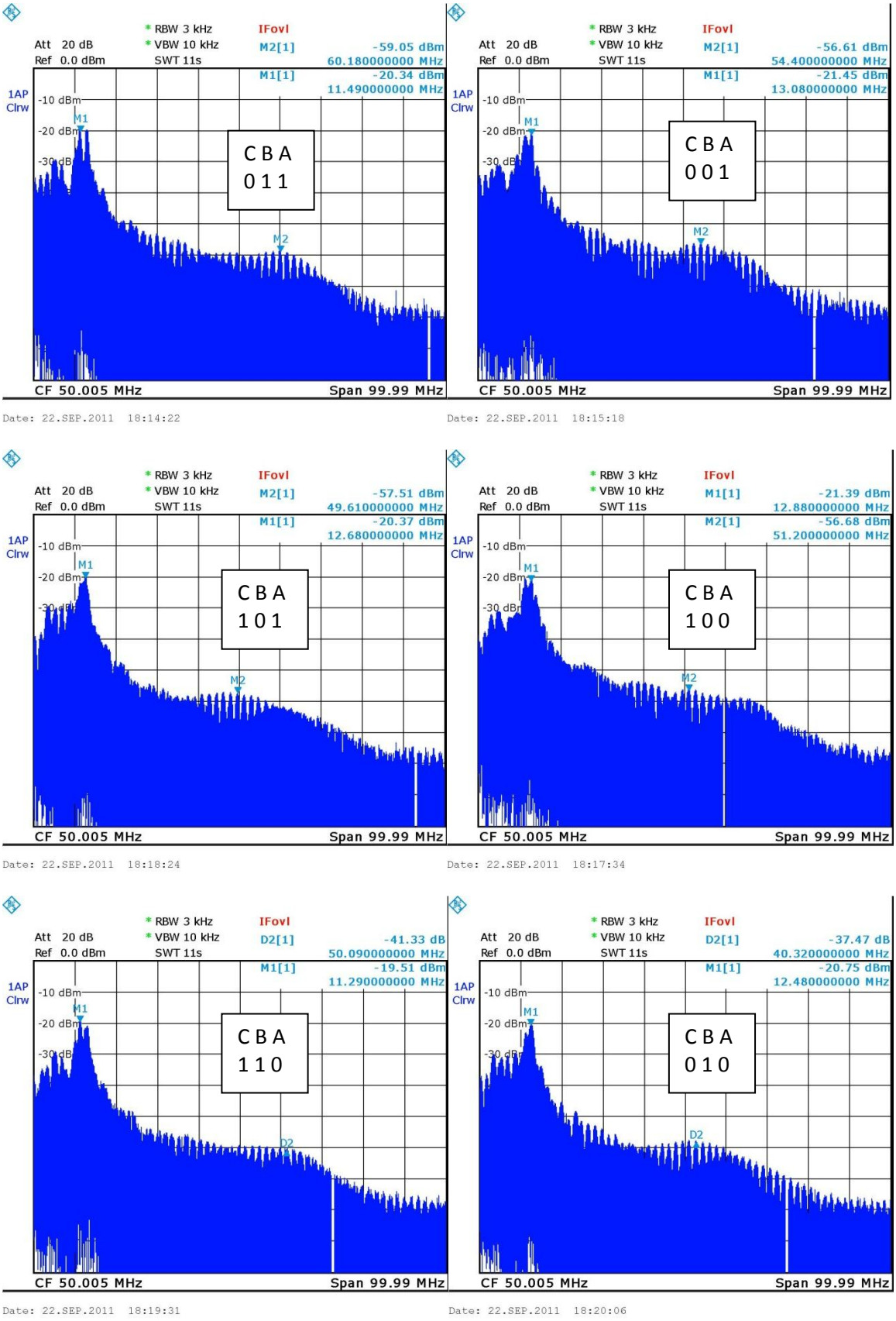



Fig. 3-5. Measured CM current w/ BN on Phase terminals, w/o BN on DC terminals.

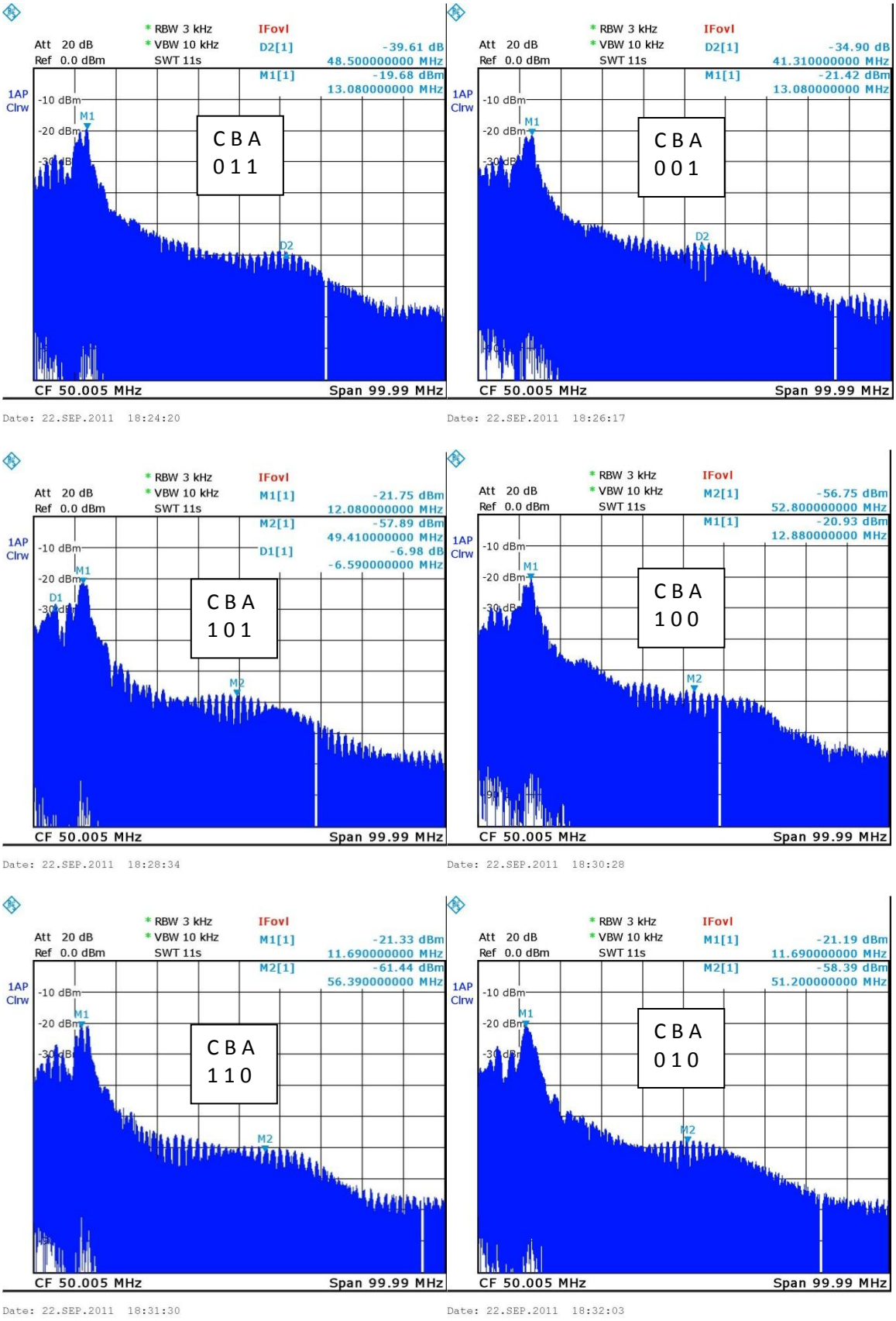



Fig. 3-6. Measured CM current w/ BN on B and C terminals, w/o BN on DC and A terminals.

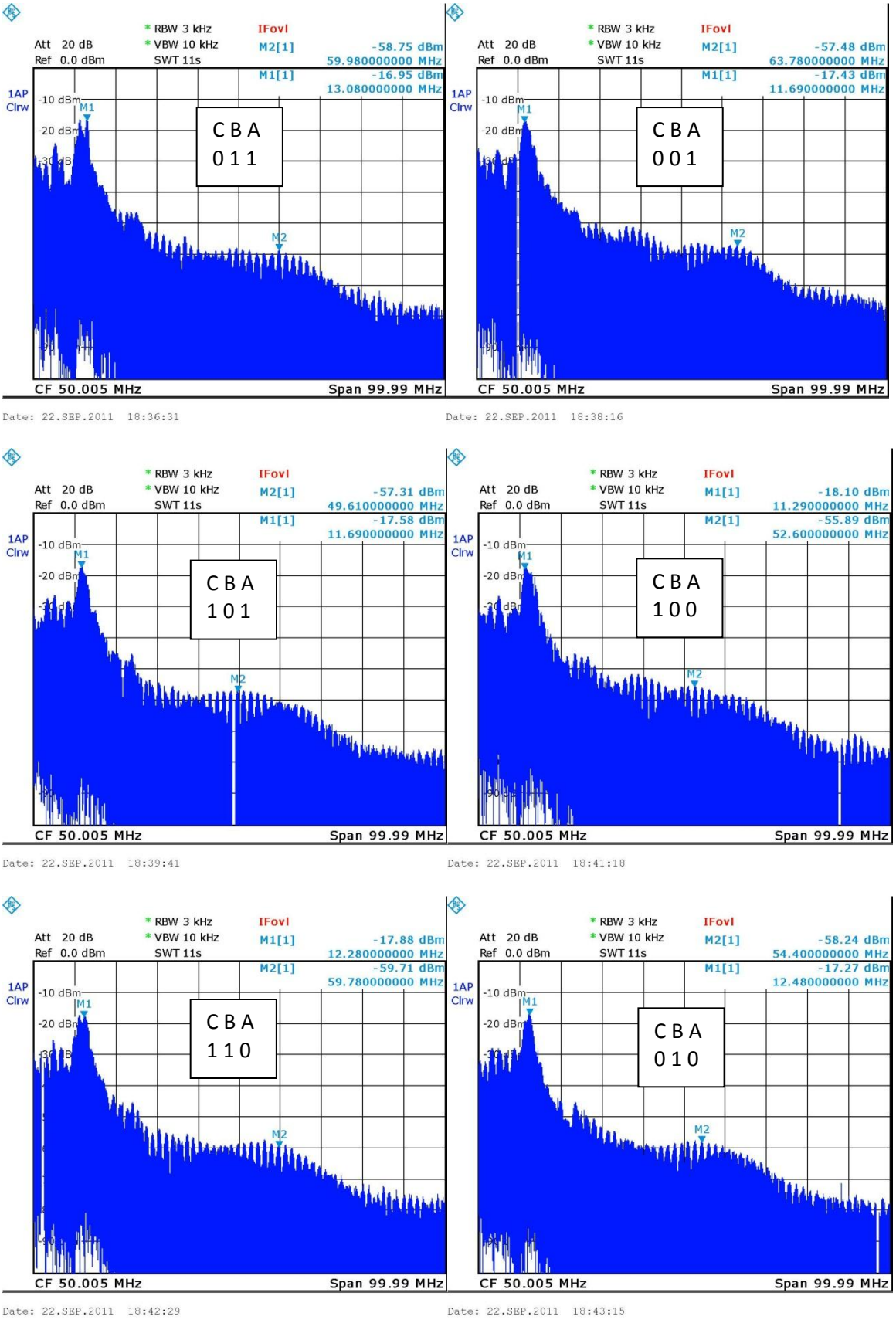



Fig. 3-7. Measured CM current w/o BN on either DC or phase terminals.

Fig. 3-8 shows the peak values from the plots in Figs. 3-3 through 3-7 for the CBA 001 state. While it is clear that the common mode currents from 10 MHz to 60 MHz are generally lower with the balancing network than without, the overall reduction is only a few dB. Figs. 3-9 and 3-10 show similar results for the inverter in the 110 and 011 states.

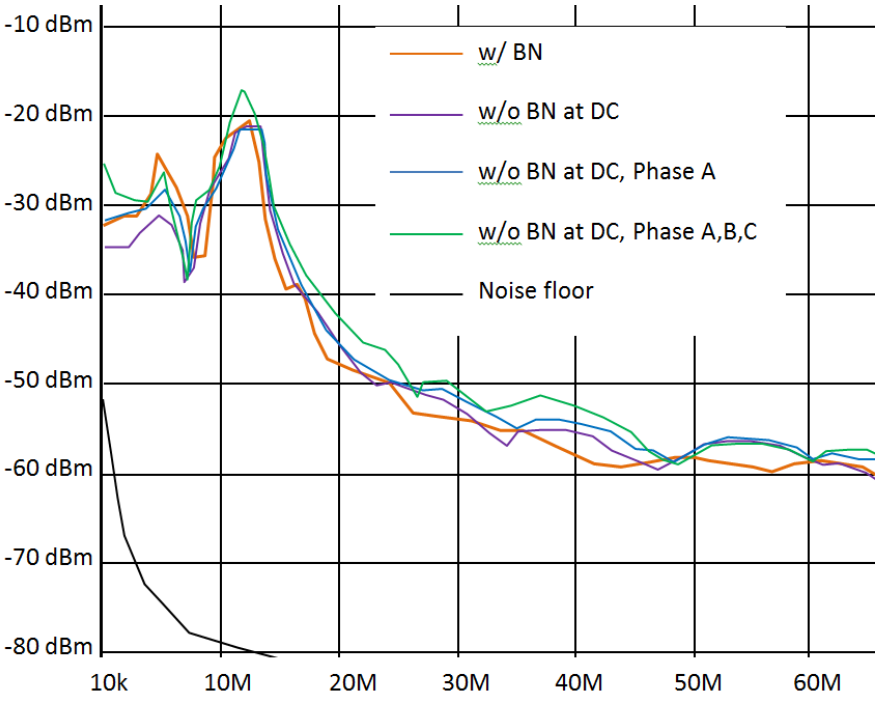



Fig. 3-8. Measured CM current with inverter in the CBA 001 state.

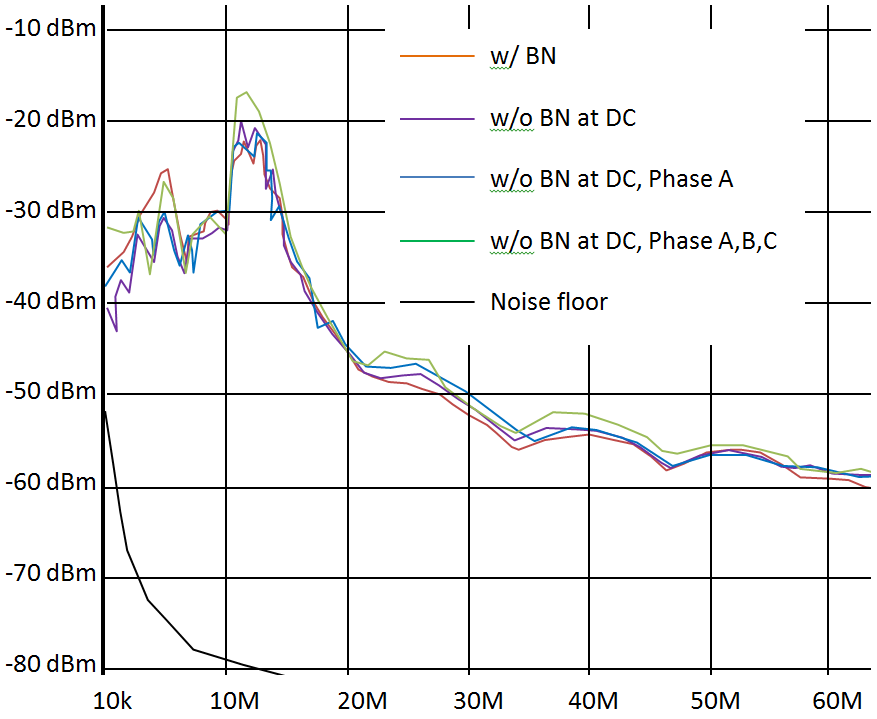



Fig. 3-9. Measured CM current with inverter in the CBA 110 state.

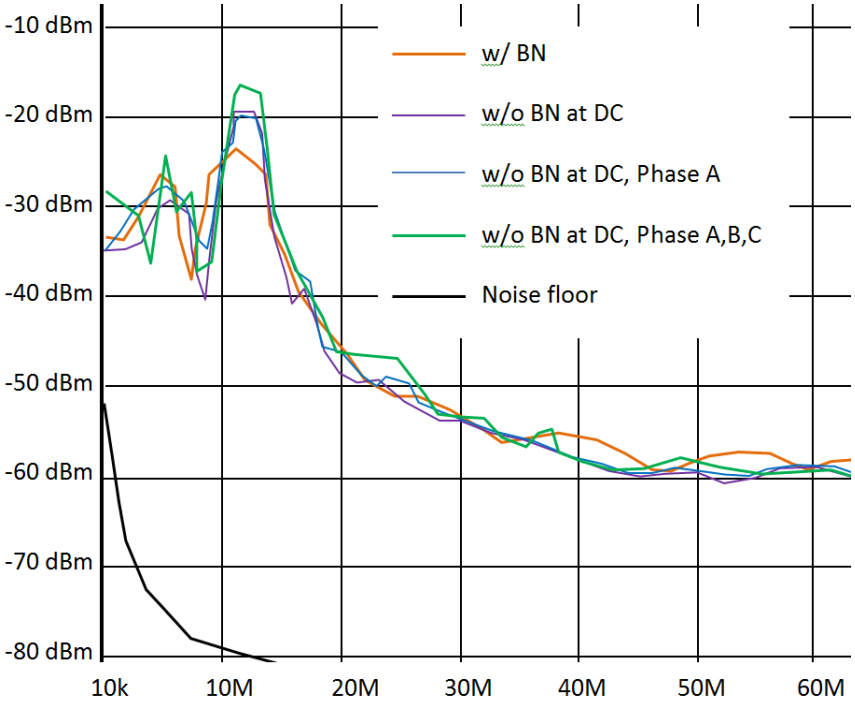



Fig. 3-10. Measured CM current with inverter in the CBA 011 state.

Choosing the optimum values of R and C can be difficult without knowing the impedance of the inverter output, so other values of R and C were tried. Fig. 3-11 shows the measured common-mode current in each state with a 3-nF capacitor and a 47-Ω resistor used as a balancing network. In this case, there was no balancing network on the inverter's DC inputs. Similarly, Fig. 3-12 shows the measured common-mode current with a 3-nF, 23.5-Ω balancing network and Fig. 3-13 shows the results with a 3-nF, 0-Ω balancing network.

Since these measurements were performed by a different researcher on a different day than the measurements in Figs. 3-4 through 3-10, small differences in the results are not necessarily relevant. However, each of the configurations with the larger capacitance reduces the peak of the spectrum at around 12 MHz by at least 5 dB. The balancing network as currently implemented on the CA6 inverter board appears to significantly reduce this peak relative to measurements without the balancing network or with just the 1-nF capacitors. The 0-ohm network reduces the middle of the spectrum, but increases the current at higher frequencies.

Although more analysis remains to be done, the preliminary results suggest that balancing networks on phase outputs and the DC inputs of the CA6 inverter reduce peak emissions by 5 dB or more. The resonant peak in our test set-up occurred at 12 MHz due to the geometry of our motor/harness structure. Future measurements will be made using a set-up that radiates the common-mode power and resonates at a frequency above 30 MHz. We will also experiment with a two-capacitor structure similar to the one described in [8].

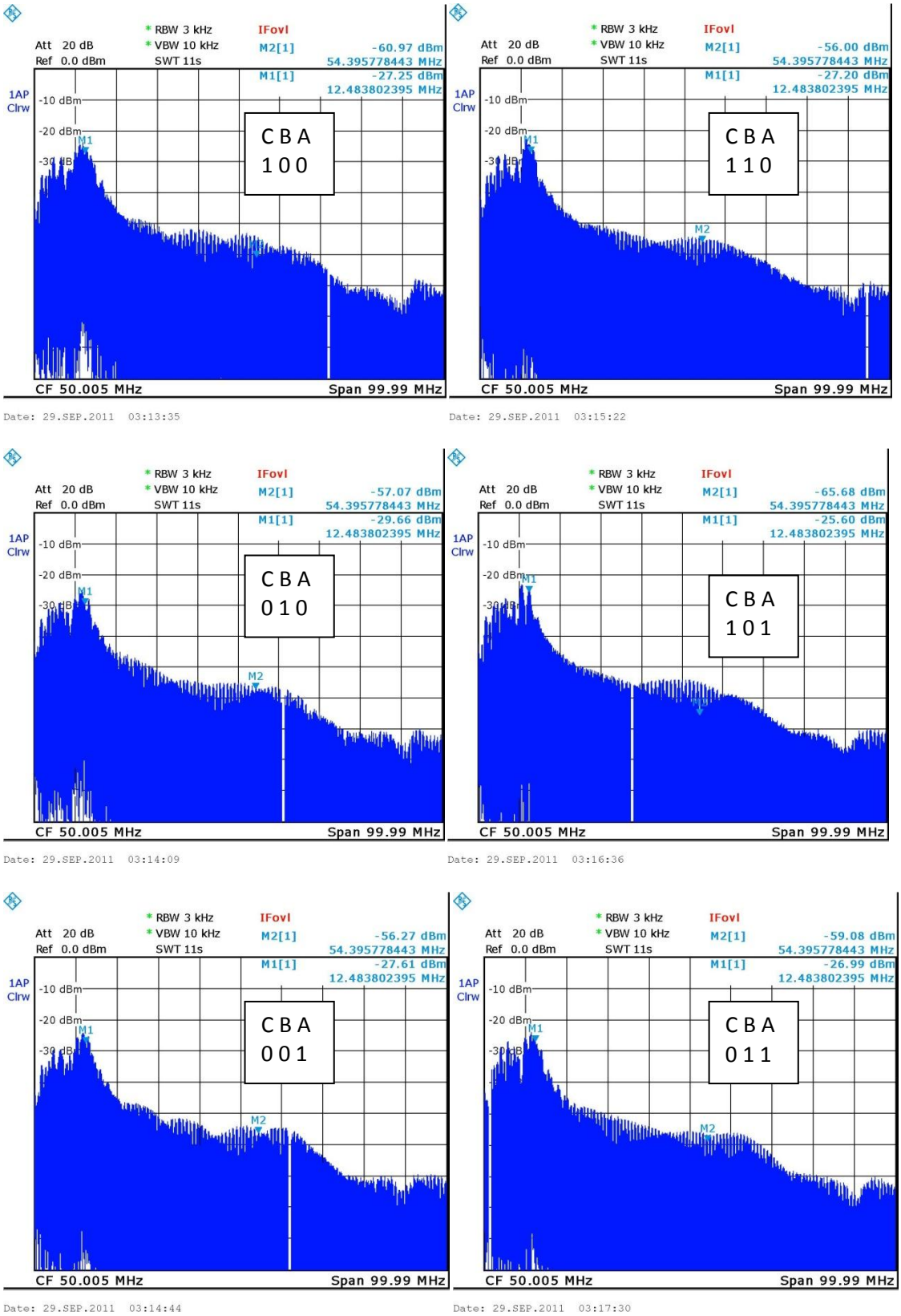



Fig. 3-11. Measured CM current with 3-nF, 47-Ω balancing network.

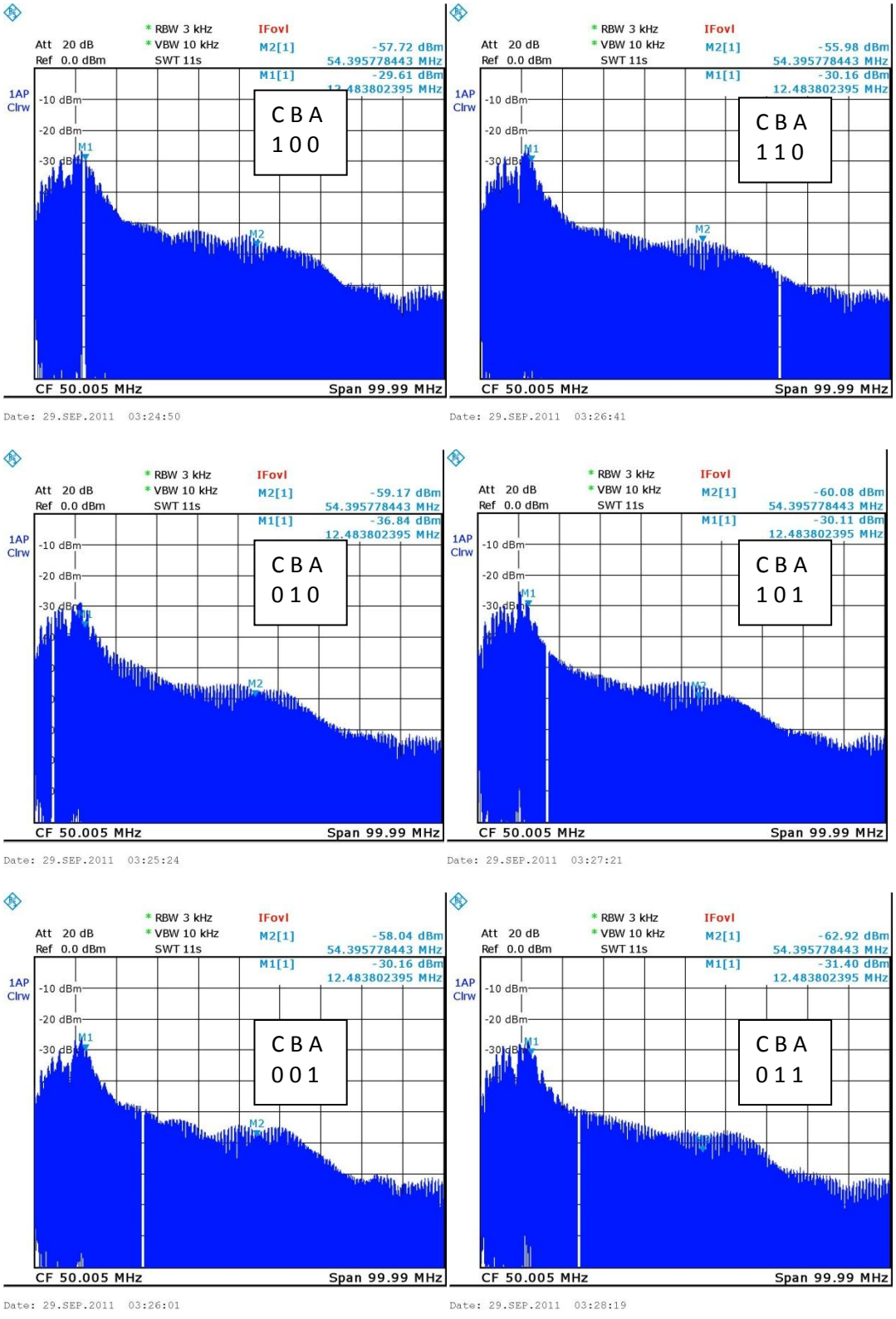



Fig. 3-12. Measured CM current with 3-nF, 23.5-Ω balancing network.

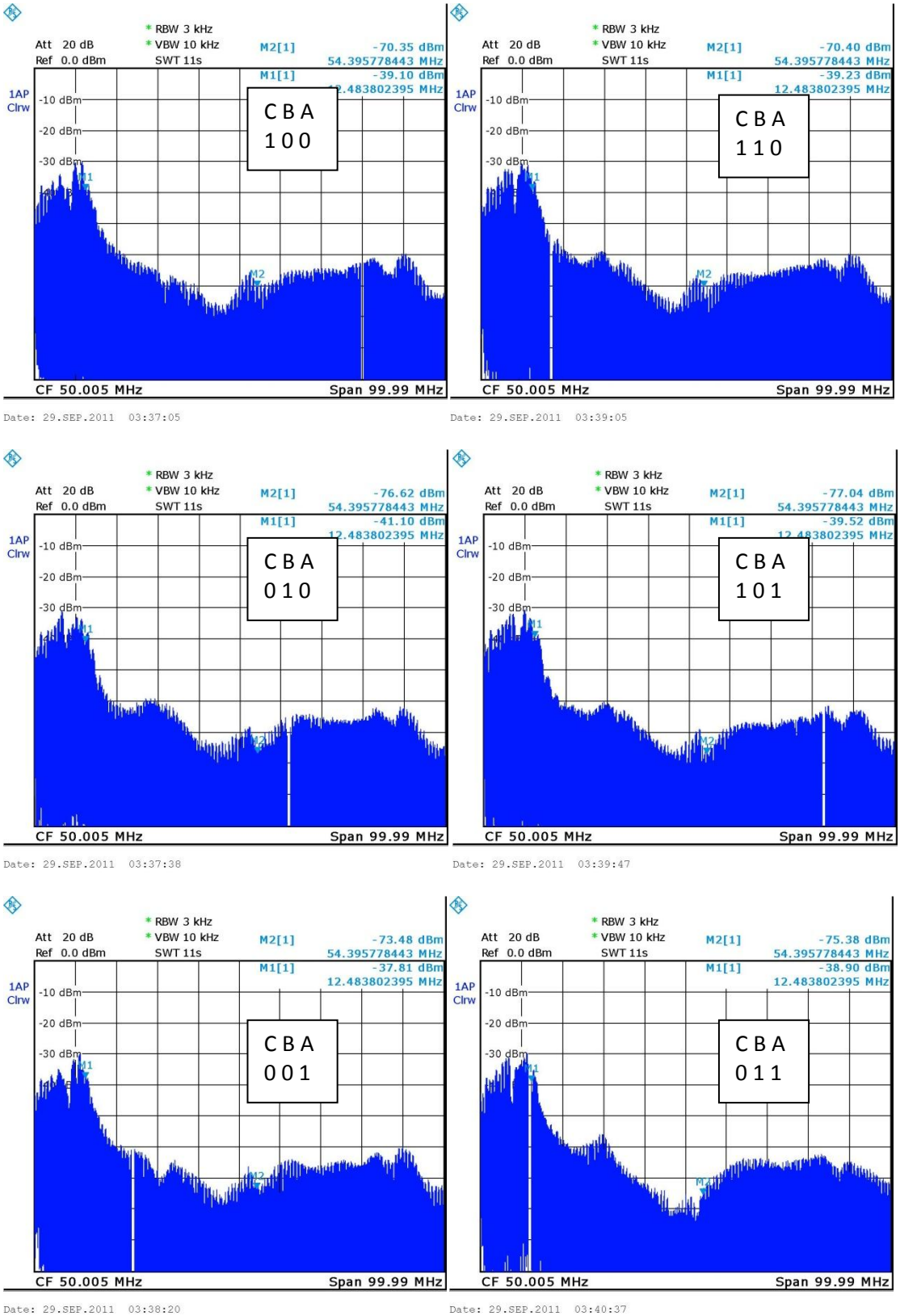



Fig. 3-13. Measured CM current with 3-nF, 0-Ω balancing network.

# 4. Summary and Future Research Directions

The primary goal of this project is to provide a cost sensitive (i.e. without ferrites) production solution to reduce conducted and radiated electromagnetic emissions to levels that will allow Class A and Class B inverters to pass EN14982 / CISPR12. Since the ferrites currently found on power inverters are targeted towards frequencies around 30 MHz, it seems likely that the balancing network currently implemented on the CA6 inverter is capable of eliminating the need for these ferrites. However, EN14982 and CISPR12 cover a wide range of frequencies and more work will be required to extend the bandwidth and improve the overall performance of these passive balancing networks. Clemson researchers will continue to evaluate the existing design as implemented on the CA6 inverter to evaluate its effect on radiated emissions and determine optimum values for the network components. They will also evaluate alternative network designs that provide stable impedance over a greater bandwidth.

Since passive balancing networks are a high-frequency solution. Clemson researchers will continue to investigate alternative MOSFET switching structures with a naturally balanced capacitance as well as active balancing techniques for reducing common-mode emissions in the kHz – MHz frequency range.

# References


[1] H. Kwak and T. Hubing, "A Novel Balanced Cable Interface for Reducing Common-Mode Currents from Power Inverters and Other Electronic Devices," Clemson Vehicular Electronics Laboratory Technical Report # CVEL-10-018, April 8, 2011.

[2] H. Kwak and T. Hubing, "Investigation of the Imbalance Difference Model and its Application to Various Circuit Board and Cable Geometries," Clemson Vehicular Electronics Laboratory Technical Report # CVEL-10-017.1, May 21, 2011.

[3] C. Zhu and T. Hubing, "Estimating the Q-factor of Resonances in the Time Domain," Clemson Vehicular Electronics Laboratory Technical Report # CVEL-11-028, October 1, 2011.

[4] Tetsushi Watanabe, Hiroshi Fujihara, Osami Wada and Ryuji Koga, " A prediction method of common-mode excitation on a printed circuit board having a signal trace near the ground edge," *IEICE Trans. Commun*., vol. E87-B, no. 8, pp. 2327-2334, Jun. 2004.

[5] Tohlu Matsushima, Tetsushi Watanabe, Yoshitaka Toyota, Ryuji Koga and Osami Wada, "Increase of common-mode radiation due to guard trace voltage and determination of effective via-location," *IEICE Trans. Commun*., vol. E92-B, no. 6, pp. 1929-1936, Jun. 2009.

[6] Tohlu Matsushima, Tetsushi Watanabe, Yoshitaka Toyota, Ryuji Koga and Osami Wada, "Evaluation of EMI reduction effect of guard traces based on imbalance difference method," *IEICE Trans. Commun*., vol. E92-B, no. 6, pp. 2193-2200, Jun. 2009.

[7] Changyi Su and Todd Hubing, "Imbalance difference model for common-mode radiation from printed circuit board," *IEEE Transactions on Electromagnetic Compatibility*, vol. 53, no. 1, Feb. 2011, pp. 150-156.

[8] T. Zeeff, T. Hubing, T. Van Doren and D. Pommerenke, "Analysis of simple two-capacitor low-pass filters," *IEEE Transactions on Electromagnetic Compatibility*, vol. 45, no. 4, Nov. 2003, pp. 595-601.