CVEL

THE CLEMSON UNIVERSITY VEHICULAR ELECTRONICS LABORATORY

TECHNICAL REPORT: CVEL-12-030

An Active Balancing Circuit for 3-Phase AC Motor Drivers

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EXECUTIVE SUMMARY

This report provides a summary of the design and testing of an active balancing circuit for three-phase AC motor drivers. The circuit actively compensates for the imbalances in the driver circuitry by driving the 0-volt ground on the circuit board relative to the common chassis of the load and the circuit board. The active balancing circuitry was able to reduce the common-mode current on the phase wires by as much as 10 dB in the 10 kHz – 20 MHz frequency range.

I. INTRODUCTION

This report provides a summary of the design and testing of an active balancing circuit for three-phase AC motor drivers. The circuit actively compensates for the imbalances in the driver circuitry by driving the 0-volt ground on the circuit board relative to the common chassis of the load and the circuit board. Section II covers the design of the board with a focus on the active balancing part of the circuit. Section III describes the test method and the test results. Section IV compares and discusses the test results. Section V summarizes the active balance circuit tests.

II. Circuit Board Design

A. Circuit schematic.

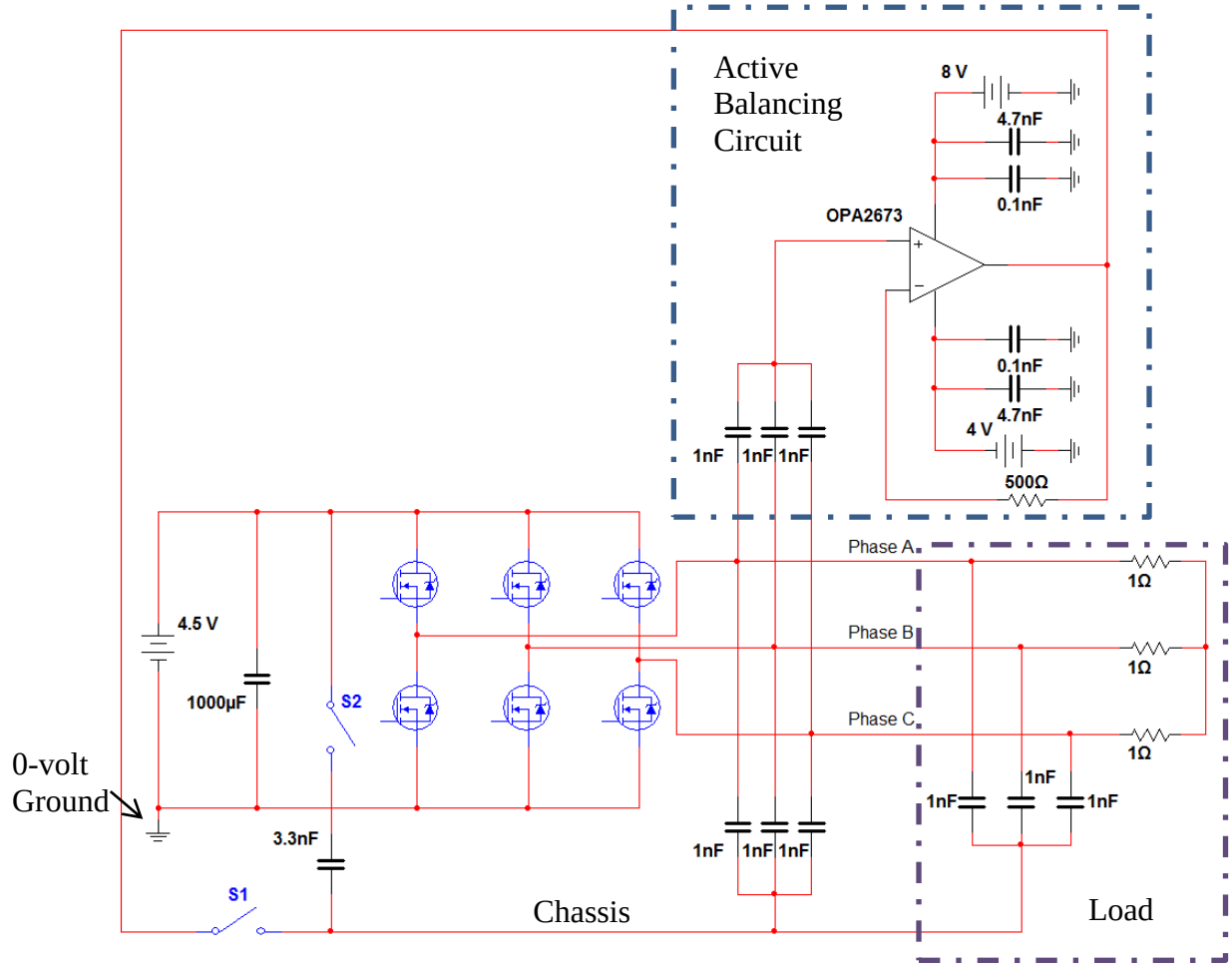

Fig. 1. Active balancing circuit board schematic.

Fig. 1 shows the schematic of the active balancing circuit. The circuit employs a unity gain amplifier (OPA 2673) to drive the board chassis relative to the 0-volt ground of the board. The OPA 2673 op-amp is selected for its wide unity gain bandwidth (Fig. 2), high slew rate (typ. 3000 V/µs) and high peak current output capability (typ. ±700 mA). One drawback of the op-amp is its low working voltage range (±6.5 V). For this reason, the power supply of the circuit board was limited to 4.5 V.

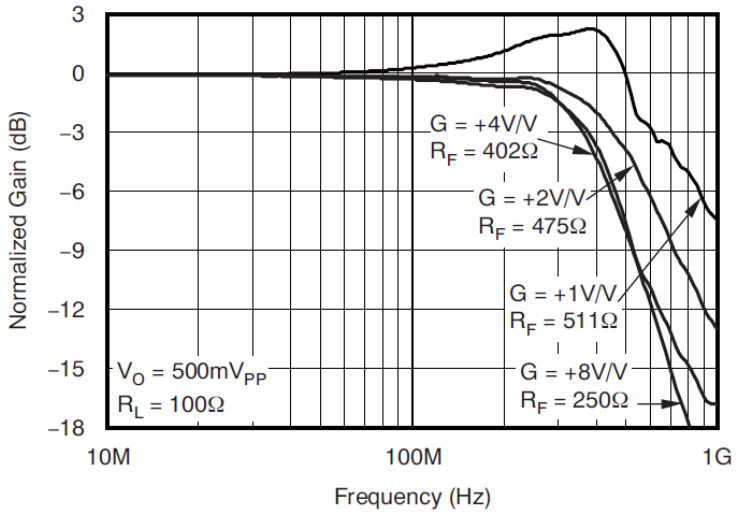

Fig. 2. OPA 2673 small signal frequency response [1].

Three 1-nF capacitors detect the average phase to 0-volt ground voltage and feed it into the op-amp. A switch S1 was included to permit the disconnection of the op-amp output from the chassis. Three 1-nF capacitors at the load represent the load-to-chassis parasitic capacitance, and three 1-nF capacitors on the board represent the parasitic capacitances of the low-side MOSFET drains to the chassis. A 3.3-nF capacitor connecting the positive DC rail to the chassis simulates the parasitic capacitances of the high-side MOSFET drains to the chassis and can also be electrically disconnected from the board using switch S2. Switches S1 and S2 are used to evaluate the effects of the high-side MOSFET parasitic capacitance and the active balancing circuitry on the phase common mode current.

B. Board layout

The circuit in Fig. 1 was implemented on a 2-layer printed circuit board. Figs. 3 and 4 show the top and bottom layers of the board respectively.

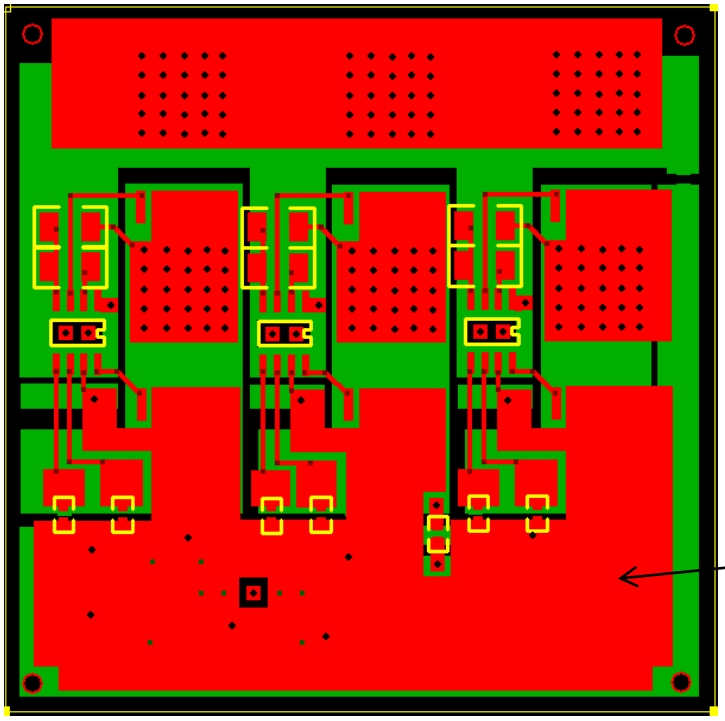

Fig. 3. Top layer of the circuit board.

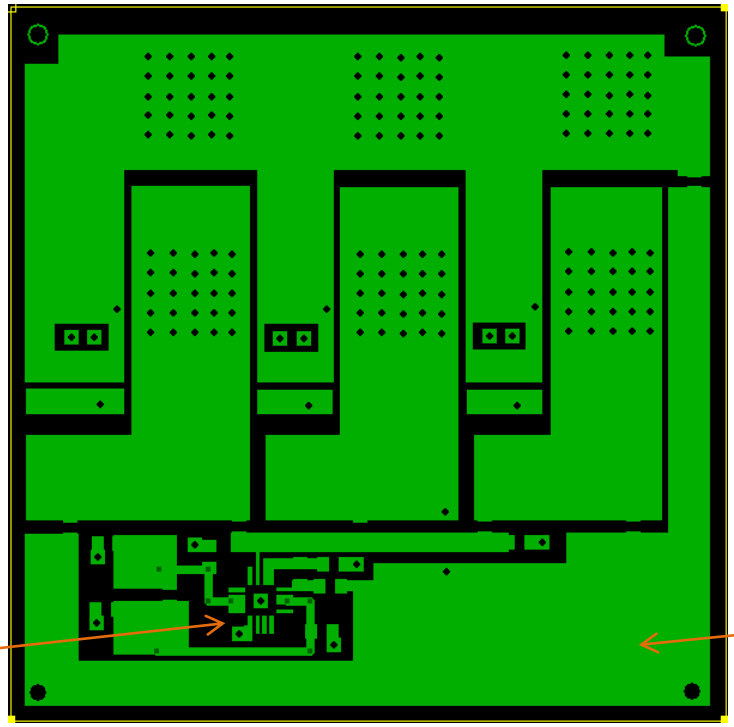

Fig. 4. Bottom layer of the circuit board.

Careful attention was paid to layout of the op-amp circuit. The distances from the power supply pins to the 0.1-µF decoupling capacitors were minimized, along with the distance from the output pin to the board chassis and distance from the input pin to the phase-voltage-detecting capacitors. For this application, only channel B of the OPA2673 was used (Fig. 5). The pin configuration is shown in Fig.5.

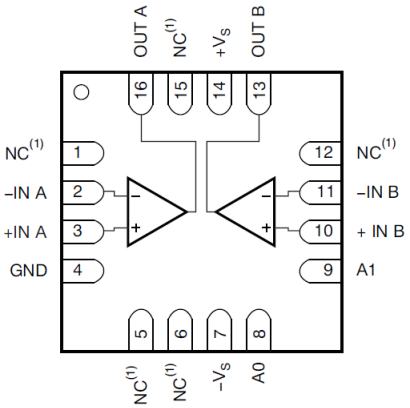

Fig. 5. OPA 2673 Pin configuration [1].

C. Fabricated Board

Figs. 6 and 7 show the fabricated board. All tests described in Section III were done using this board with switches S1 and S2 selectively open or closed.

Fig. 6. Front side of the fabricated board.

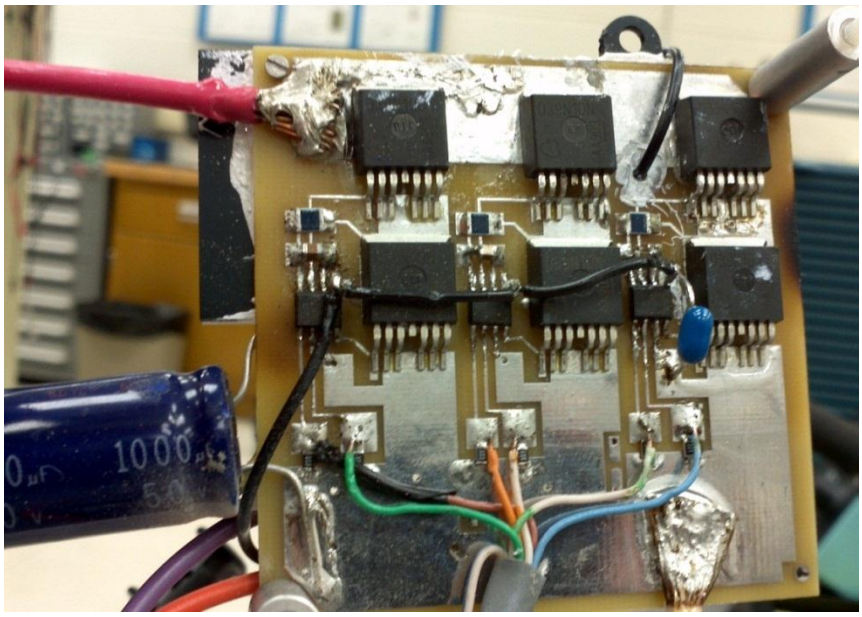

Fig. 7. Back side of the fabricated board.

D. Digital drive scheme

A microcontroller (Freescale MC9S08DZ128), which has six center aligned PWM outputs, was used to control the six MOSFETs in the circuit board. For convenience, the microcontroller was not built into the inverter circuit board. Instead, a SofTec EVB9S08DZ128 kit (Fig. 8) was used to supply the digital PWM signals to the MOSFETs. The built-in button switches on the kit were suitable for switching among different programed space vectors.

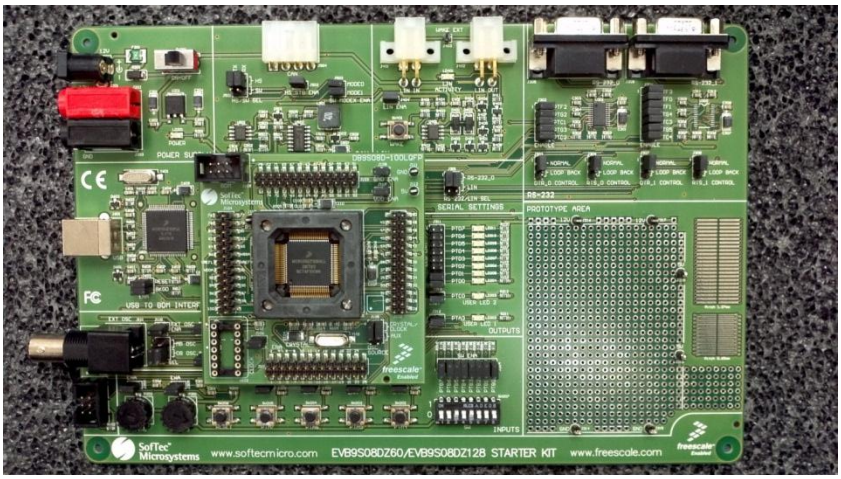

Fig. 8. SofTec EVB9S08DZ128 starter kit.

Fig. 9 show the measured phase voltages of the inverter circuit board under one of the programed drive schemes. The blue, cyan and purple curves represent Phase A, B and C to 0-volt ground voltages, respectively, and the green curve is the current in Phase A. Since the load is mainly resistive, the phase current is not as smooth as the one with motor connected. A high duty cycle was employed to achieve high phase current with a relatively low DC supply voltage.

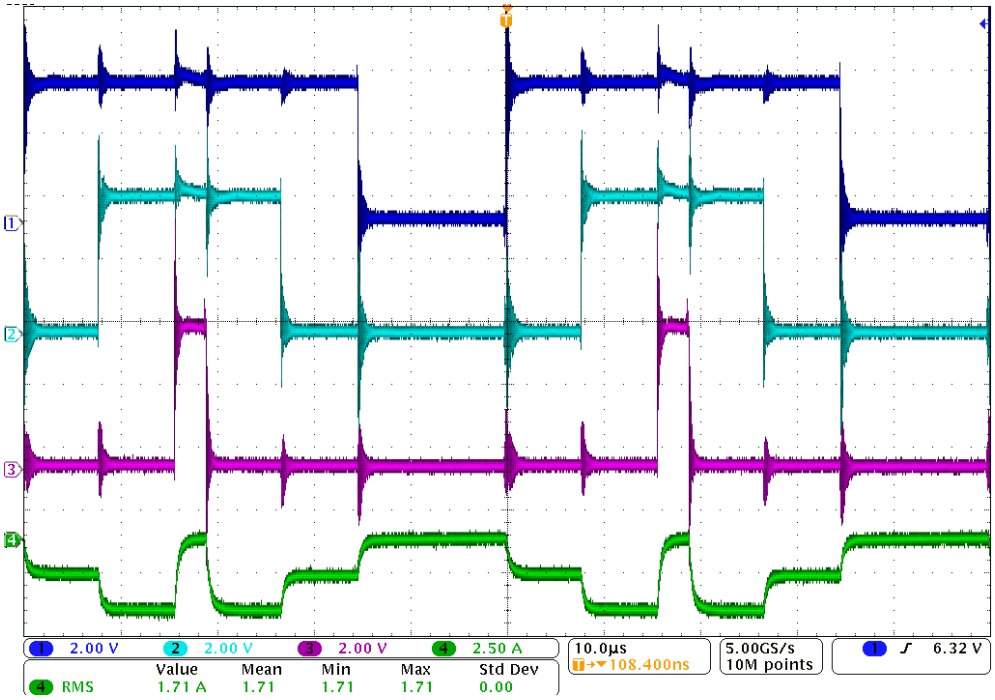

Fig. 9. Phase voltages and current

III. Measurement Results

A. Test setup

The test set up is shown in Fig. 10. Three 1-nF SMD capacitors were placed between phase wires on the load side and the copper chassis. The copper tape connects the board chassis and the load chassis to form a common chassis ground. A current probe was clamped around the three phase wires to measure the common-mode current under different conditions as described below.

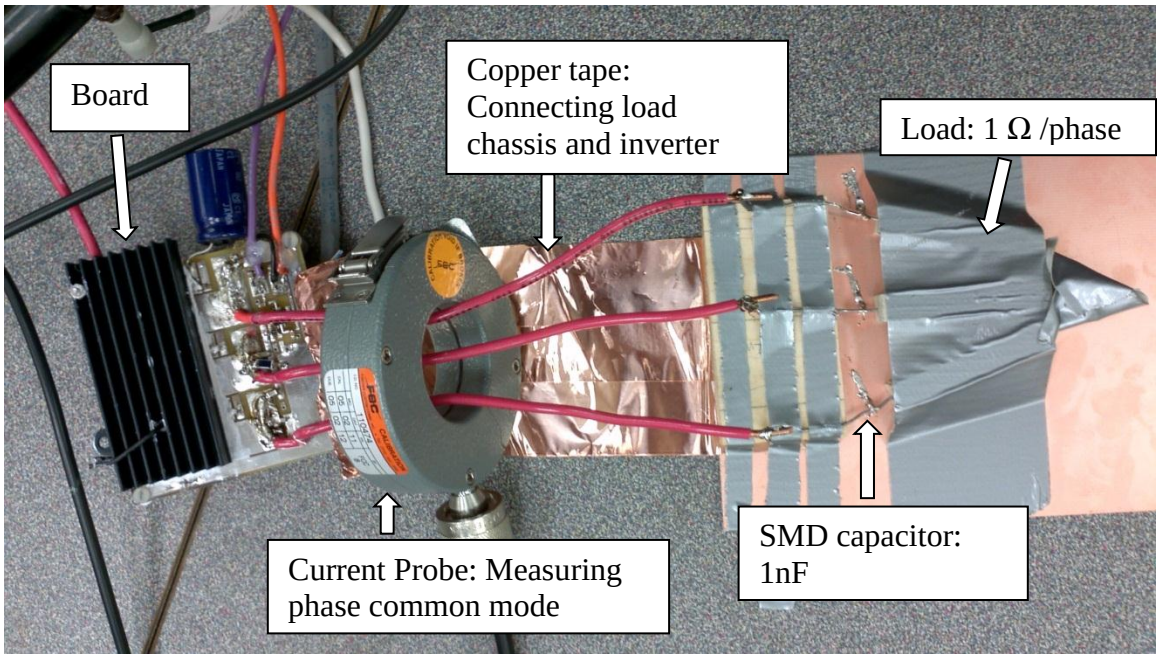

Fig. 10. Test setup.

The tests were conducted in the following sequence:

1. Measure three-phase common current with switches S1 and S2 both open.
2. Measure three-phase common current with switch S1 open and switch S2 closed.
3. Measure three-phase common current with switches S1 and S2 both closed.

Each procedure was repeated for four different programed space vectors for a fixed duty cycle. Four very similar results were obtained for the four space vector driving schemes, only the results for the driving scheme shown in Fig. 9 are reported here.

B. Test results

Figs. 11 – 16 show the common-mode current measurements obtained with the same space vector and duty cycle, but different switch settings, from10 kHz to 60 MHz.

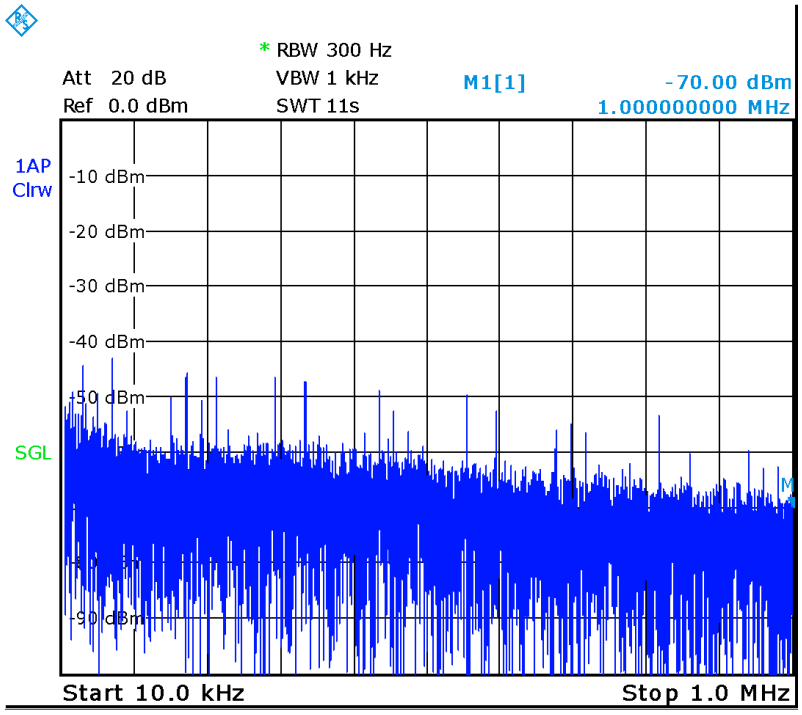

Fig. 11. Three-phase common mode current (10k – 1 MHz) with S1 and S2 open.

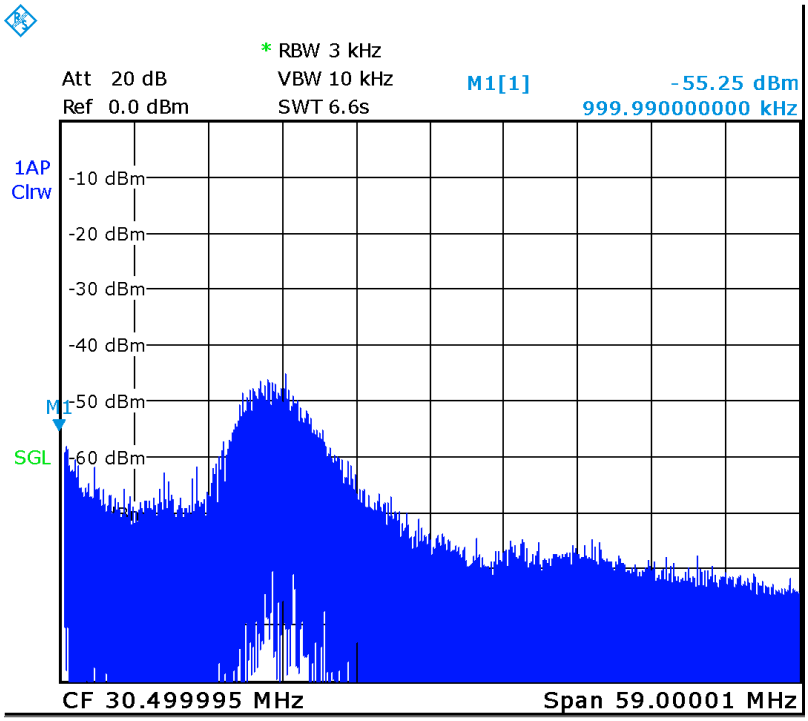

Fig. 12. Three-phase common mode current (1 – 60 MHz) with S1 and S2 open.

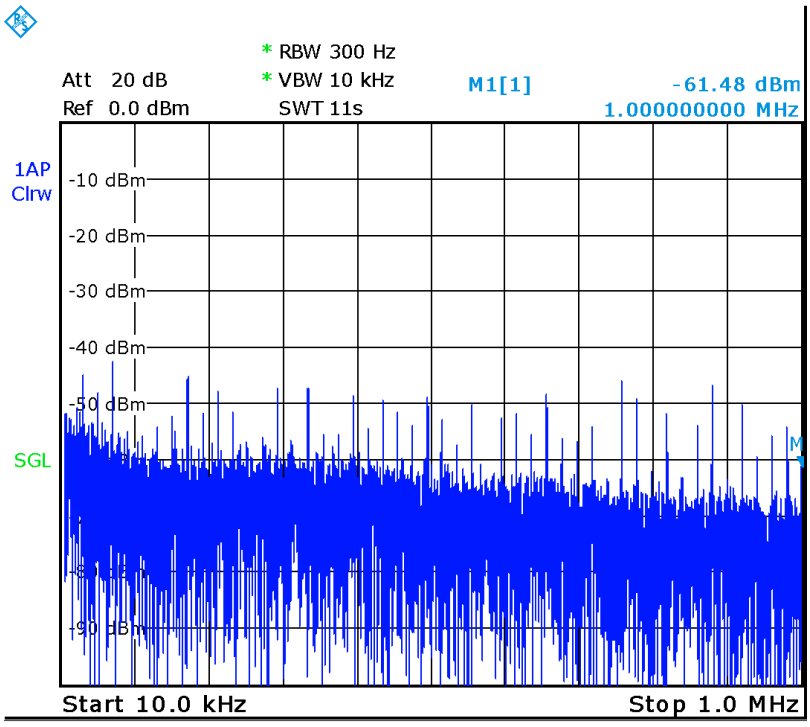

Fig. 13. Three-phase common mode current (10k – 1 MHz) with S1 open and S2 closed.

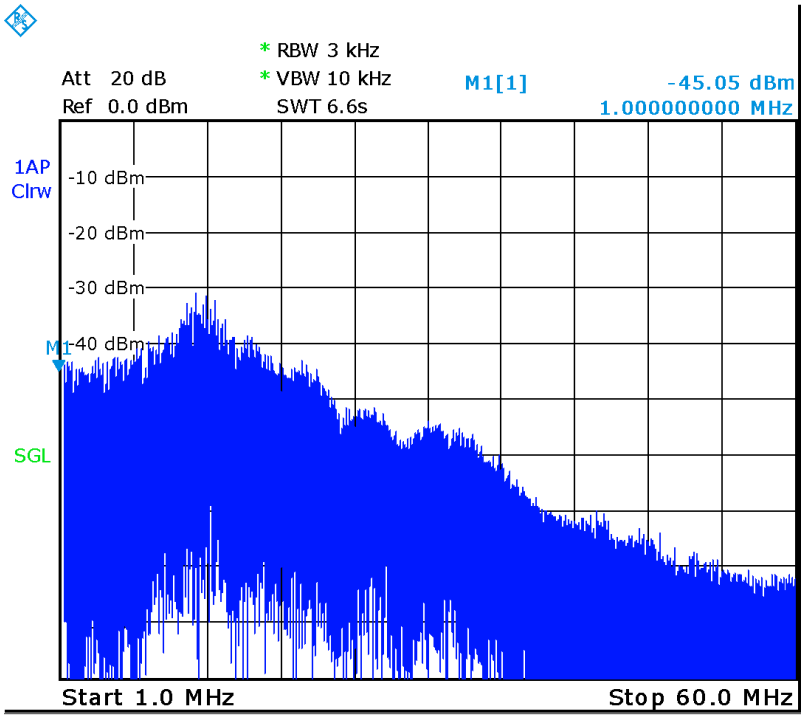

Fig. 14. Three-phase common mode current (1 – 60 MHz) with S1 open and S2 closed.

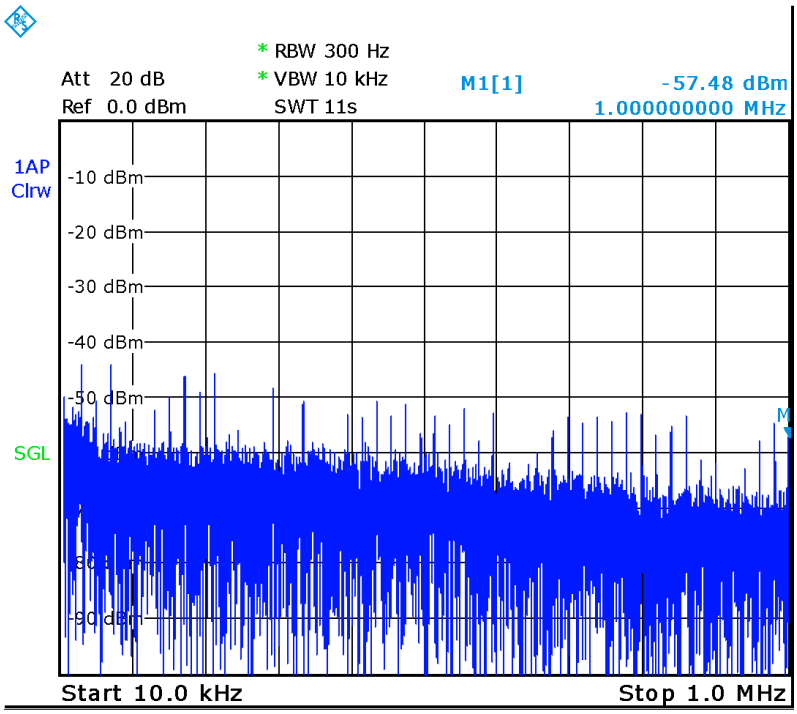

Fig. 15. Three-phase common mode current (10k – 1 MHz) with S1 and S2 closed.

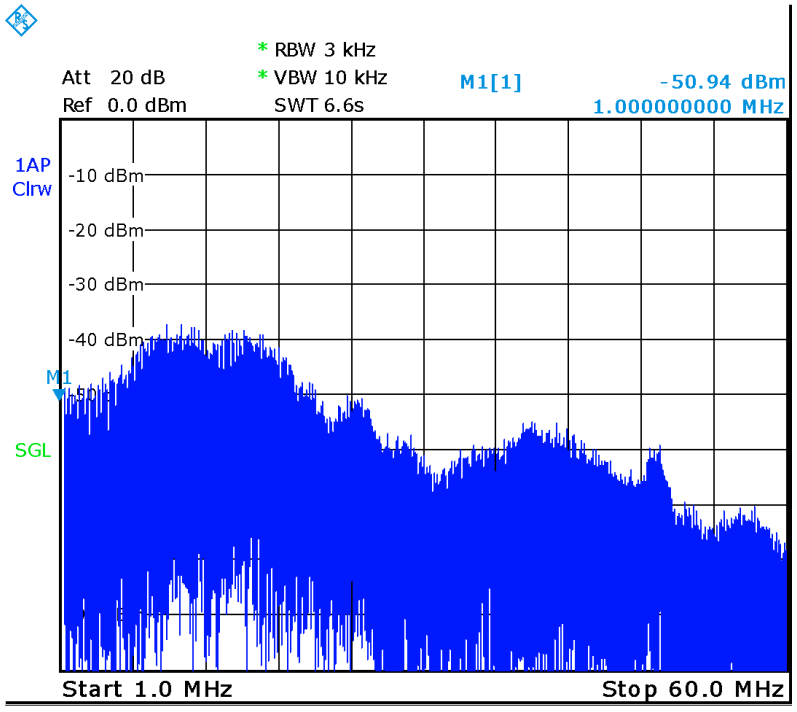

Fig. 16. Three-phase common mode current (1 – 60 MHz) with S1 and S2 closed.

IV. Results Comparison and Discussion

A. Results comparison

Figs. 11 – 16 are combined and plotted with a logarithmic frequency scale in Fig. 17.

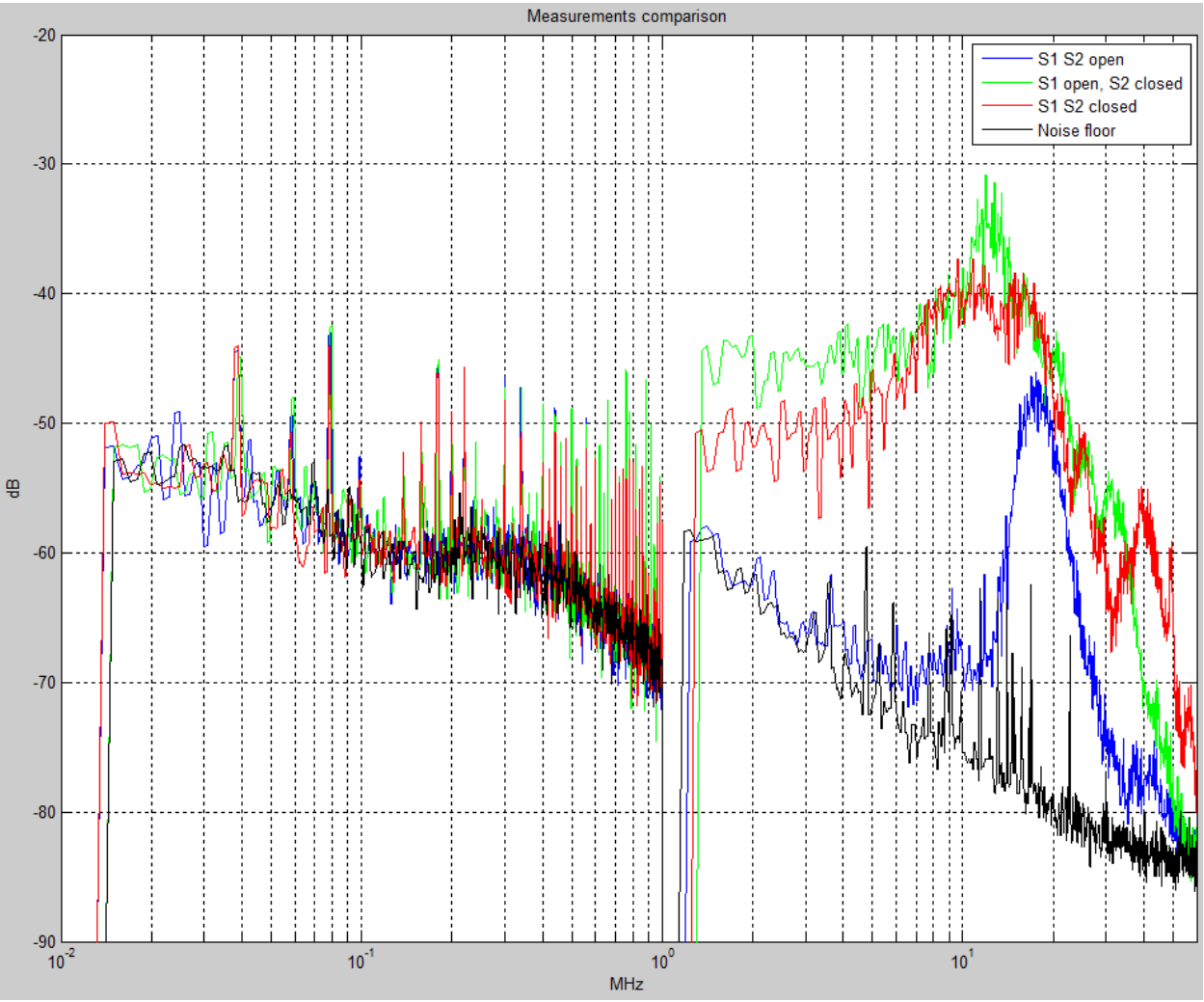

Fig. 17. Comparison of test results.

The blue, green and red curves are results from procedures 1, 2 and 3 described in Section III, respectively. The black curve is the noise floor of the spectrum analyzer.

B. Discussion

The blue curve in Fig. 17 exhibits the lowest common-mode current. It is obtained under the condition that there is no parasitic capacitance from the high-side MOSFET to the board chassis. This is the ideal situation as discussed in a previous technical report [2].

As soon as the parasitic capacitance was introduced by closing switch S2, the common-mode current increased tremendously as indicated by the green curve in Fig. 17. This is the current situation in the CA6 inverter [2].

After applying the active balancing circuit by closing switch S1, the common-mode current below 20 MHz is reduced as much as 10 dB at the peak (red curve in Fig. 17). However above 20 MHz, the active balancing circuit makes the noise worse. This is a problem which should be relatively easy to fix by filtering the op-amp input.

V. Summary

An active balancing circuit for a three-phase motor driver was designed to suppress the phase common-mode current. It actively compensates for the inherent imbalance caused by the SVPWM driving scheme by driving the 0-volt ground on the circuit board relative to the board chassis. A test circuit was constructed, tested and analyzed to demonstrate the effectiveness of the active balancing circuit. Results show as much as a 10-dB reduction in the common-mode current peaks between 10 kHz and 20 MHz.

REFERENCES

[1] "OPA2673 datasheet", Texas Instruments.

[2] C. Zhu, A. McDowell and T. Hubing, "EMI Source Modeling of the John Deere CA6 Motor Driver", Clemson Vehicular Electronics Laboratory Technical Report # CVEL-11-029, October 1, 2011.