CVEL

THE CLEMSON UNIVERSITY VEHICULAR ELECTRONICS LABORATORY

TECHNICAL REPORT: CVEL-13-041

Preliminary Investigation of the Current Path and Circuit Parameters Associated with the Characteristic Ringing in a MOSFET Power Inverter

J. Hunter Hayes and Dr. Todd Hubing

Clemson University

January 16, 2013

Table of Contents

1. Characteristics of Series RLC Circuits

The characteristics of a series RLC circuit of the type shown in Fig. 1 are well known [1,2].

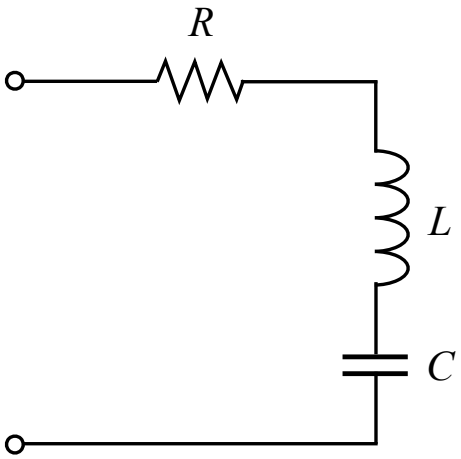

Fig. 1. Series RLC Circuit

For a given series RLC circuit, the exponential decay rate, α, can be found by

$$\alpha = \frac{R}{2L}. \tag{1}$$

This parameter is a measure of how quickly the ringing of an impulse dies out. It is closely related to the damping factor,

$$\zeta = \frac{\alpha}{2\pi f_0} = \frac{R}{2}\sqrt{\frac{C}{L}}. \tag{2}$$

The damping factor helps determine the damping characteristics of the ringing, i.e., whether the ringing is under-, over-, or critically-damped. Likewise, the frequency at which the ringing will occur is given by

$$f_0 = \frac{1}{2\pi\sqrt{LC}}. \tag{3}$$

These parameters can be combined to create the quality factor, Q, of the RLC circuit:

$$Q = \frac{1}{R}\sqrt{\frac{L}{C}} = \frac{1}{2\zeta} = \frac{\pi f_0}{\alpha}. \tag{4}$$

The Q factor of a circuit roughly corresponds to the number of observable peaks before the ringing falls below 5% of its initial peak value [1].

2. MOSFET Equivalent Circuit Model

From [3] and [4], the equivalent circuit of a MOSFET transistor is shown in Fig. 2. In order to examine the validity of the Matrix Pencil Method to detect shifts in the poles of a transistor due to aging, the circuit in Fig. 3 was designed and constructed. The gate of the low-side MOSFET is tied low, while the gate of the high-side MOSFET is driven by a PWM signal.

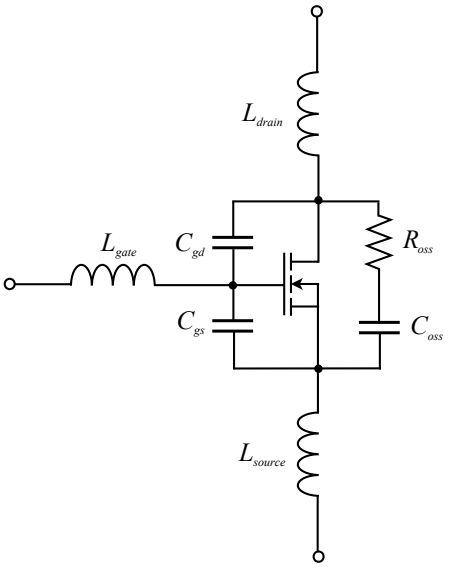

Fig. 2. Equivalent circuit of a MOSFET

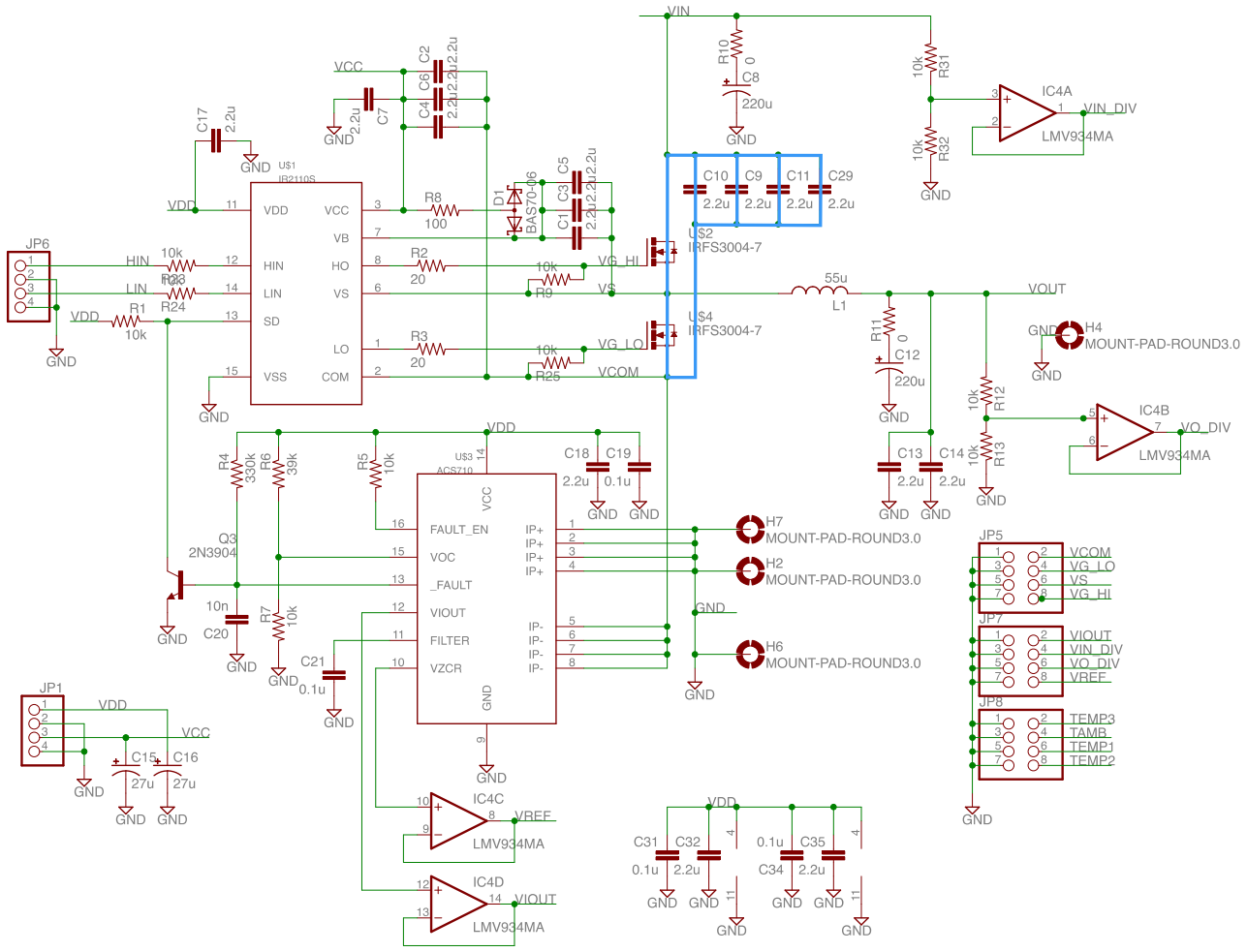

Fig. 3. MOSFET test circuit for the evaluation of the MPM

Through careful analysis of the constructed circuit, it has been determined that the vast majority of the ringing current flows along the path highlighted in blue on Fig. 3. In Fig. 4, which shows the top and bottom layouts of the board, the current flowing on the top side of the board is marked in red, while the current flowing on the bottom side is marked in blue. Note that these lines are only a rough guide and that the actual ringing current will spread out along pads and go through multiple vias.

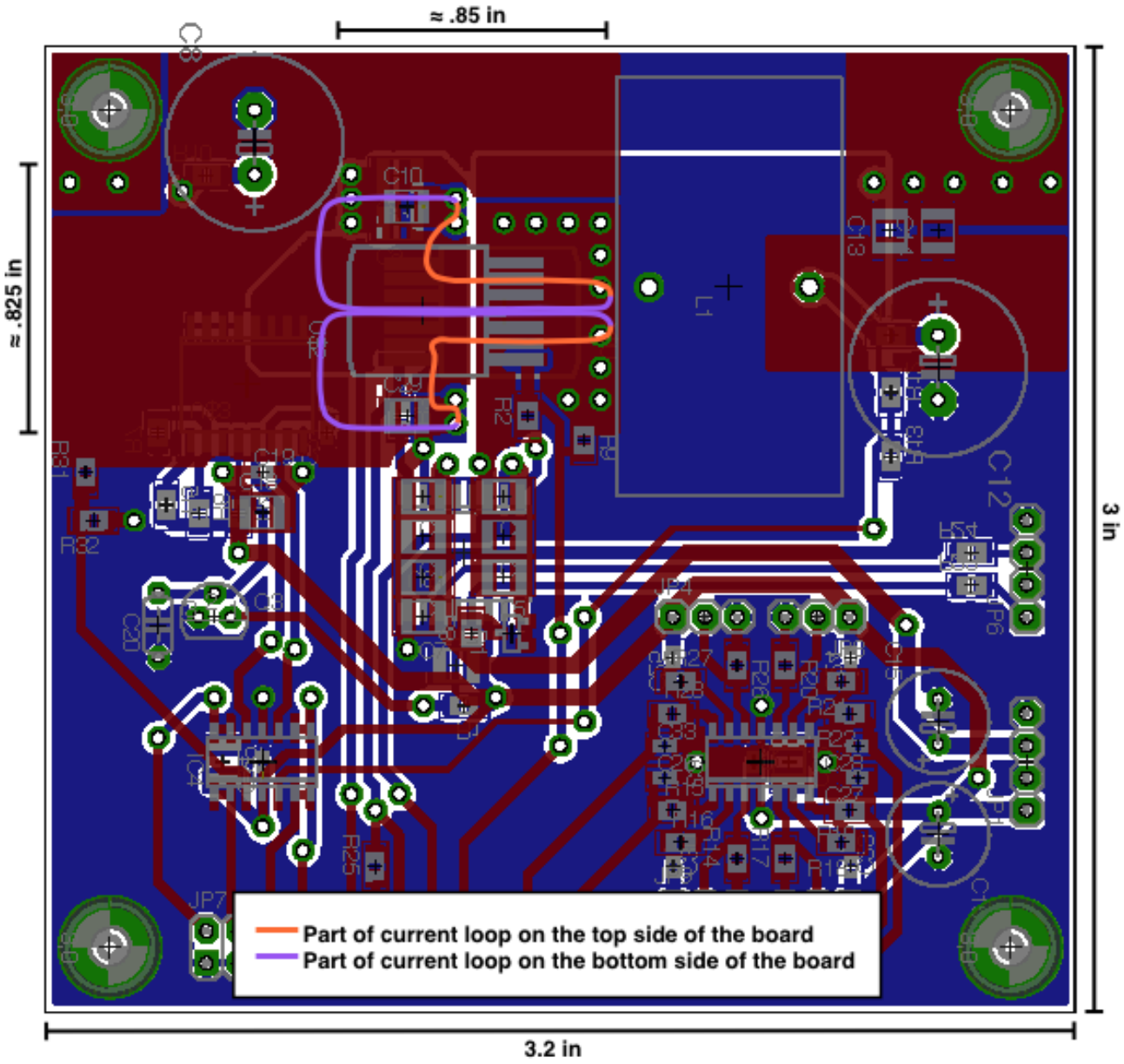

Fig. 4. Layout of MOSFET test circuit with current path highlighted

Note that capacitors C8 and C9, though not visible in Fig. 4, are located immediately under C10. At high frequencies (e.g. above 1 MHz), current tends to flow through the path of least inductance rather than the path of least resistance. From Fig. 4, it is obvious that the closest paths, those with the least amount of inductance, are the paths that include C8, C9, C10, and C29.

From analysis of the MOSFET equivalent circuit in Fig. 2 and the schematic and layout of the MOSFET test circuit in Fig. 3 and Fig. 4, an equivalent circuit model of the ringing current loop,

shown in Fig. 5, is proposed in order to accurately describe the ringing behavior of the MOSFET test circuit. Note that this equivalent circuit is valid only for ringing on the high-to-low transition of the output voltage, with both the high- and low-side MOSFET transistors in switched-off states. For analysis of ringing that occurs on the low-to-high transition, the low-side MOSFET may be modeled in the same manner, while the high-side MOSFET may be modeled as simply $R_{DS(ON)}$. The inductances of the drain and source of both MOSFETs have been lumped together with the total loop inductance of the circuit, L_{LOOP}.

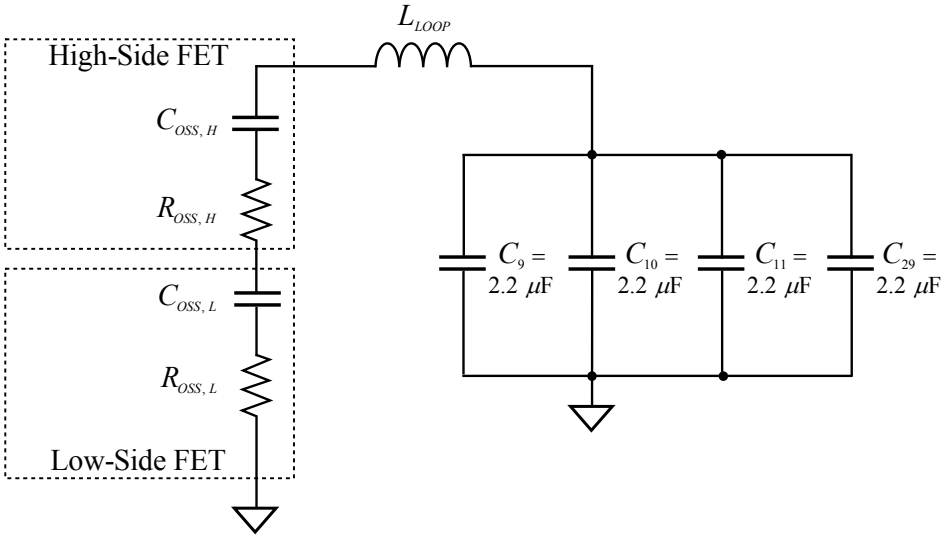

Fig. 5. Equivalent circuit of MOSFET test circuit ringing current loop

3. Measurement of C_{OSS}

With a known ringing frequency and exponential decay rate, the total loop resistance and inductance can be calculated if the capacitance of the circuit is known. This then allows the R_{OSS} of each transistor to be determined as well as L_{LOOP}. To determine the total capacitance of the circuit, the C_{OSS} of each transistor must be measured. Since C_{OSS} depends on the drain-to-source bias voltage, it must be measured at the bias points of both the high- and low-side transistors. The DC drain-to-source voltage of each transistor was measured under operating conditions and was found to be approximately 3.08 V for the high-side MOSFET, and approximately 2.28 V for the low-side MOSFET. Next, C_{OSS} at each bias voltage was measured using the setup found in Fig. 6

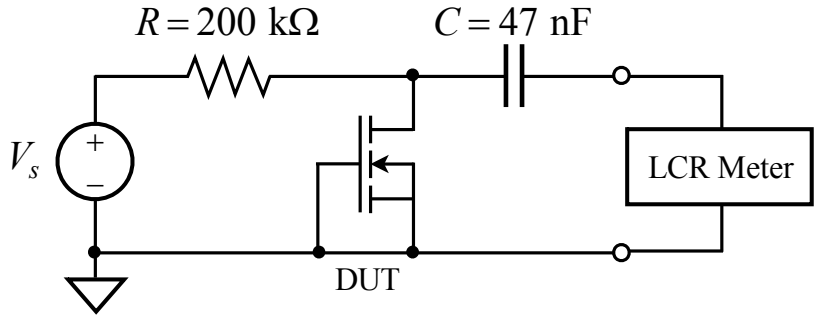

Fig. 6. Setup for measuring C_{OSS}

The 200-kΩ resistor between the voltage source and the transistor in Fig. 6 was used to ensure that the voltage source did not interfere with the capacitance measurements of the LCR meter. It allowed the meter to measure the capacitance of the transistor rather than that of the source. The 47-nF capacitor in series with the LCR meter was used as protection to block the DC biasing voltage from the meter. Once the capacitance of the circuit was measured at the proper DC bias voltages, C_{OSS} was calculated from

$$C_{OSS} = \left[\frac{1}{C_{MEAS}} - \frac{1}{47\ \text{nF}} \right]^{-1} \tag{5}$$

to account for the fact that C_{OSS} was measured in series with the 47-nF capacitor. A table of the capacitances resulting from this measurement can be found in Table 1.

Table 1 – C_{OSS} Measurements

Transistor	V_{DS}	C_{MEAS}	C_{OSS}
Low-Side MOSFET	3.08 V	7.2 nF	8.5 nF
High-Side MOSFET	2.28 V	7.4 nF	8.8 nF

4. Final Equivalent Circuit Model

The final equivalent model of the ringing present in the circuit of Fig. 3 is shown below in Fig. 7.

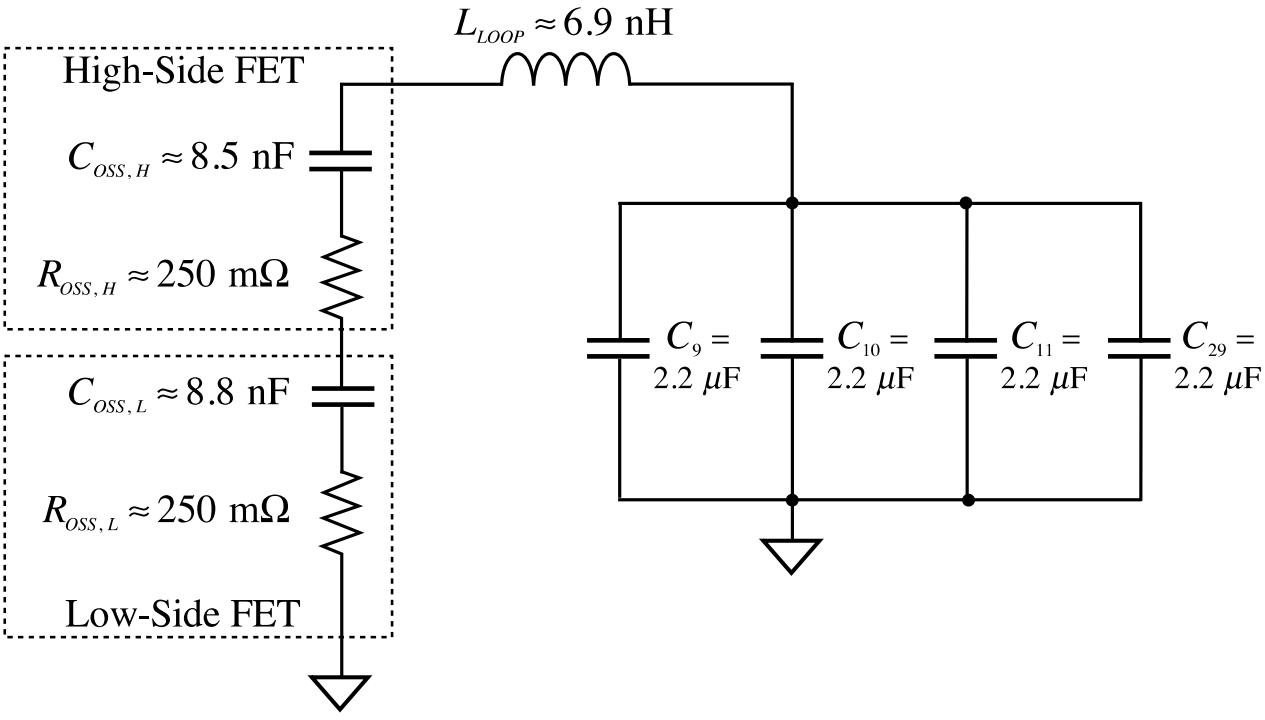

Fig. 7. Equivalent circuit of MOSFET test circuit ringing current loop

This circuit can be simplified to the series RLC circuit shown in Fig. 8 in order to more easily examine the properties of the ringing it produces.

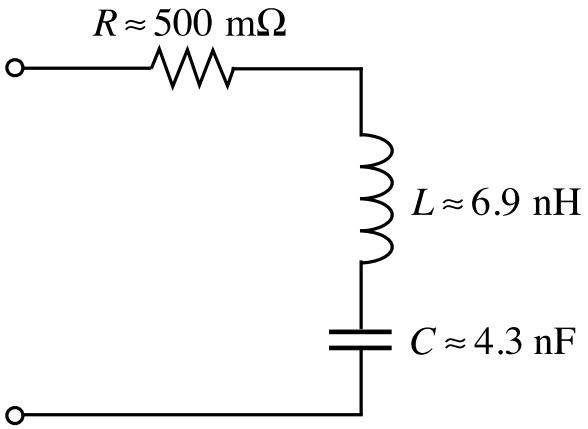

Fig. 8. Simplified circuit of MOSFET test circuit for ringing analysis

Given the equivalent circuit parameters in Fig. 8 and Eqns. (1)-(4), the characteristics of the ringing this circuit produces are

$$\alpha = \frac{R}{2L} = \frac{500\ \text{m}\Omega}{2 \cdot 6.9\ \text{nH}} \cong 36\ \ {}^{\text{Np}}\!/\!_{\mu\text{s}}$$

$$f_0 = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{(6.9\ \text{nH}) \cdot (4.3\ \text{nF})}} \cong 29\ \text{MHz}\ ,$$

$$Q = \frac{1}{R}\sqrt{\frac{L}{C}} = \frac{1}{500\ \text{m}\Omega}\sqrt{\frac{6.9\ \text{nH}}{4.3\ \text{nF}}} \cong 2.5$$

which are consistent with the results obtained by the Matrix Pencil Method.

5. Validation of Series RLC Circuit Model for MOSFET Test Circuit

To validate the series RLC model of the MOSFET test circuit, shown in Fig. 5, a simple experiment was performed. First, C29 was removed. This was expected to increase the inductance of the loop by forcing more current to go through C8, C9, and C10. Next, C8, C9, and C10 were removed, leaving none of the four decoupling capacitors. Similarly, this was expected to increase the inductance of the current loop by causing the ringing current to now have to travel along a much larger loop in order to return to its point of origin. By estimating that removing all four decoupling capacitors would increase the loop inductance by a factor of 2, α and f_0 were both expected to decrease by a factor of ${}^{1}\!/\!_{\sqrt{2}}$. This was very nearly the case. Fig. 6 demonstrates that removing all four decoupling capacitors increased the inductance by a factor of roughly 3.25.

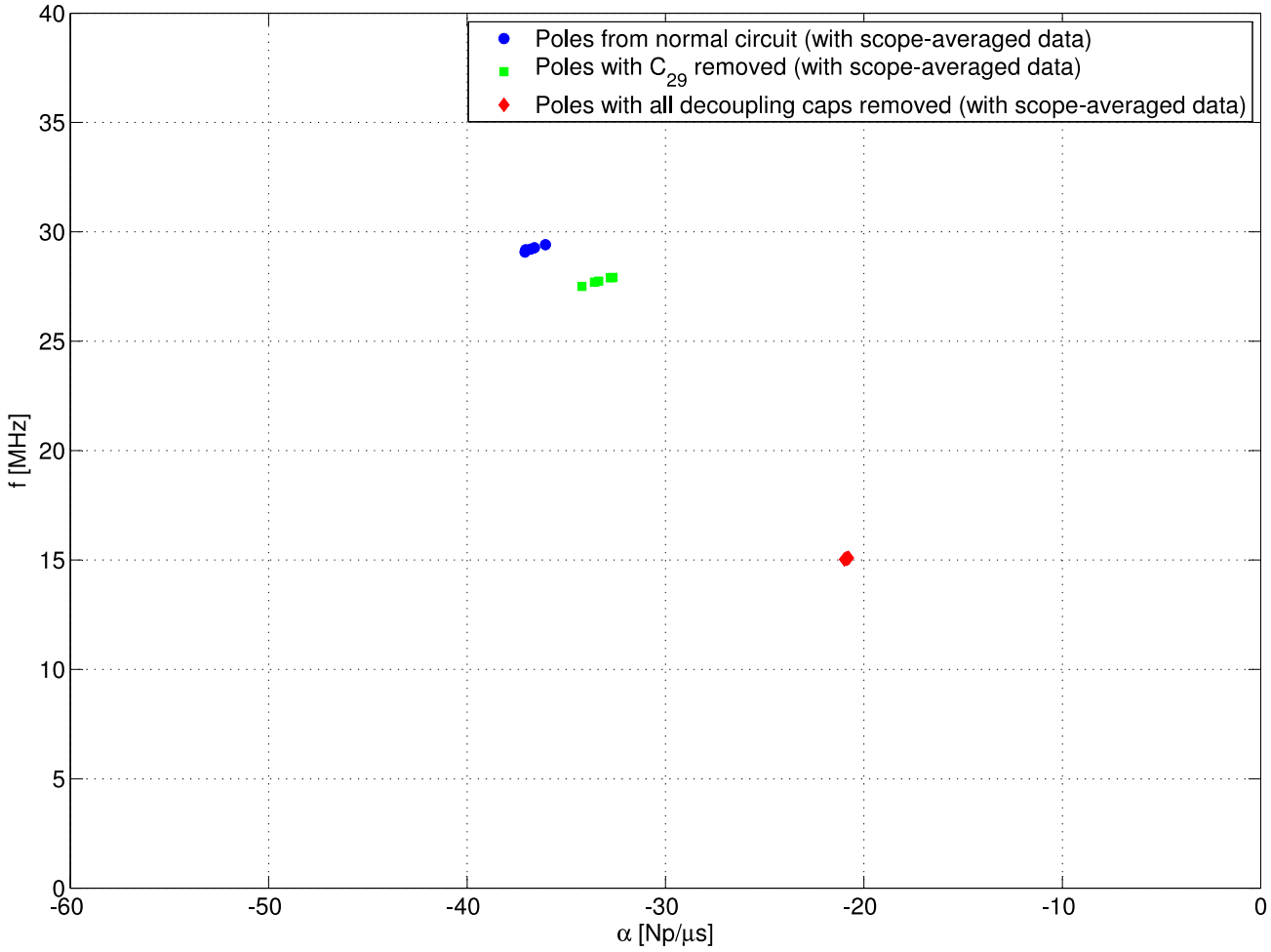

Fig. 6. Matrix Pencil Method pole plots with varying numbers of decoupling capacitors

References

[1] C. Zhu and T. Hubing, "Q-Factor and Resonance in the Time and Frequency Domain," *Clemson Vehicular Electronics Laboratory Technical Report: CVEL-11-028*, Oct. 1, 2011.

[2] "RLC Circuit," *Wikipedia*, http://en.wikipedia.org/wiki/RLC_circuit

[3] K. Kam, et al., "Analysis and Mitigation Techniques for Broadband EMI from Synchronous Buck Converter," *IEEE EMC Magazine*, vol. 1, no. 3, 2012.

[4] K. Kam et al., "Quantification of Self-Damping of Power MOSFET in a Synchronous Buck Converter," *IEEE Trans. on EMC*, vol. 53, no. 4, pp. 1091-1093, Nov. 2011.