

## **TECHNICAL REPORT: CVEL-13-048**

### **High-Voltage Pulse Testing of Multi-layer Ceramic Capacitors**

D. Zhang and T. Hubing

Clemson University

February 15, 2014

---

---

## Table of Contents

Abstract.....	3
1. Introduction.....	3
2. Experiment.....	4
2.1 Test setup and test procedures .....	4
2.2 Test samples and test intensities .....	6
3. Results and Discussion .....	6
3.1 Summary .....	6
3.2 Voltage waveforms .....	8
3.3 Failure voltage.....	10
3.4 Degradation and recovery of post-failure resistance.....	15
3.5 Degradation of capacitance.....	18
4. Conclusion .....	19
References.....	19



---

## Abstract

This report investigates the susceptibility of multi-layer ceramic (MLC) capacitors to high-voltage electrical fast transients (EFTs). Both X7R and NPO MLC capacitors with a 50-V voltage rating and 0603 package size were tested. X7R capacitors often failed during a spike in the voltage, but exhibited no obvious degradation in measured insulation resistance immediately after the failure event. NPO capacitors usually failed by suddenly shorting and maintained the short after the failure. With time or the application of additional voltage spikes, some X7R capacitors exhibited a full recovery, returning to their initial state.

## 1. Introduction

The multi-layer ceramic (MLC) capacitor is widely used in automotive applications due to its low cost and small size. It often serves as an input/output component thus exposing it to a high risk of electrical overstress.

Traditional failure analysis of MLC capacitors focuses on pre-testing and post-failure analysis. These studies have helped people to better understand the characteristics of MLCCs and have helped to guide the manufacturing process. However, very few studies have focused on the analysis of capacitor failures that may go unnoticed during the normal operation of a system. Undetected capacitor failures in safety-critical or mission-critical systems can have serious consequences. Therefore, it is important to understand how different types of capacitors are likely to fail, and the electrical behavior that these capacitors are likely to exhibit after a failure.

Two failure modes of an MLC capacitor are low insulation resistance and degraded capacitance. Low insulation resistance, typically due to shorting between the capacitor plates, is the most common failure mode. Failures of insulation resistance can be categorized into two groups: near short circuits or simply degraded insulation resistance. A degradation in the insulation resistance might go undetected, but could affect the performance of the system. Both of low insulation resistance and degraded capacitance can be caused by electrical overstress.

Traditionally, the long-term reliability and failure analysis of ceramic capacitors has been based on highly accelerated life testing (HALT). Capacitors were tested in a high-humidity and high-temperature environment with an applied DC voltage. These tests have been used to predict the usable life of capacitors and to establish de-rating rules. In [1], DC voltages as high as 400 V were applied to 50-V capacitors during HALT testing to reduce the qualification time. In these tests, a capacitor was considered to have failed if its leakage current exceeded 100  $\mu$ A.

The study in [2] demonstrated that X7R capacitors exposed to electrostatic discharge can exhibit a non-linear resistance in parallel with the capacitance. Capacitance degradation due to ESD was also observed in [3].

Failures due to electrical fast transients (EFTs) have also been the subject of intense study. These studies can be classified into two groups. In [4], [5] and [6], under-damped series R-L-C circuits were used to study capacitor failures due to transients caused by step-up voltages. In [4], 50-V rated Z5U barium titanate capacitors were found to fail with a step voltage between 250-275 V. The peak failure voltage caused by the ringing of the circuit was 900-950 V, which was more than twice the step voltage due to the voltage dependence of the capacitance. According to the study, these capacitors had a static breakdown voltage between 1030-1100 V. The peak current observed during a failure was 26 A. The failed capacitors behaved like a short circuit, which lead to a catastrophic failure in the presence of the DC voltage. In [5], low-voltage step-up pulses were applied to NPO, X7R and Z5U capacitors. The step voltage across a 0.1- $\mu$ F capacitor was 4 V and the current was about 0.75 A. Each

capacitor was subjected to about 3.6 billion pulses during a 1-hour test and no insulation resistance failure was observed. In [6], a surge step stress test (SSST) was used to investigate failure modes in capacitors of different types including 6.3-V rated MLC capacitors. The 100-ppm failure step-up voltage derived from a 2-parameter Weibull fitting method for these capacitors were 10 to 19 times the rated voltage.

Another group of tests employed R-C circuits to study the failure of capacitors exposed to voltage surges. In [7], a 100- $\mu$ sec high-voltage single pulse was applied to capacitors with a resistor limiting the current. The voltage across the capacitor increased linearly until the breakdown was reached. The voltage then dropped to a low sustained value, which implied that the capacitor had not failed as a short circuit. It was found that there was little correlation between the rated voltage and the breakdown voltage. In [8], a similar R-C circuit was used to test the current surge susceptibility of MLC capacitors. Sectioned and polished capacitors with exposed internal structures were tested. The capacitors had a rated voltage of 50 V and capacitances of 0.1  $\mu$ F and 0.33  $\mu$ F. A series of 125-V pulses was applied with a maximum peak current of 1 A. A degradation of insulation resistance (by approximately a factor of 10) was observed during the test. Unlike [7], the paper described the failure mechanism as the heat-induced local melting of internal electrodes.

The study described in this report focuses on characterizing MLC capacitors under electrical overstress (EOS) induced by an LC oscillating circuit. The capacitance and the insulation resistance of the capacitors were recorded after each electrical pulse was applied.

## 2. Experiment

### 2.1 Test setup and test procedures

The test setup in Fig. 1 was used to apply high-voltage pulses across MLC capacitors while monitoring the applied voltage waveform and then measuring the resistance and capacitance of the test capacitor. The test bench includes a laptop which controls and coordinates the other test equipment. An LCR meter (B&K Precision 879B) is used to measure the capacitor parameters. The oscilloscope and high-voltage differential probe record the voltage across the test capacitor. The test equipment connects to the test circuit shown in Fig. 2.

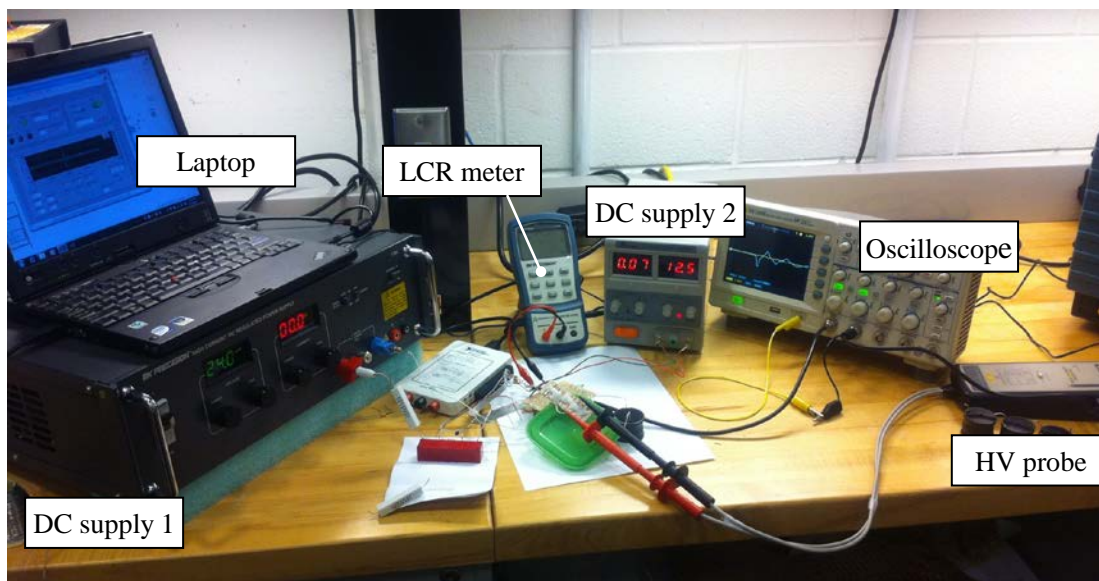


Fig. 1. High-voltage pulse test setup.

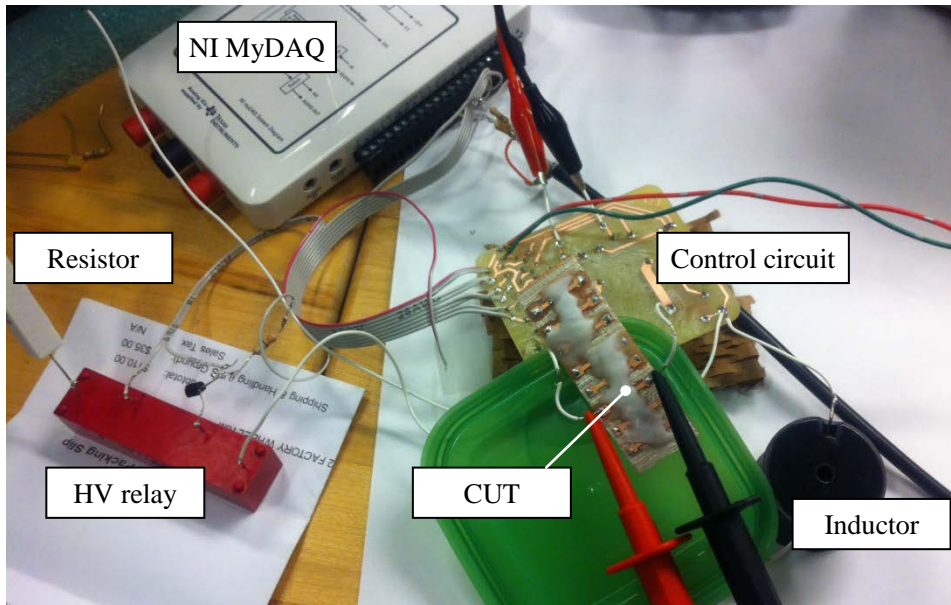


Fig. 2. High AC voltage pulse test circuit.

A schematic of the test circuit is provided in Fig. 3 (not including relay control circuits). During the test, an NI MyDAQ switches on the high-voltage (HV) relay to establish a steady-state current in the inductor and then switches off the relay. The initial current in the inductor induces an oscillation in the LC circuit. Thus, an adjustable high AC voltage can be applied to the capacitor by adjusting the initial current through the inductor. The frequency of the pulsed voltage is determined by the value of the inductor and the capacitor being tested.

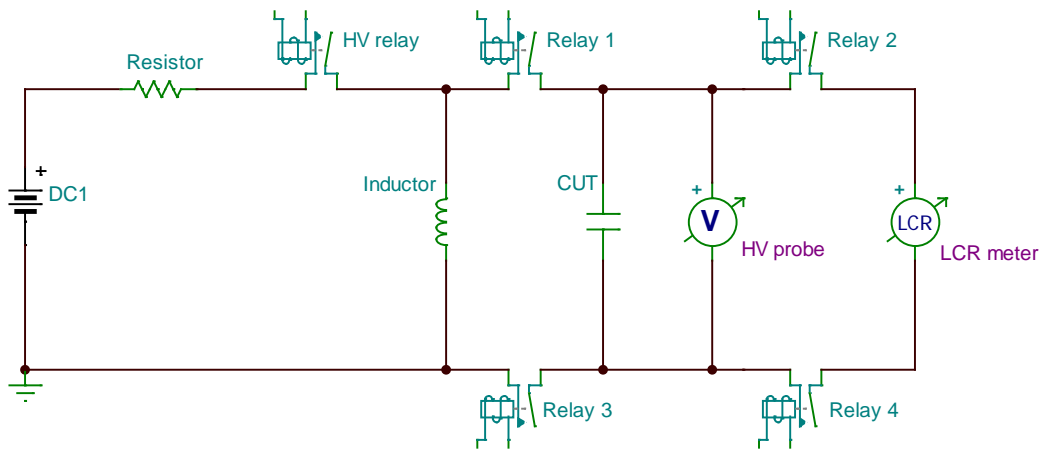


Fig. 3. Schematic of the test circuit.

As indicated in Fig. 3, the initial current in the inductor is regulated by the resistor and the voltage of the DC1 supply. During the test, Relay 1 and Relay 3 are always turned on, and Relay 2 and Relay 4 are turned off. After the voltage across the capacitor has died down to an insignificant level, Relay 1 and Relay 3 are turned off, and Relay 2 and Relay 4 are turned on. This allows the parameters of the capacitor to be measured by the LCR meter. The measured capacitance and resistance incorporate the

impedance of the high-voltage probe as well. According to the nominal specification of the probe (Probe Master 4241A), it has the impedance of a 10-pF capacitance in parallel with a 50-M $\Omega$  resistance to ground for each input. Relative to the capacitance and the AC resistance of the capacitor-under-test, the impedances of the probe can be neglected. LabVIEW software running on the laptop repeats the test approximately every 10 seconds. The program also controls the LCR meter and the oscilloscope as indicated in Fig. 4.

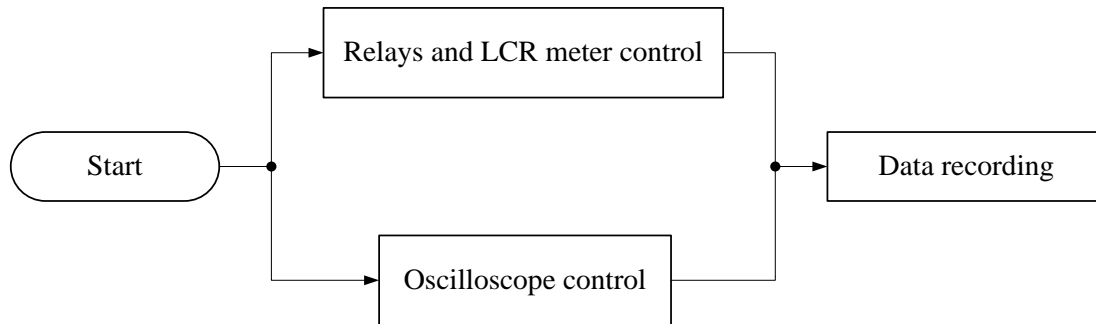


Fig. 4. LabVIEW software control blocks.

## 2.2 Test samples and test intensities

Both X7R and NPO capacitors were evaluated. The X7R capacitors were manufactured by AVX and had nominal values of 1 nF, 10 nF or 100 nF. The NPO capacitors were manufactured by TDK and had a nominal value of 10 nF. Both types of capacitors had a voltage rating of 50 V and a 0603 package size. The initial current in the inductor was adjusted by changing the voltage of the DC1 supply for a given resistor value. The initial current was adjusted to provide just enough energy to cause the capacitor to fail after tens of pulses. To determine this initial current value, a trial test was performed for each capacitor of a given type. The test results for these trial capacitors are also included in the report.

## 3. Results and Discussion

### 3.1 Summary

The test samples included 25 10-nF X7R capacitors, 2 100-nF X7R capacitors, 2 1-nF X7R capacitors, and 25 10-nF NPO capacitors. Table 1 lists the test capacitors and the circuit parameters of each test. The measured parameters associated with each failure event and the post-failure resistance and capacitance of the capacitor-under-test are also listed in the table.  $R_{\min}$  is the minimum insulation AC resistance measured during the test and  $R_{\text{parallel}}$  is the AC insulation resistance measured after the capacitor failed. No failure voltages or post-failure resistances were recorded if the capacitor did not fail or if the failure was not recorded. Some of the post-failure capacitances are not listed, because the capacitors failed with a very low parallel resistance making the measurement of the capacitance inaccurate. Failure events were identified when the resistance measured after the pulse was lower than 1/10th of the initial resistance, or an oscillating voltage across the capacitor could not be established during successive pulses. Initial currents were calculated by dividing the voltage of DC1 supply by the resistance of the regulating resistor.

Table 1: Test configurations and results

Number	Nominal Capacitance [nF]	Test Inductor [H]	Regulating Resistor [ $\Omega$ ]	DC1 Supply [V]	Failure count	$V_{\text{peak}}$ at failure event [kV]	$R_{\text{parallel}}$ after failure event [ $\Omega$ ]	$R_{\text{min}}$ in parallel with CUT [ $\Omega$ ]	$C_{\text{min}}$ of CUT [nF]
X7R-1	10	18.7 m	56	15	963	0.8	59.2 k	2.2	8.6
X7R-2	10	18.7 m	56	15	2425	0.8	1070 k	5.7	_***
X7R-3	10	18.7 m	56	15	1190	0.8	1300 k	13	_***
X7R-4	10	18.7 m	56	15	1327	0.94	1210 k	21	_***
X7R-5	10	18.7 m	56	15	4191	0.976	370 k	7.8	_***
X7R-6	10	18.7 m	56	15	8292	0.96	34.7 k	4.4	_***
X7R-7	10	18.7 m	56	15	8827	0.928	1400 k	12	_***
X7R-8	10	18.7 m	56	15	513	0.656	1170 k	7.2	_***
X7R-9	10	18.7 m	56	15	3726	0.96	823 k	2.8	_***
X7R-10	10	18.7 m	56	15	385	0.944	1100 k	87	8.2
X7R-11*	10	1.84 m	20	15	-	-	-	965 k	9.4
X7R-12**	10	1.84 m	20	15	-	-	-	1.13 k	6.8
X7R-13	10	1.84 m	20	15	9683	0.944	1340 k	321	4.7
X7R-14*	10	820 $\mu$	20	24	-	-	-	996 k	7.8
X7R-15	10	820 $\mu$	20	30	3	0.976	988 k	180	9.1
X7R-16	10	820 $\mu$	20	25	21	0.976	47 k	90	8.7
X7R-17**	10	820 $\mu$	20	24.2	-	-	-	2.36 k	8.0
X7R-18	10	820 $\mu$	20	24.2	334	0.704	492 k	230	0.24
X7R-19	10	166 $\mu$	6.8	13.6	1	0.96	12.7 k	489	9.7
X7R-20	10	166 $\mu$	6.8	13.6	43	0.96	1040 k	151 k	9.2
X7R-21	10	166 $\mu$	6.8	13.6	352	0.928	529 k	391	8.6
X7R-22	10	166 $\mu$	6.8	13.6	89	0.928	30.9 k	272	8.9
X7R-23	10	166 $\mu$	6.8	13.5	46	0.928	955 k	105	9.1
X7R-24	10	166 $\mu$	6.8	13.4	287	0.928	974 k	263	0.54
X7R-25	10	166 $\mu$	6.8	13.3	1387	0.96	92.9 k	372	0.61
X7R-26	100	166 $\mu$	6.8	18~18.5	618	0.56	47 k	1.3	4.23
X7R-27	100	166 $\mu$	6.8	18.4	81	0.576	2.64 k	1.1	5.45
X7R-28	1	13.4 m	110	22	5104	1.328	1170 k	9.4	_***
X7R-29*	1	13.4 m	110	23	14189	-	-	427 k	0.85
NPO-1**	10	820 $\mu$	6.8	14.8	7	-	-	0.715	10.21
NPO-2	10	820 $\mu$	6.8	14.7	10	0.608	0.822	0.608	10.07
NPO-3*	10	820 $\mu$	6.8	14.5	-	-	-	17.7 M	10.32
NPO-4	10	820 $\mu$	6.8	14.6	1	0.576	0.595	0.561	10.01
NPO-5	10	820 $\mu$	6.8	14.6	49	0.592	0.511	0.511	10.22
NPO-6	10	820 $\mu$	6.8	14.6	42	0.56	0.828	0.753	10.25
NPO-7	10	820 $\mu$	6.8	14.6	36	0.56	0.738	0.631	10.17



NPO-8	10	820 $\mu$	6.8	14.6	225	0.592	0.617	0.513	10.27
NPO-9**	10	330 $\mu$	2.2	10	1	-	-	0.871	10.32
NPO-10	10	330 $\mu$	3	11	15	0.64	0.691	0.658	10.31
NPO-11	10	330 $\mu$	3	10.8	10	0.616	0.897	0.631	10.25
NPO-12	10	330 $\mu$	3	10.8	47	0.608	0.756	0.660	10.17
NPO-13	10	330 $\mu$	3	10.5	24	0.632	0.667	0.574	10.26
NPO-14	10	330 $\mu$	3	10.5	15	0.632	0.659	0.621	10.30
NPO-15	10	330 $\mu$	3	10.2	2	0.616	36.0 M	0.923	9.889
NPO-16	10	330 $\mu$	3	10	1	0.592	0.780	0.739	8.649
NPO-17	10	330 $\mu$	3	9.8	60	0.576	0.698	0.698	10.26
NPO-18	10	2.46 m	20	19.6~19.8	249	0.576	0.548	0.548	10.29
NPO-19	10	2.46 m	20	19.8	2	0.496	0.831	0.831	10.21
NPO-20	10	2.46 m	20	19.7	239	0.568	0.704	0.628	10.17
NPO-21	10	2.46 m	20	19.7	10	0.576	0.782	0.616	10.15
NPO-22	10	2.46 m	20	19.6	4546	0.576	0.545	0.448	10.09
NPO-23	10	15.03 m	39	19	55	0.576	0.691	0.634	10.17
NPO-24	10	15.03 m	39	18.9~19.2	348	0.576	0.591	0.508	10.26
NPO-25	10	15.03 m	39	19	25	0.576	0.758	0.626	10.34

\* Note: No insulation resistance failure is observed for the test sample.

\*\* Note: The test data were not recorded for the failure event.

\*\*\* Note: The measurement of the capacitance is not accurate with a small parallel resistance.

### 3.2 Voltage waveforms

Typical voltage waveforms across a capacitor-under-test prior to failure are shown in Fig. 5. Sinusoidal waveforms are observed for an NPO capacitor, and approximately sinusoidal waveforms are observed for X7R capacitors. The X7R waveforms are not perfectly sinusoidal due to the highly dependent capacitance of X7R capacitors on the applied voltage. For NPO capacitors, the dependence of the capacitance on the voltage prior to breakdown is generally negligible. The circuits with NPO capacitors have higher quality factors than the circuits with X7R capacitors. The quality factors were at least 1000 for the NPO capacitors and at least 40 for the X7R capacitors in this test (both measured at 1  $V_{rms}$  and 1 kHz). Two kinds of waveforms for an X7R capacitor or an NPO capacitor are observed during the test. One is a simple sinusoidal (or approximately sinusoidal) waveform as indicated by pulse #328 of X7R-18 and pulse #40 of NPO-1 in Fig. 5. The other type, as indicated by pulse #323 of X7R-18 and pulse #41 of NPO-1, starts with sharp voltage spikes and has lower oscillating voltage amplitudes. This phenomenon can be explained by the test as described as follows.



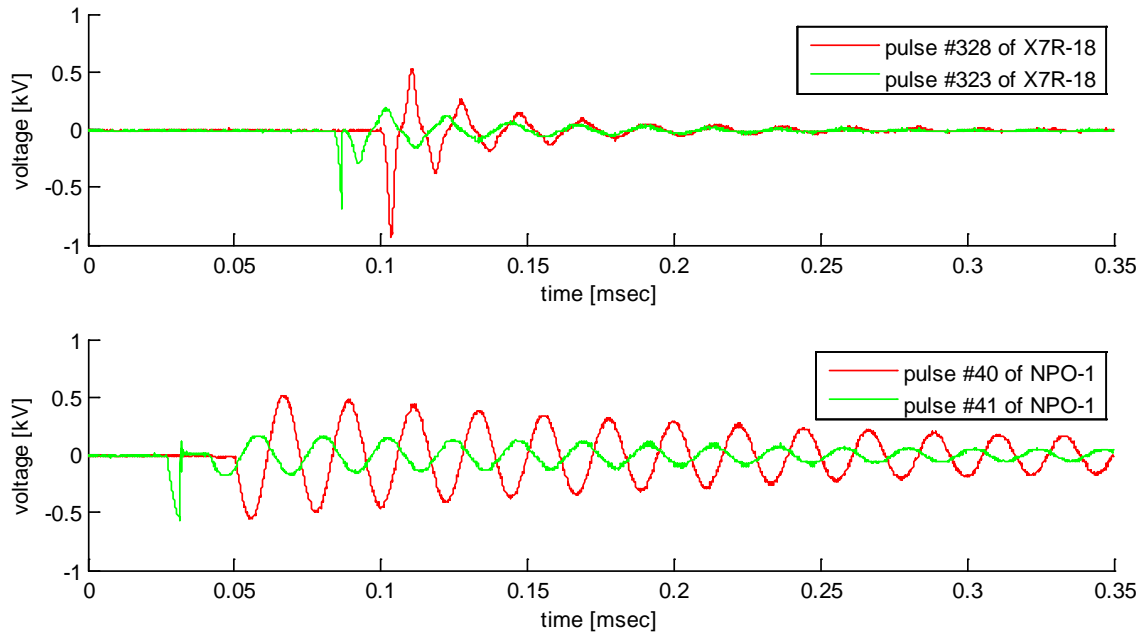


Fig. 5. Typical test voltage waveforms.

Although the high-voltage relay is specifically designed for high-voltage applications, there are still small sparks between the contacts due to the high  $di/dt$  that occurs when the relay opens. A test was performed to identify this phenomenon. Fig. 6 shows 4 locations (spots) where the current was measured and Fig. 7 shows the waveforms of the measured currents. The current spikes observed at Spot 1, Spot 3 and Spot 4 suggest that the corresponding voltage spikes are caused by sparks between the contacts of the high-voltage relay.

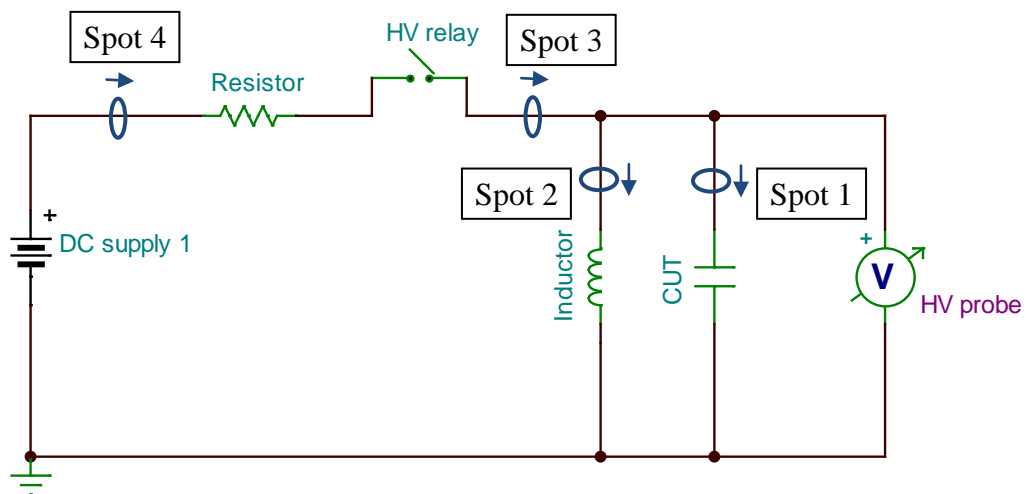


Fig. 6. Current measurement spots.

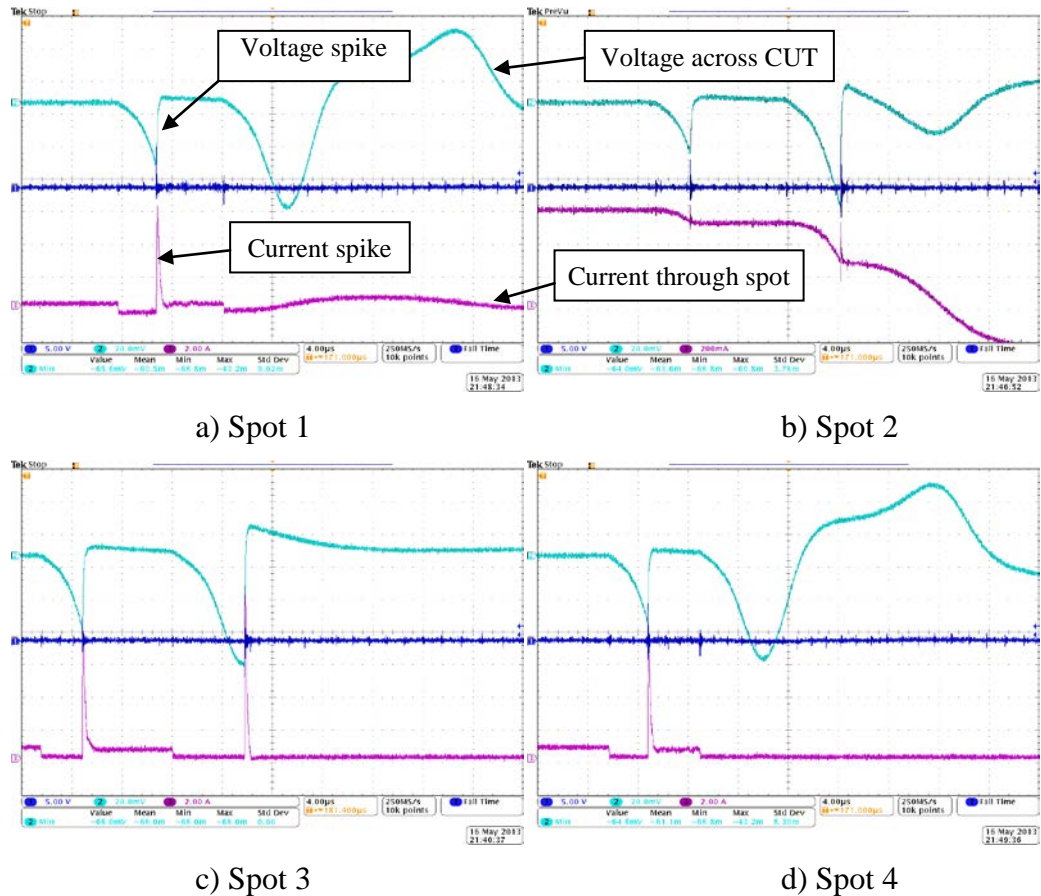


Fig. 7. Voltage and current waveforms.

### 3.3 Failure voltage

Due to the nature of the test, which is repeatedly applying a high AC voltage (10 to 20 times the rated voltage), the exact failure pulse can be difficult to identify. In these tests, capacitor failures were determined by the resistance measurement. If the resistance measured after a pulse was less than 1/10 of the initial value, the capacitor failed. However, this is not always a reliable way to identify a failure. Even if the resistance has not degraded significantly, the capacitor may be defective. In Fig. 8, after pulse #3, the resistance measured does not show any obvious degradation compared with resistances measured after the previous pulses. Starting after pulse #4, the measured resistance decreases to less than 1 k $\Omega$ . Based on the measurements, the conclusion is drawn that the capacitor failed at pulse #4. However, according to the recorded voltage waveforms on the right of the figure, it is clear that the maximum voltage applied to the capacitor during pulse #4 was only 0.24 kV, which is less than a half the peak voltage of earlier pulses. Also, after pulse #3, the spikes were smaller and the ringing was damped. Thus, the capacitor appeared to be defective prior to pulse #4. Therefore pulse #3 in Fig. 8 was determined to be the failure pulse. Similar methods were used to determine the failure pulse for the other capacitors. In other words, the failure event was defined as the pulse after which a low resistance was measured or low-peak pulses without ringing were observed.

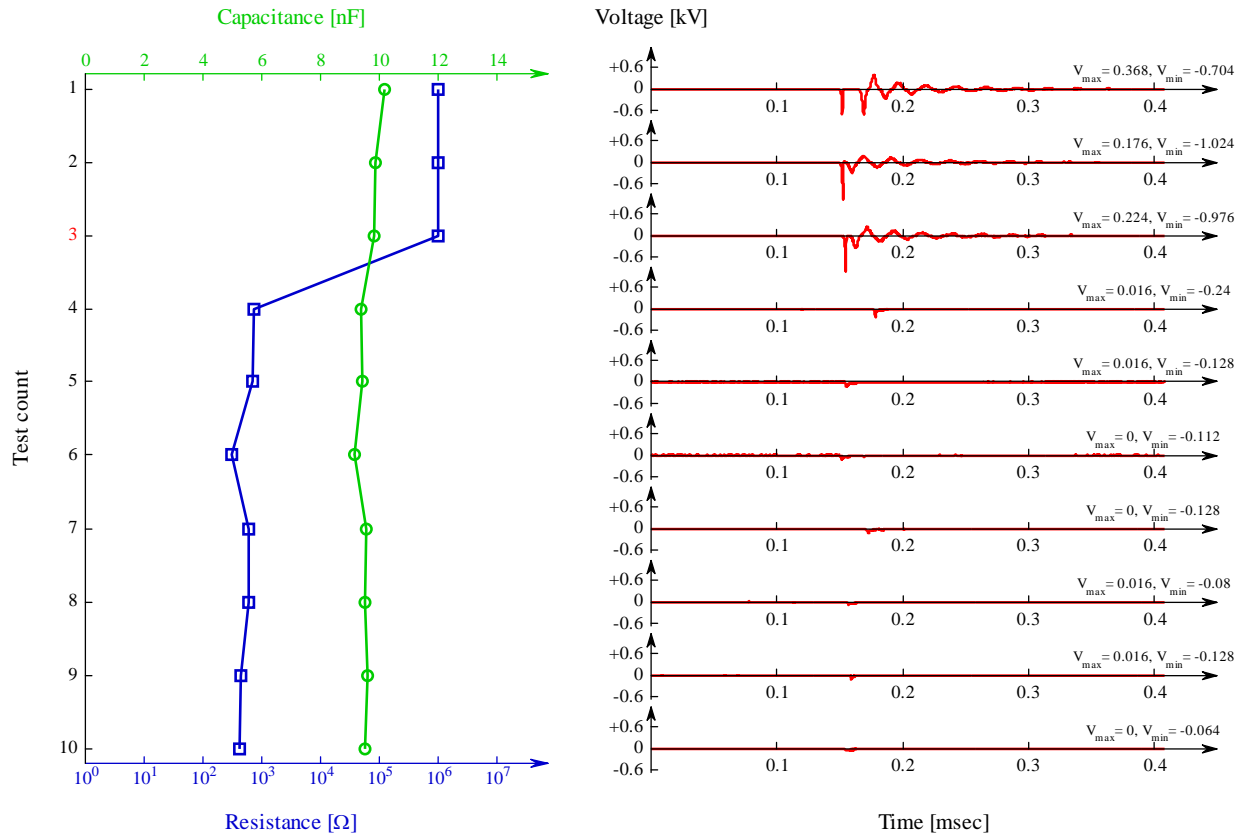


Fig. 8. Voltage waveforms of test counts before and after the failure and corresponding capacitance and resistance measurements of X7R-15.

As shown in Fig. 9, the failure voltage for X7R capacitors decreases with the nominal value of the capacitor, varying from about 0.6 kV for 100-nF capacitors to more than 1.3 kV for the 1-nF capacitor. 10-nF X7R capacitors feature a higher failure voltage than NPO capacitors with the same nominal capacitance. However, this does not imply that a 10-nF X7R capacitor is more capable of handling electric overloads than a 10-nF NPO capacitor. The X7R capacitance decreases with voltage reducing the ability to store electric charge. In Table 1, the minimum initial current in an 820- $\mu$ H inductor that causes a failure is about 1.2 A for a 10-nF X7R capacitor and 2.1 A for a 10-nF NPO capacitor. Thus, in this case, more energy is needed to damage the NPO capacitor than the X7R capacitor with the same nominal capacitance.

Fig. 10 shows the failure voltage of the 10-nF capacitors grouped by the inductance of the inductor in the LC circuit. Different inductances result in different resonant frequencies. The value of the inductance did not significantly affect the failure voltage for the various 10-nF capacitors in these tests.

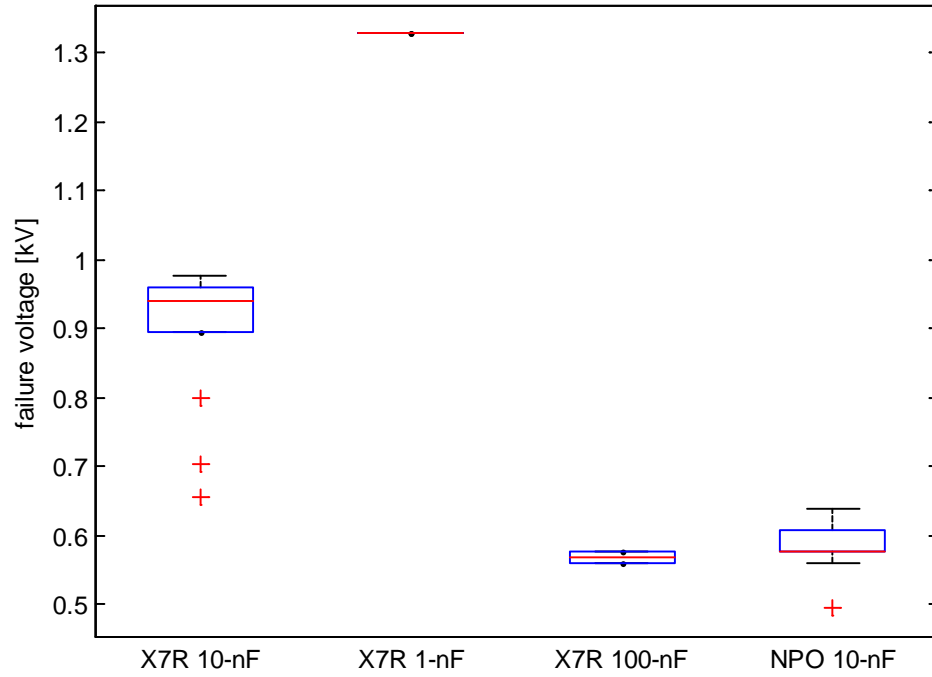


Fig. 9. Failure voltage of capacitors with different nominal values.

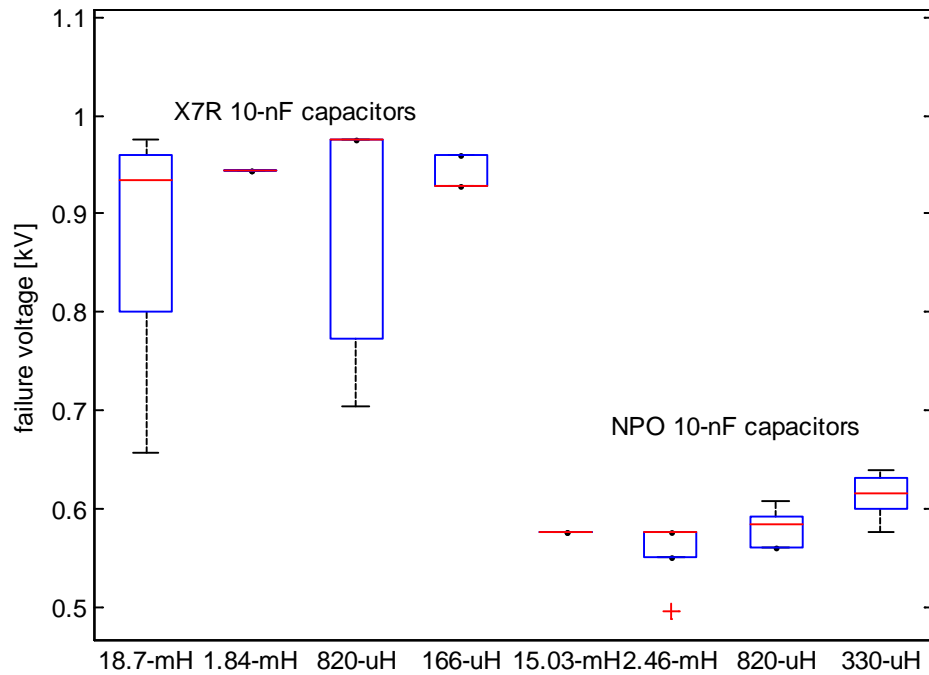


Fig. 10. Failure voltage of 10-nF capacitors grouped by inductance.

The waveform of the failure pulse varied depending on the type of capacitor. As shown in Fig. 11, most of the failures appear to occur on the first voltage peak.

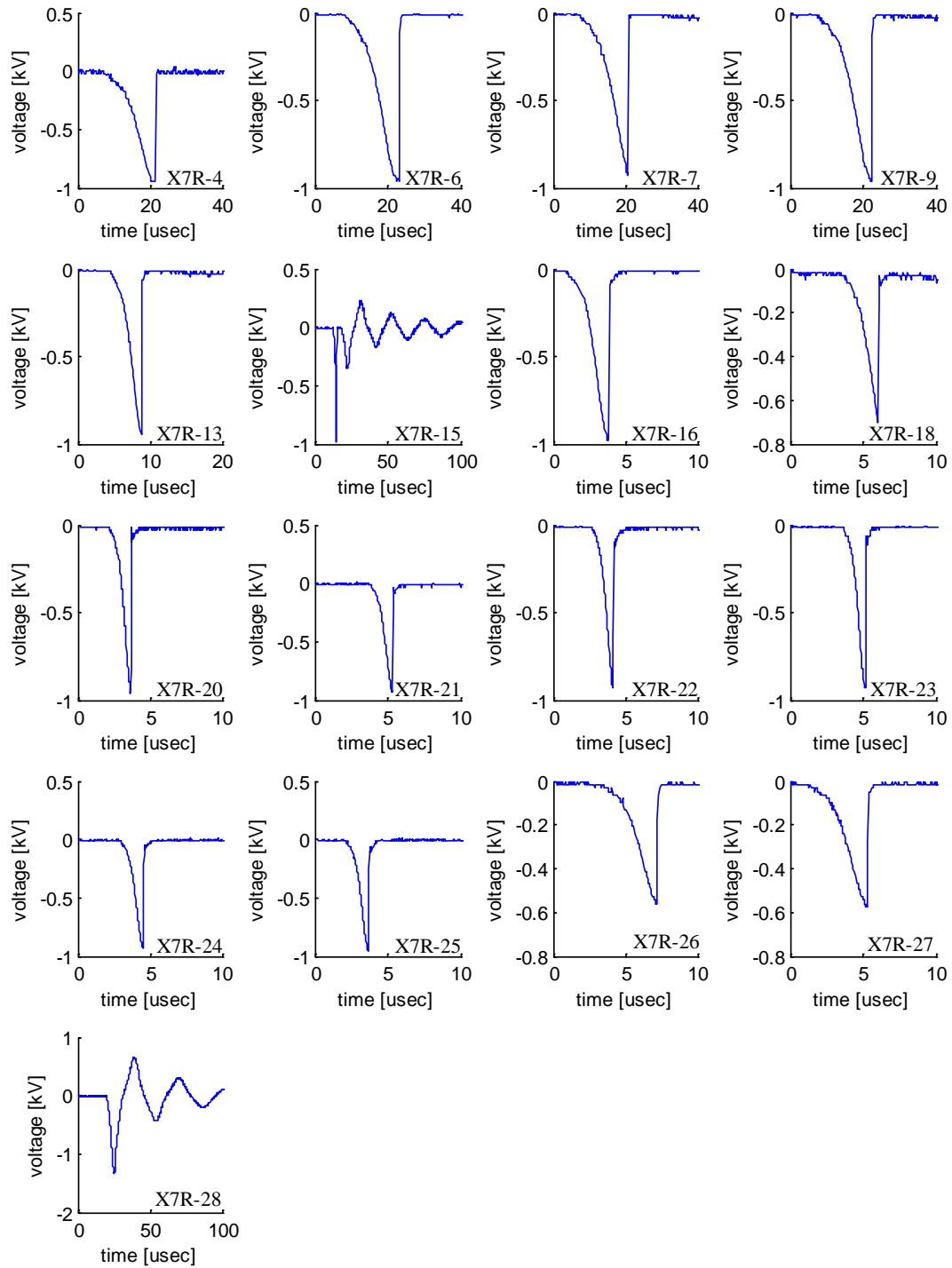


Fig. 11. Failure voltage waveforms for X7R capacitors.

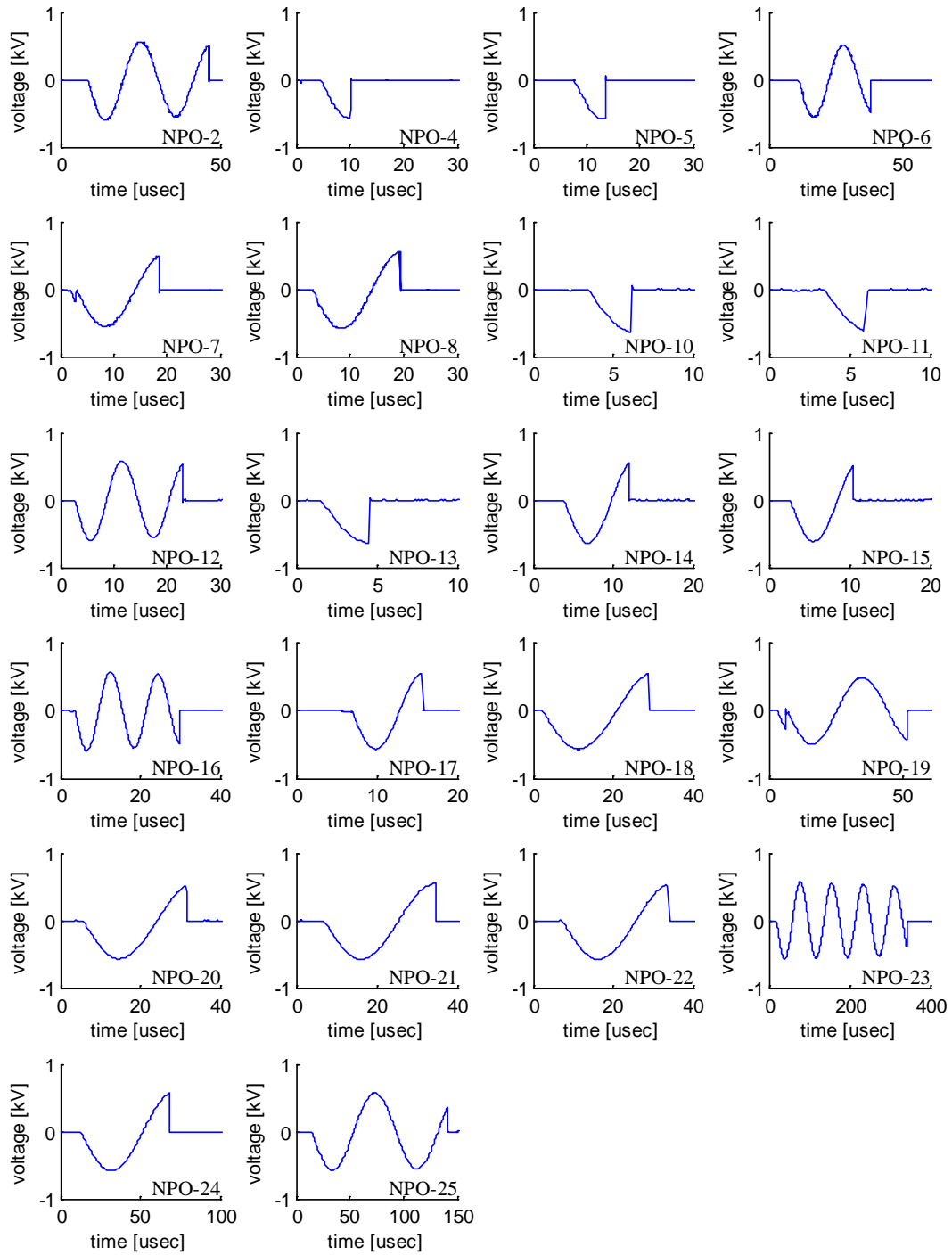


Fig. 12. Failure voltage waveforms for NPO capacitors.

The NPO capacitors present a different scenario regarding the failure waveform. In Fig. 12, of 22 failure waveforms recorded, only 5 of them fail at the first voltage peak. The other capacitors survive the first voltage peak, which has the highest amplitude. An extreme case is observed on the sample NPO-23, which survives the first 4 cycles before the sudden change in voltage at a relatively low level. All of the NPO capacitors tested failed short (with relatively low resistances).

### 3.4 Degradation and recovery of post-failure resistance

One of the objectives of this study was to evaluate the degradation of insulation resistance that can occur when capacitors are subjected to high-voltage pulses. Fig. 13 shows the range of AC resistances measured at 1 kHz with the LCR meter after the failure pulse. It indicates that X7R capacitors generally fail with a resistance higher than 2 k $\Omega$ , and NPO capacitors fail with much lower resistance values. Only 1 of the 25 NPO capacitors tested failed with a high resistance (Fig. 14). The sample NPO-15 failed with an insulation resistance of about 30 M $\Omega$  measured right after the failure pulse (#2). The measured resistance of X7R capacitors immediately after a failure was comparable to the measured value before the failure. X7R capacitors tended to behave like varistors or diodes after a failure, exhibiting a low resistance only when exposed to high voltages.

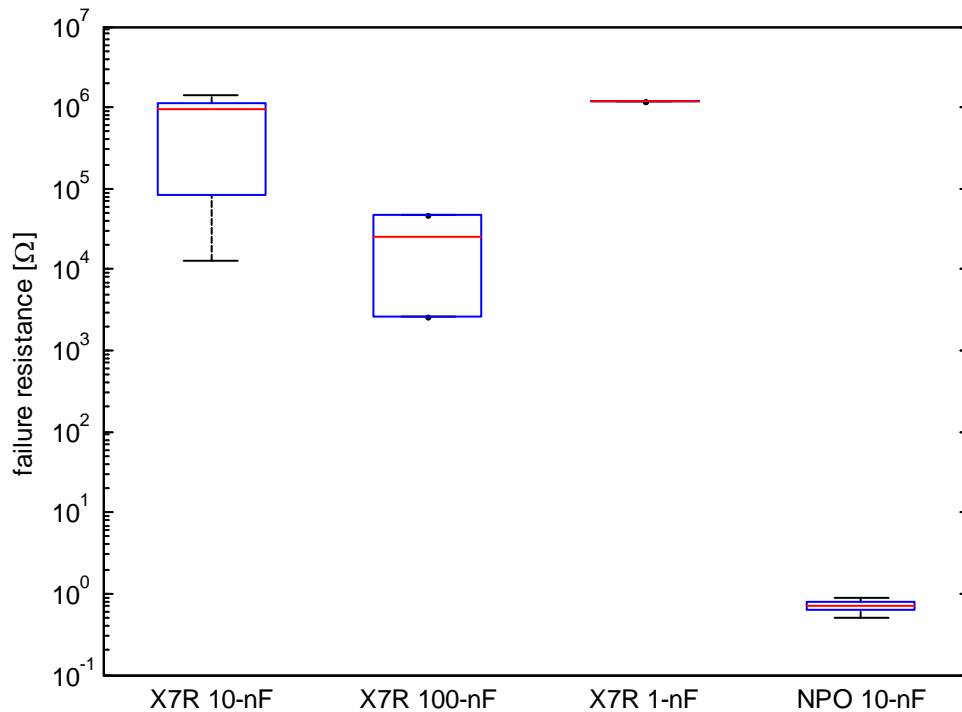


Fig. 13. Parallel resistance measured after the failure pulse.



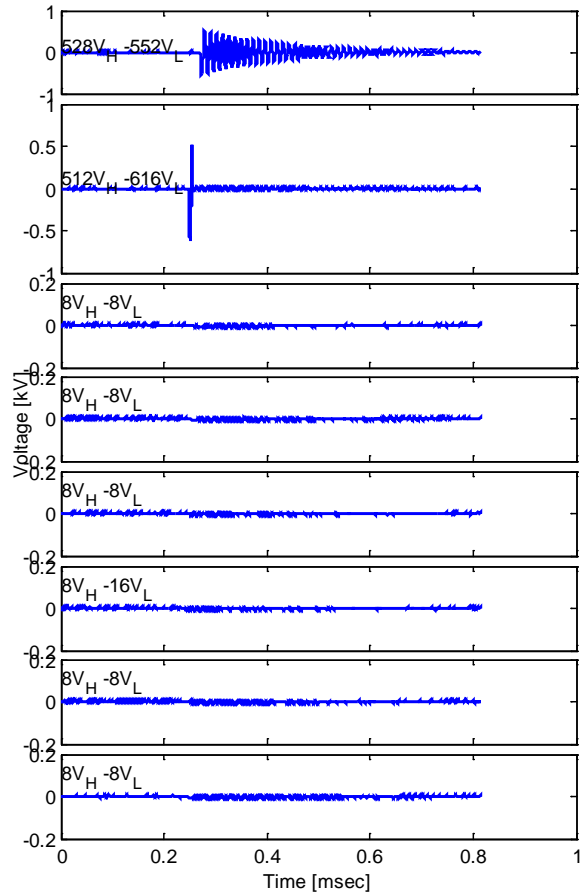
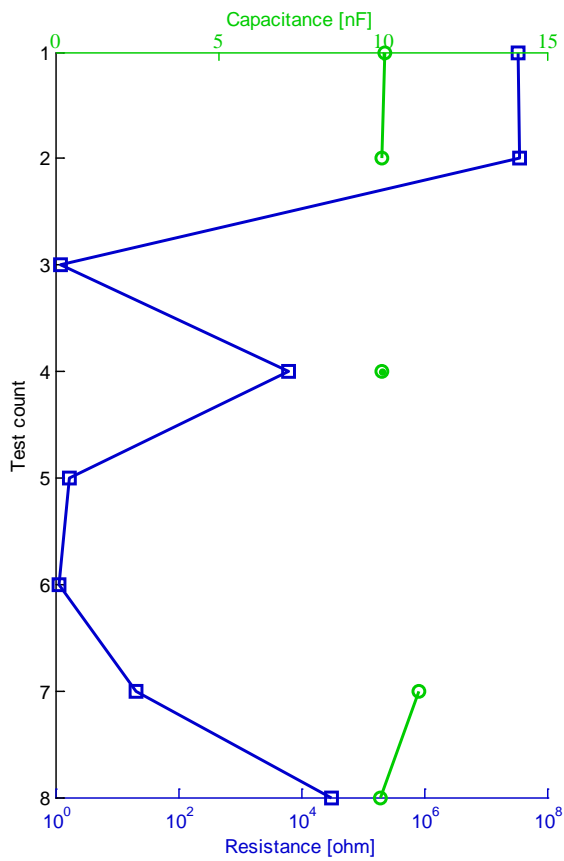


Fig. 14. An outlier of NPO capacitors in the failure resistance.

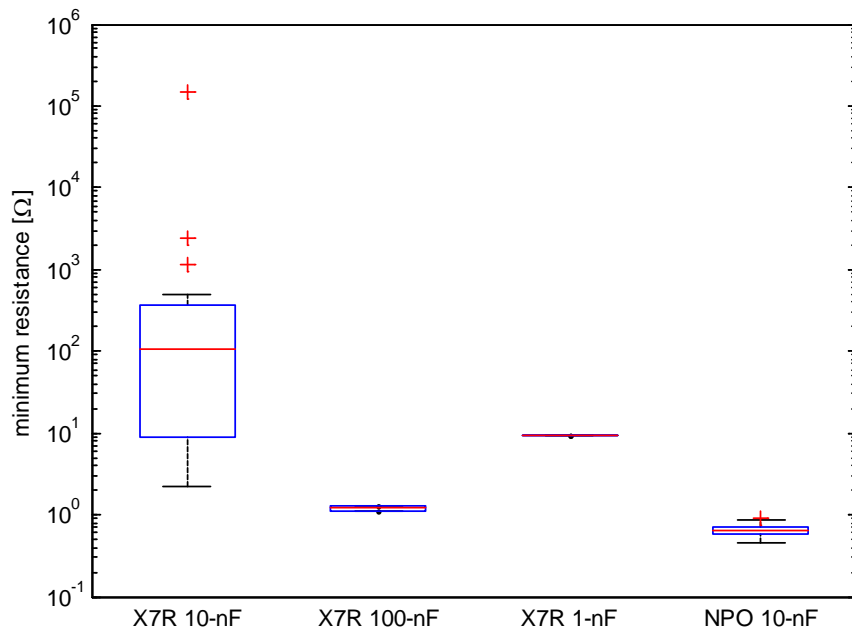


Fig. 15. Lowest resistance measured during the pulse test.

The failure resistance recovers fully or partially in some of the X7R capacitors during the pulse test. In Fig. 16, the insulation resistance of an X7R capacitor fully recovered from pulses #2200 to #2500 and from pulses #3000 to #3800. The capacitor failed at a pulse number of about #1500. A full recovery means that the measured resistance is at least as high as it was in the measurements before the failure. For NPO capacitors, a full recovery was never observed. The AC resistance could only be recovered partially and briefly as seen in Fig. 17.

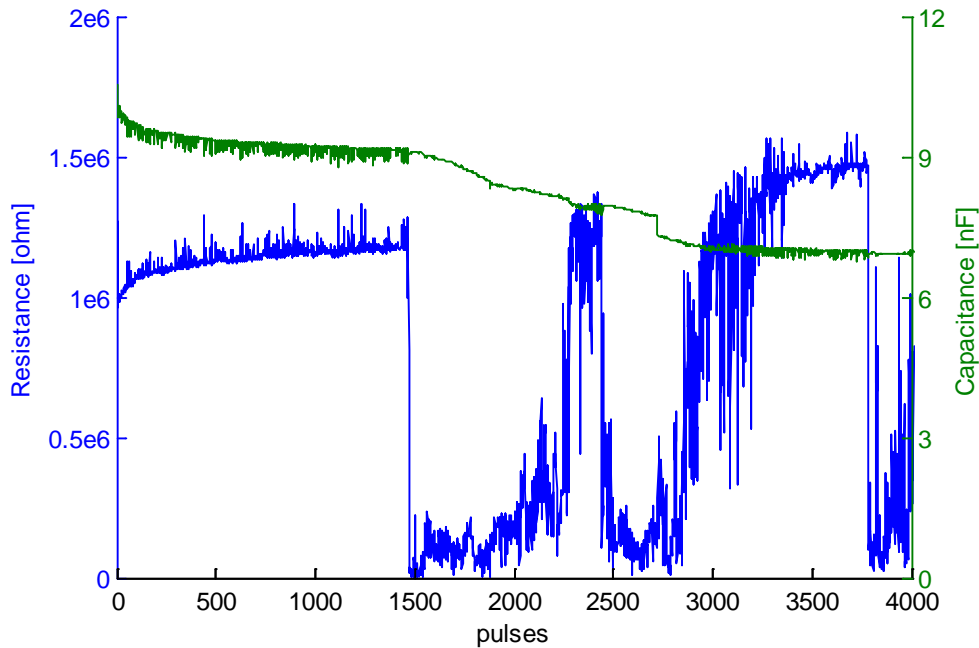


Fig. 16. Recovery of parallel resistance during the pulse test of the sample X7R-12.

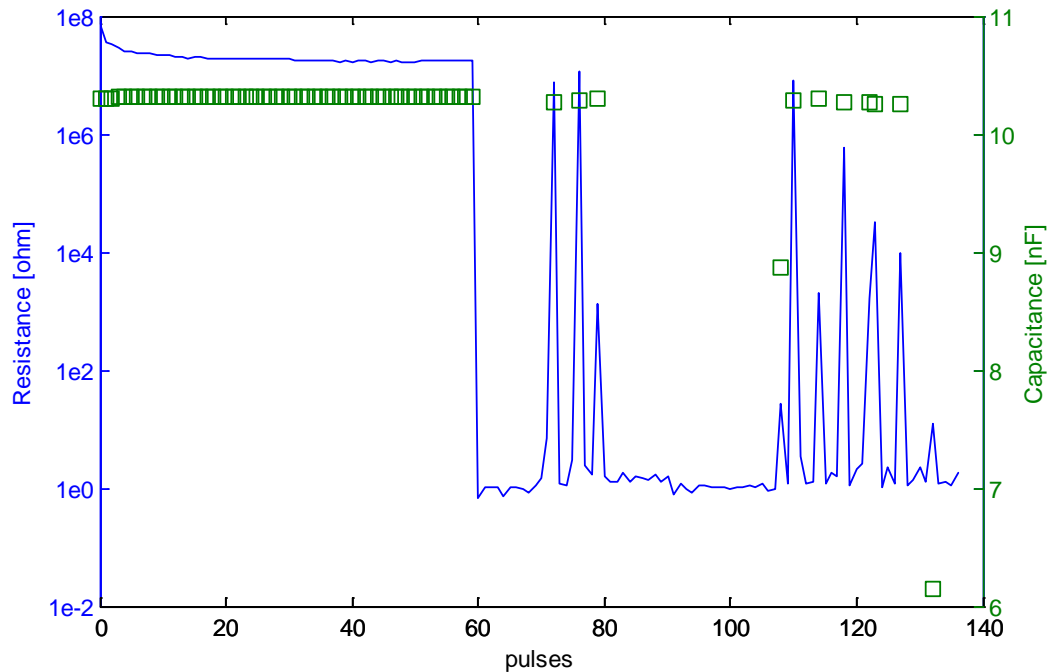


Fig. 17. Recovery of parallel resistance during the pulse test of the sample NPO-17.

### 3.5 Degradation of capacitance

The capacitance of X7R capacitors was degraded during the course of the testing. All X7R capacitors lost more than 10% of their initial capacitance after about 300 pulses. Some capacitors lost more than 20% of their initial value (e.g. Fig. 18). For NPO capacitors, the capacitance increased slightly during the course of the testing up to the point where a failure was observed.

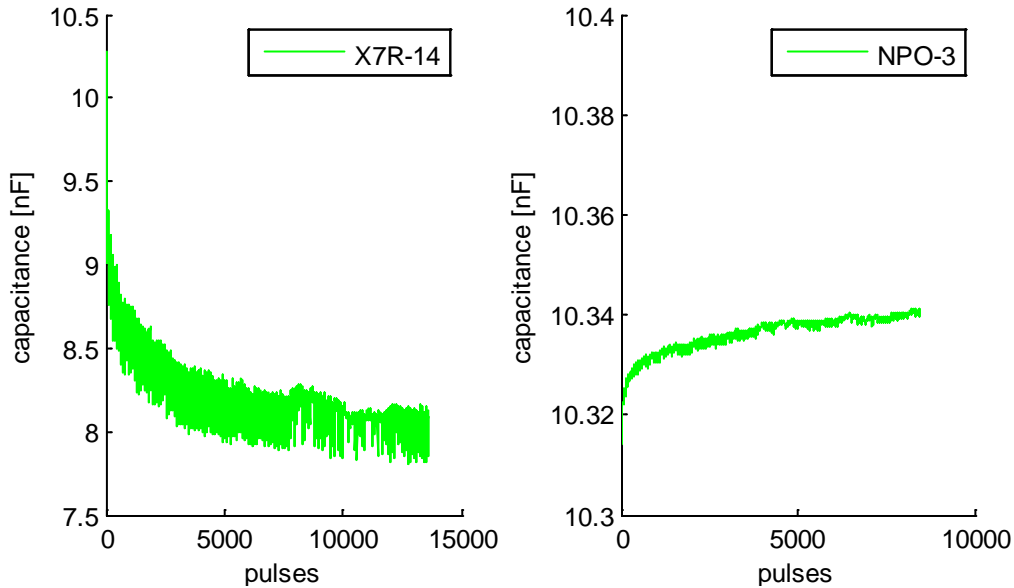


Fig. 18. Examples demonstrating how the capacitance typically changed during the course of the testing.

Some of the X7R capacitors decreased in capacitance in a step manner as seen in Fig. 19. In some of these tests, 90% of the capacitance was lost. The degradation of capacitance could not be confirmed for the NPO capacitors because the NPO capacitors fail with a much lower parallel resistance, which makes the measurement of the capacitance inaccurate. The continuously stepping-down capacitance might be due to the loss of individual electrode plates caused by the high-voltage overstresses.

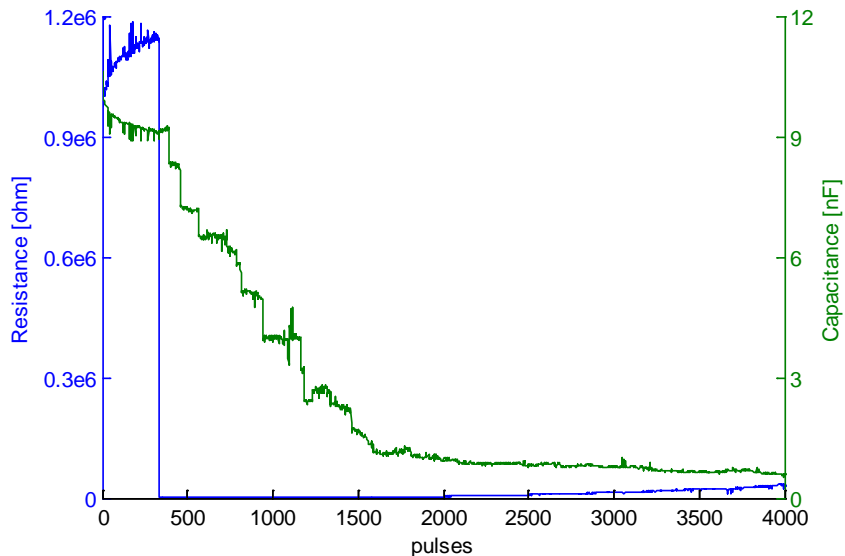


Fig. 19. Severe degradation of capacitance during the pulse test of the sample X7R-18.

---

## 4. Conclusion

The failure voltages and failure modes of X7R and NPO capacitors exposed to a series of electrical fast transients were analyzed in this paper. Most of the failures for X7R capacitors occurred at the peak of the applied voltage waveform. X7R capacitors with lower capacitances failed at higher voltages. The value of the inductor used to create the transient did not significantly affect the failure voltage. Most of the X7R capacitors tested did not exhibit an obvious decrease in insulation resistance immediately following the failure pulse, though their resistance tended to drop significantly with the repeated application of pulses after the failure. X7R capacitors sometimes recovered their insulation resistance fully or partially during post-failure pulses. More than a 10% degradation in capacitance was commonly observed for X7R capacitors subjected to repeated EFTs. Some X7R capacitors lost about 90% of their initial capacitance during the course of the testing.

For a given capacitance (10-nF), NPO capacitors failed at lower voltages than X7R capacitors. However, because the capacitances of X7R capacitors decreased with increasing applied voltages, the energies stored in the NPO capacitors during a failure were actually higher than those stored in the X7R capacitors. NPO capacitors often failed as short circuits. NPO capacitors were less likely to recover with the repeated application of pulses, and recovered only partially and briefly. Capacitance degradation was not observed in NPO capacitors.

## References

- [1] R. Munikoti and P. Dhar, "Highly Accelerated Life Testing (HALT) for Multilayer Ceramic Capacitor Qualification," *IEEE Trans. Compon., Hybrids, Manuf. Technol.*, vol. 11, no. 4, Dec. 1988.
- [2] D. Zhang, K. Patil and T. Hubing, "Non-Linear Resistance of Multi-layer Ceramic Capacitors Caused by Electrostatic Discharge," *Clemson Vehicular Electronics Laboratory Technical Report, CVEL-13-042*, Apr. 29, 2013.
- [3] S. Tenbohlen, F. Streibl, J. Hartmann, and M. Zerrer, "Derating of Ceramic Capacitors under ESD Stress," *Proc. of IEEE Int. Symp. Electromagn. Compat.*, pp. 1-4, Sept. 2008.
- [4] H. C. Ling and D. D. Chang, "Surge Test Characteristics of High K Multilayer Ceramic Capacitors," *IEEE Trans. Compon., Hybrids, Manuf. Technol.*, vol. 14, no. 3, Sept. 1991.
- [5] N. H. Chan and B. S. Rawal, "Low-Voltage Performance of Multilayer Ceramic Capacitors," *AVX Technical Information*, Jul. 19, 2004.
- [6] D. Liu, "Failure Modes in Capacitors When Tested Under a Time-Varying Stress," Capacitor and Resistor Technology Symposium, CARTS USA 2011, Jacksonville, FL, Mar. 2011.
- [7] H. Domingos, D. P. Quattro and J. Scaturro, "Breakdown in Ceramic Capacitors under Pulsed High-Voltage Stress," *IEEE Trans. Compon., Hybrids, Manuf. Technol.*, vol. CHMT-1, no. 4, Dec. 1978.
- [8] H. C. Ling and D. D. Chang, "In-Situ Observation of Electrode Melting in Multilayer-Ceramic Capacitors," *Proc. of 38th Electronic Components Conf.*, pp. 87-94, May 1988.