CVEL

THE CLEMSON UNIVERSITY VEHICULAR ELECTRONICS LABORATORY

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Parasitic Inductance Cancellation for Filtering to Chassis Ground Using Surface Mount Capacitors

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Abstract

Parasitic inductance cancellation is applied to a surface mount shunt capacitor that is connected through a screw to a chassis ground plate separate from the reference planes of the PCB. This filter is demonstrated to have considerably better filtering performance than a comparable conventional shunt capacitor arrangement from 60 MHz to 800 MHz in a 50-Ω system.

1. Introduction

A recent publication by the authors, [1], and a paper in preparation, "A Compact Implementation of Parasitic Inductance Cancellation for Shunt Capacitor Filters on Multilayer PCBs," [2], have both demonstrated designs for using inductance cancellation to improve the high-frequency performance of low-pass filters using surface mount shunt capacitors. In these filter configurations, the capacitor connects a signal trace to a ground plane on the same printed circuit board (PCB). Another common configuration in practical EMI filters is filtering to a chassis ground electrically and/or physically isolated from the PCB ground. In this configuration, inductance cancellation filters have the potential to be especially effective and compact relative to alternative methods for improving the high-frequency filtering performance of surface mount capacitors. This report presents experimental results from the application of the coupled via inductance cancellation design presented in [2] to the practical situation of filtering to a metal plate mounted below a four-layer board.

2. Design and Construction of Filters

The design presented here was modeled in FASTHENRY, as in [1], [2]. Once desirable parameter values were determined, a four-layer printed circuit board (PCB) was fabricated. The PCB consists of the following copper layers and dielectric substrates: top layer copper, 0.31 mm FR4, ground plane copper, 0.711 mm FR4, power plane copper, 0.31 mm FR4, and bottom layer copper. All copper layers were 35 μm thick. The PCB layout is shown in Fig. 1 for the top copper layer and in Fig. 2 for the bottom copper layer. In order to provide a chassis ground conductor in the setup, a 0.70 mm thick thermally conductive electrical insulator and a 0.81 mm thick aluminum plate were placed below the bottom layer of the PCB. Screws with an outer thread diameter of 1.44 mm connected the aluminum plate to the solder pads of the capacitors. SMA connectors penetrated the PCB-insulator-aluminum stack at both ends of the board. The end result was that the currents from the network analyzer primarily traveled in a loop along the top layer of the board, through the capacitor body, through a screw, and then returned along the aluminum plate.

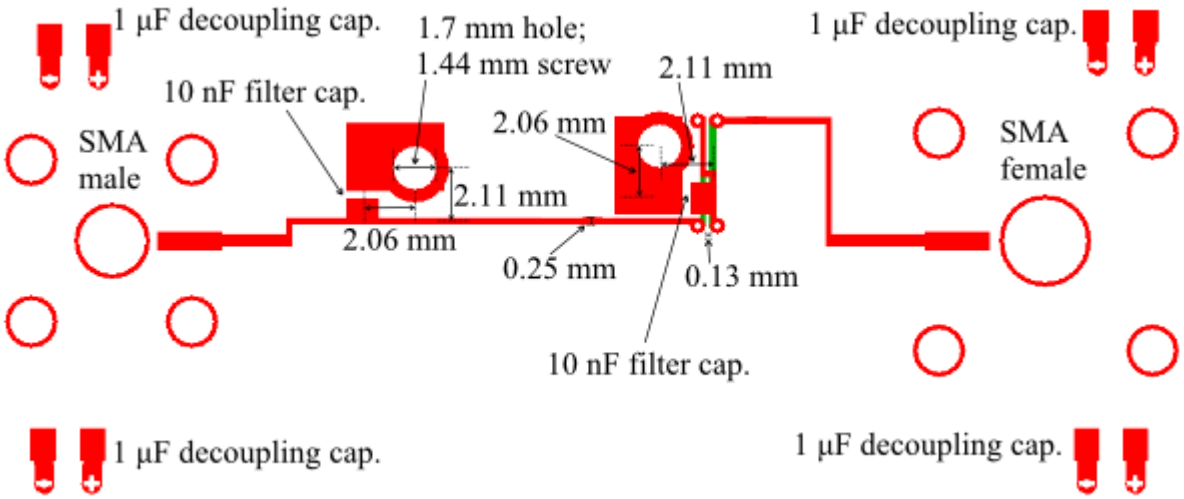

Fig. 1. Top-layer board layout.

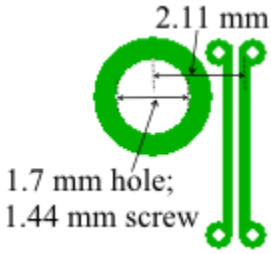

Fig. 2. Bottom layer copper that forms coupled via inductance cancellation design.

Fig. 3 shows a photograph of the top of the constructed board. This photograph shows a removed PCB trace branch bypassing the filter using inductance cancellation on the top and another PCB trace branch on the bottom with another inductance cancellation design implementation. For the results presented in this report, the bottom branch and the bypass branch on the top were not used, and the traces were cut as shown in Fig. 3. For comparing the performance of the inductance cancellation filter to that of a conventional single capacitor filter, the insertion gains were measured when only one of the two 10-nF filter capacitors with 0603 packages shown in Fig. 3 was present. The boards additionally had four 1-µF decoupling capacitors placed at the corners of the board that connected the power and ground planes of the PCB. Fig. 4 shows a cross-sectional view of the layer stack with the aluminum plate on the top, the insulator in the middle and the PCB on the bottom.

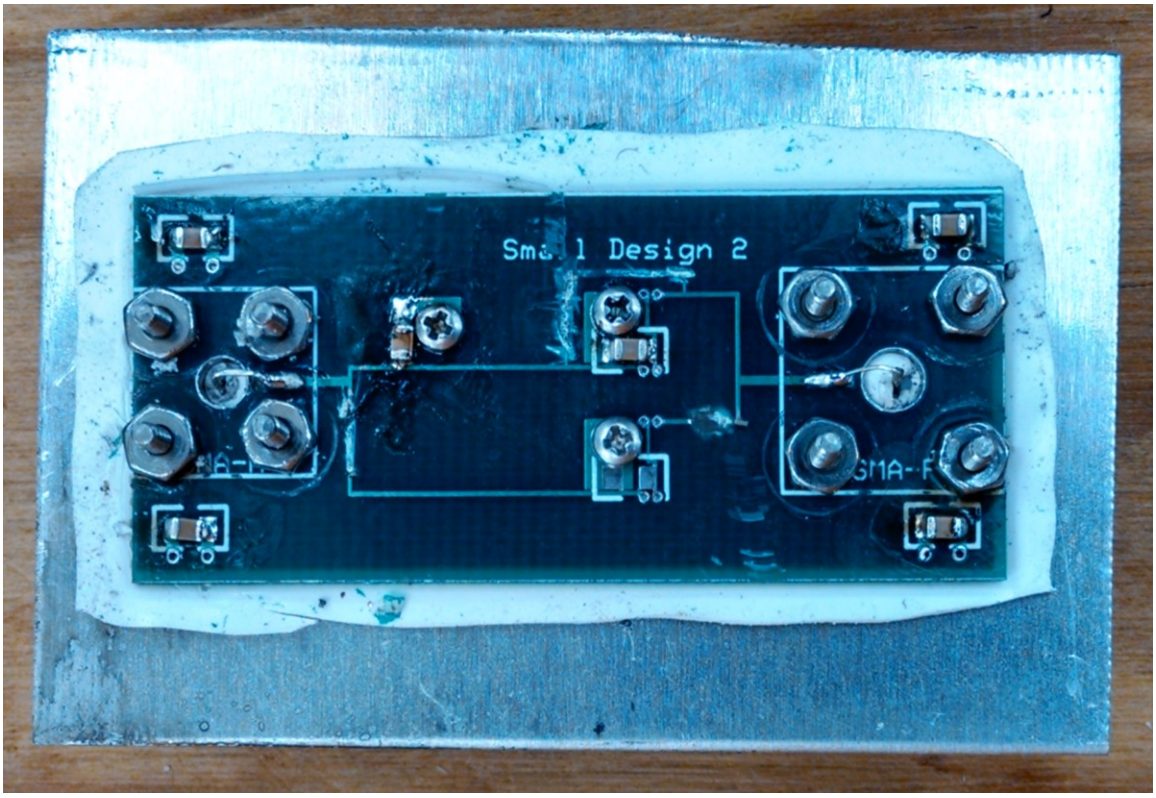

Fig. 3. Top view of constructed board with both filter capacitors soldered on.

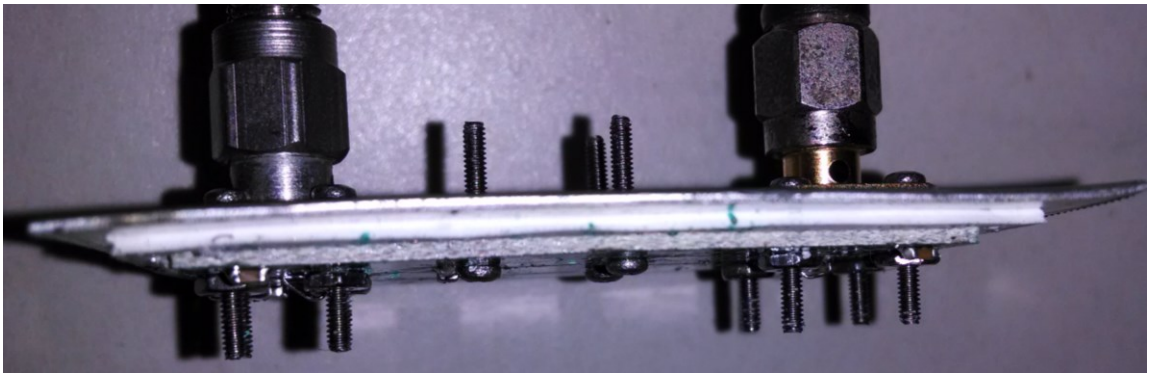

Fig. 4. Cross section of constructed board.

3. Experimental Results

For comparison, the insertion gain of the constructed board was measured when a 10-nF capacitor was soldered onto the pads for the conventional shunt capacitor and no capacitor was soldered onto the pads for the inductance cancellation filter. These results are plotted as the dashed red curve in Fig. 5. Likewise measured results for the board with a 10-nF capacitor soldered onto the pads of the inductance cancellation filter only are shown in the solid blue curve in Fig. 5. The inductance cancellation filter exhibits approximately 15 dB improved performance from 100 MHz to 500 MHz relative to the conventional shunt capacitor.

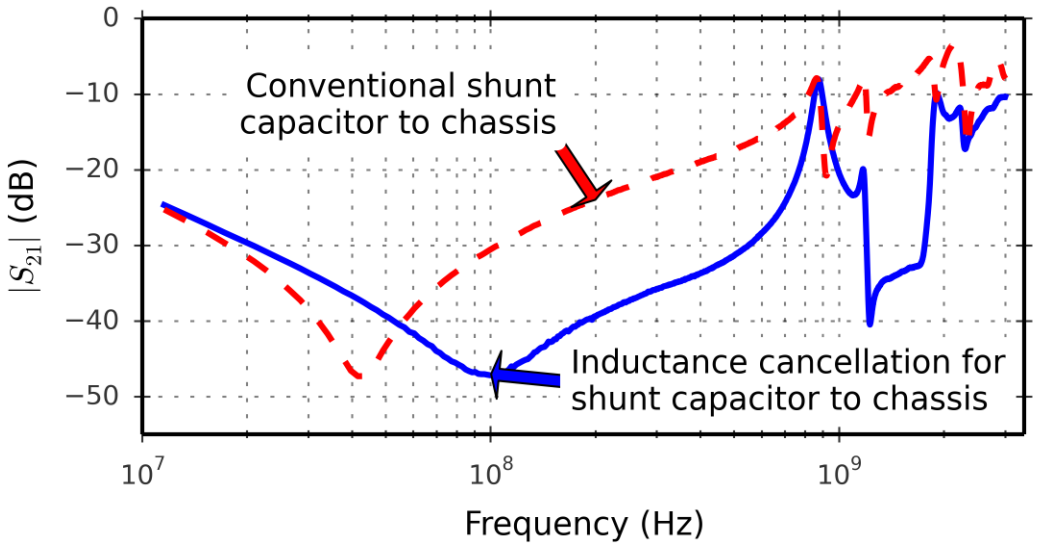

Fig. 5. Measured insertion gains of conventional shunt capacitor filter and inductance cancellation design.

4. Conclusion

This usage of the coupled via inductance cancellation filter from [2] for improving the performance of surface mount capacitors used to filter signals to a chassis ground represents a practical application of inductance cancellation designs for surface mount capacitors. The design was compactly implemented on a four layer PCB. The design presented here uses narrower traces than the coupled via designs presented in [2], so the coplanar traces in this work contribute to a greater proportion of the overall cancellation inductance than do the coplanar traces in [2].

References

[1] A. J. Mcdowell and T. H. Hubing, "Parasitic Inductance Cancellation for Surface Mount Shunt Capacitor Filters," *IEEE Trans. Electromag. Compat.*, vol. 56, no. 1, pp. 74–82, Feb. 2014.

[2] A. J. Mcdowell and T. H. Hubing, "A Compact Implementation of Parasitic Inductance Cancellation for Shunt Capacitor Filters on Multilayer PCBs," 2014. In preparation.