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The Effect of Electrical Fast Transients on Multi-Layer Ceramic Capacitors

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Abstract

This paper investigates the susceptibility of multi-layer ceramic (MLC) capacitors to high-voltage electrical fast transients (EFTs). X7R and NP0 MLC capacitors with a 50-V voltage rating and 0603 package size were tested. X7R capacitors often failed during a spike in the voltage, but exhibited no obvious degradation in the measured insulation resistance at low voltages immediately after the failure. NP0 capacitors usually failed by suddenly shorting and maintaining the short after the failure. With the application of additional voltage spikes, some X7R capacitors exhibited a full recovery in terms of the measured resistance, returning to their initial state. The resistance of an X7R capacitor damaged by an EFT event is a function of the applied voltage. The terminal impedance can be modeled as two diodes in parallel.

1. Introduction

Multi-layer ceramic (MLC) capacitors are widely used due to their low cost and small size. These capacitors are often used to filter inputs and outputs thus exposing them to electrical overstress. Traditional failure analysis of MLC capacitors has focused on post-system-failure analysis. These studies have helped people to better understand the characteristics of MLC capacitors and have helped to guide the manufacturing process. However, very few studies have focused on the analysis of capacitor failures that may go unnoticed during the normal operation of a system. Undetected capacitor failures in safety-critical or mission-critical systems can have serious consequences. Therefore, it is important to understand how different types of capacitors are likely to fail, and the electrical behavior that these capacitors are likely to exhibit prior to a full system failure.

Two failure modes of an MLC capacitor are low insulation resistance and degraded capacitance. Low insulation resistance, typically due to shorting between the capacitor plates, is the most common failure mode. When a failed capacitor's impedance is essentially a short at the system operating voltage, the failure is generally detected by the system. A drop in the insulation resistance from megohms to hundreds of ohms however, might adversely affect the performance of the system without creating a detectable system failure.

Traditionally, the long-term reliability and failure analysis of ceramic capacitors has been based on highly accelerated life testing (HALT). Capacitors are tested in a high-temperature environment with an applied DC voltage. These tests have been used to predict the usable life of capacitors and to establish de-rating rules. In [1], DC voltages as high as 400 V were applied to 50-V capacitors during HALT testing to reduce the qualification time. In these tests, a capacitor was considered to have failed if its leakage current exceeded 100 µA at the rated voltage. Although HALT testing has proven to be an efficient and useful method for evaluating MLC capacitors exposed to high DC voltages and high temperatures, HALT test results have not been correlated to the reliability of MLC capacitors exposed to electrical fast transients (EFTs).

Studies investigating capacitor failures due to EFTs can be classified into two groups based on the type of circuit used to generate the EFT. In [2], [3] and [4], under-damped series RLC circuits were used to study capacitor failures due to transients caused by voltage steps. In [2], 50-V Z5U barium titanate capacitors were found to fail with step voltages of 250-275 V. The peak failure voltage caused by the ringing of the circuit was 900-950 V. According to the study, these capacitors had a static breakdown voltage between 1030 and 1100 V. The peak current observed during a failure was 26 A. In this study, the failed capacitors behaved like a short circuit, which led to a catastrophic failure in the presence of the DC voltage. In [3], low-voltage pulse steps were applied to NP0, X7R and Z5U capacitors. The step voltage across a 0.1-µF capacitor was 4 V and the current was about 0.75 A. Each capacitor was subjected to approximately 3.6 billion pulses during a 1-hour test and no insulation

resistance failure was observed. In [4], a surge step stress test (SSST) was used to investigate failure modes in capacitors of different types including 6.3-V MLC capacitors. The 100-ppm failure step voltages derived from a 2-parameter Weibull fitting method for these capacitors were 10 to 19 times the capacitors' rated voltages.

Another group of tests employed RC circuits to study the failure of capacitors exposed to voltage surges. In [5], a 100-µsec high-voltage single pulse was applied to capacitors through a resistor that limited the current. The voltage across the capacitor increased linearly until breakdown was achieved. The voltage then dropped to a low sustained value, which implied that the capacitor had not failed as a short circuit. It was found that there was little correlation between the rated voltage and the breakdown voltage. In [6], a similar RC circuit was used to test the current surge susceptibility of MLC capacitors. Sectioned and polished capacitors with exposed internal structures were tested. The capacitors had a rated voltage of 50 V and capacitances of 0.1 µF or 0.33 µF. A series of 125-V pulses was applied with a maximum peak current of 1 A. A degradation of insulation resistance (by approximately a factor of 10) was observed during the test. This paper described the failure mechanism as the heat-induced local melting of internal electrodes.

The study described in this paper was focused on characterizing MLC capacitors exposed to electrical overstress (EOS) induced by an LC oscillating circuit. This form of EFT is common in automotive and industrial systems and is typically caused by the interruption of current flowing in an inductance due to the opening of a switch or relay, or a physical break in a current-carrying connection.

2. Test Setup and Test Procedures

The test setup in Fig. 1 was used to apply high-voltage pulses across MLC capacitors while monitoring the applied voltage waveform, and then measuring the parameters of the test capacitor. An LCR meter (B&K Precision 879B) was used to measure the capacitance and the equivalent parallel resistance at 1 kHz of the capacitor under test (CUT) between pulses. An oscilloscope and a high-voltage differential probe recorded the voltage across the capacitor during each applied pulse.

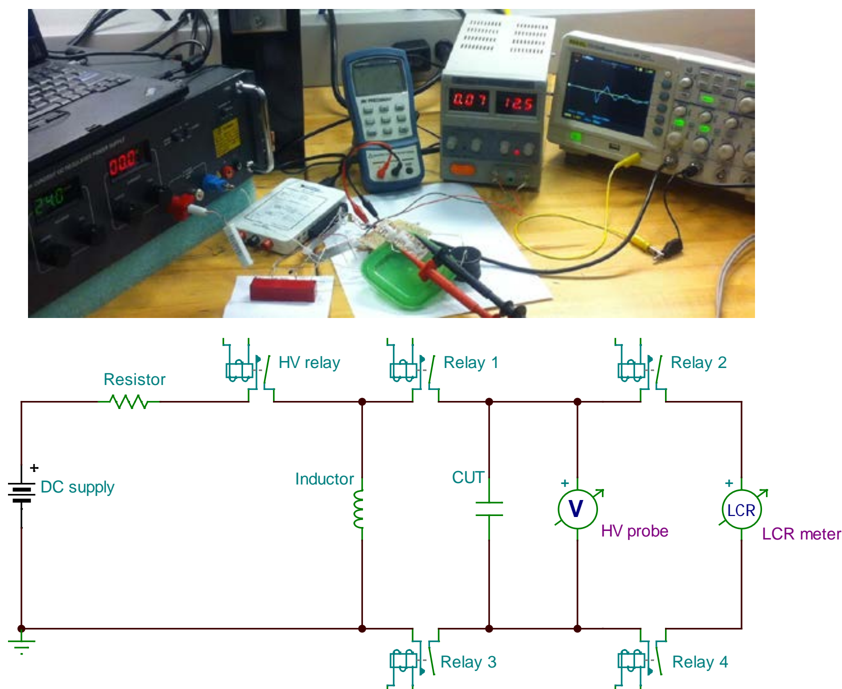


Fig. 1. EFT test configuration for MLC capacitors.

During the test, the high-voltage (HV) relay was turned on to establish a steady-state current in the inductor; then the relay was switched off. The collapsing magnetic field in the inductor induced a transient voltage across the capacitor and caused an oscillation in the LC circuit. The amplitude of the transient voltage applied to the capacitor could be controlled by adjusting the initial current through the inductor. During the course of the testing, the initial current was adjusted to provide just enough energy to cause the capacitor to fail. To determine this initial current value, a trial test was performed for each capacitor of a given type. The frequency of the voltage oscillation was determined by the inductance of the inductor and the value of the capacitor under test.

During the course of a test cycle, Relay 1 and Relay 3 were turned on, and Relay 2 and Relay 4 were turned off. After the voltage across the capacitor died down to an insignificant level, Relay 1 and Relay 3 were turned off, and Relay 2 and Relay 4 were turned on. This allowed the parameters of the capacitor to be measured by the LCR meter.

Both X7R and NP0 capacitors with a voltage rating of 50 V and a 0603 package size were evaluated. The test samples included 25 10-nF X7R capacitors, 2 100-nF X7R capacitors, 2 1-nF X7R capacitors, and 25 10-nF NP0 capacitors.

Typical test voltage waveforms for X7R and NP0 capacitors are shown in Fig. 2. The X7R waveforms are not perfectly sinusoidal because the capacitance of X7R capacitors changes depending on the applied voltage.

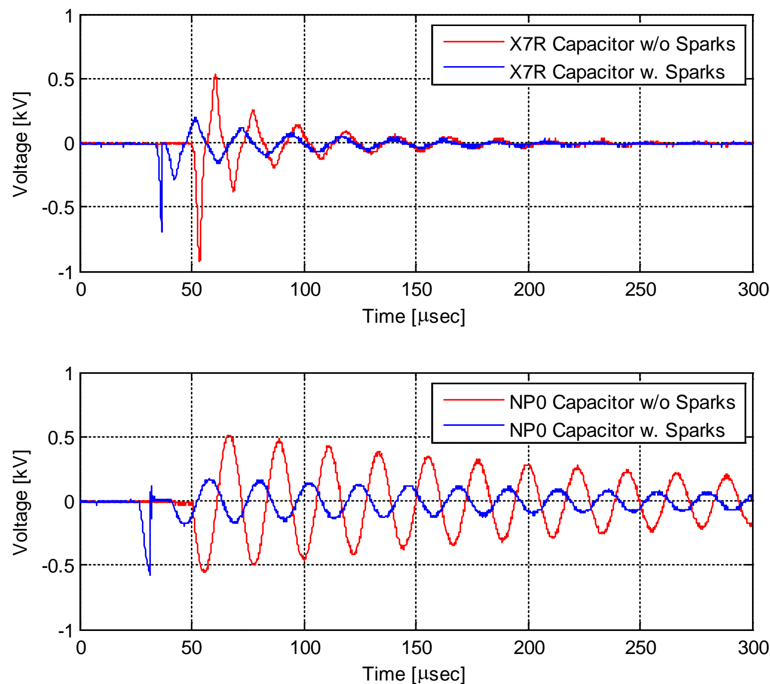


Fig. 2. Typical test voltage waveforms prior to a capacitor failure.

During some of the tests, a spark between the contacts of the HV relay would form as the relay opened. This would diminish the energy stored in the inductor resulting in a lower-amplitude oscillation as indicated by the blue curves in Fig. 2.

3. The Failure Pulse

3.1 Signature of a failure pulse

Due to the nature of the test, which repeatedly applied a high AC voltage (10 to 20 times the rated voltage) across the CUT, the exact failure pulse can be difficult to identify. In these tests, capacitor failures were defined in terms of the capacitor's leakage resistance and the voltage observed across the capacitor during the EFT pulses. After a pulse, if the measured low-voltage resistance across the terminals was less than 1/10 of the initial value, the capacitor was considered to have failed. The average insulation resistances measured at 1 kHz prior to the testing were 15 MΩ for 1-nF X7R capacitors, 1.3 MΩ for 10-nF X7R capacitors, 70 kΩ for 100-nF capacitors, and 70 MΩ for 10-nF NP0 capacitors.

A capacitor was also considered to have failed if the measured peak voltage of an EFT pulse was well below the expected value. For example, in Fig. 3, prior to pulse #3736, the resistance measured is not a full order of magnitude lower than its initial value. After pulse #3736, the resistance is 63 kΩ. According to the insulation resistance criteria, the capacitor failed at pulse #3736. However, as indicated in the lower plot in Fig. 3, a significant change in the capacitor behavior occurred during pulse #3726. The voltage waveform across the test capacitor is a brief spike and the ringing is over-damped. The capacitor was not able to sustain a high voltage even though its low-voltage insulation resistance was still high.

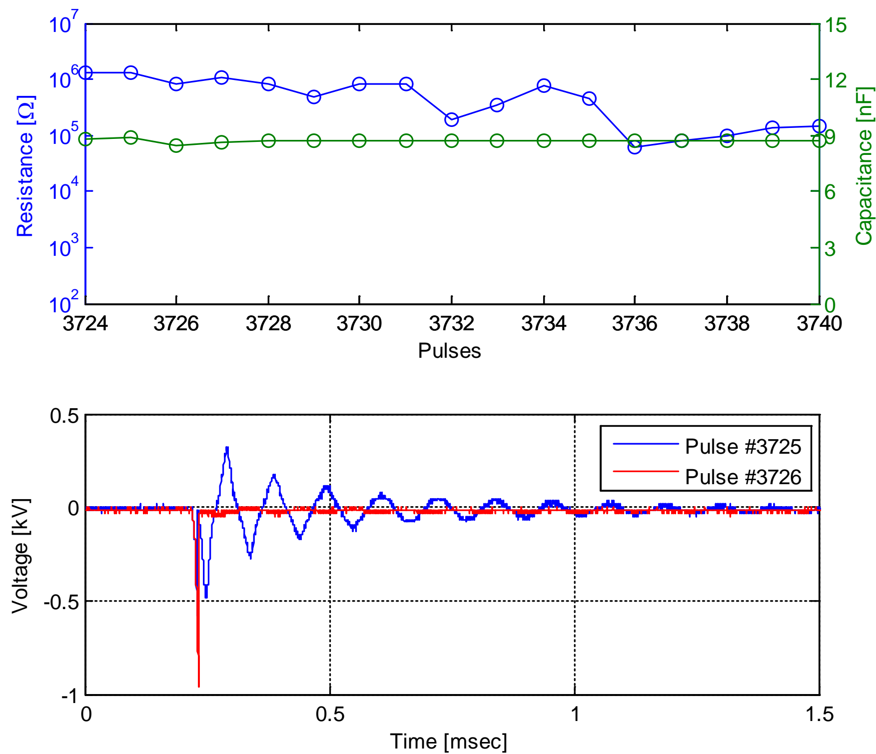


Fig. 3. Voltage waveforms before and after the failure and corresponding capacitance and resistance measurements for a 10-nF X7R capacitor.

3.2 Failure voltage

The failure voltages for different types of capacitors are described in Fig. 4. In this figure, the red line is the median; while the upper blue line and the lower blue line are the 75th percentile and the 25th percentile respectively. The upper black line and the lower black line are the extreme values ignoring outliers. A red cross indicates an outlier. The failure voltage for X7R capacitors decreases with the nominal value of the capacitor, varying from about 0.6 kV for 100-nF capacitors to about 1.3 kV for 1-nF capacitors. 10-nF X7R capacitors have a higher failure voltage than NP0 capacitors with the same nominal capacitance. It is important to note however, that the capacitance of X7R capacitors decreases with the applied voltage reducing the amount of energy, ½CV^2, stored. As a result, more energy is needed to damage NP0 capacitors compared to X7R capacitors with the same nominal capacitance. For example, about 1.8 mJ (stored in the inductor) was required to damage the 10-nF NP0 capacitors compared to just 0.6 mJ for the 10-nF X7R capacitors.

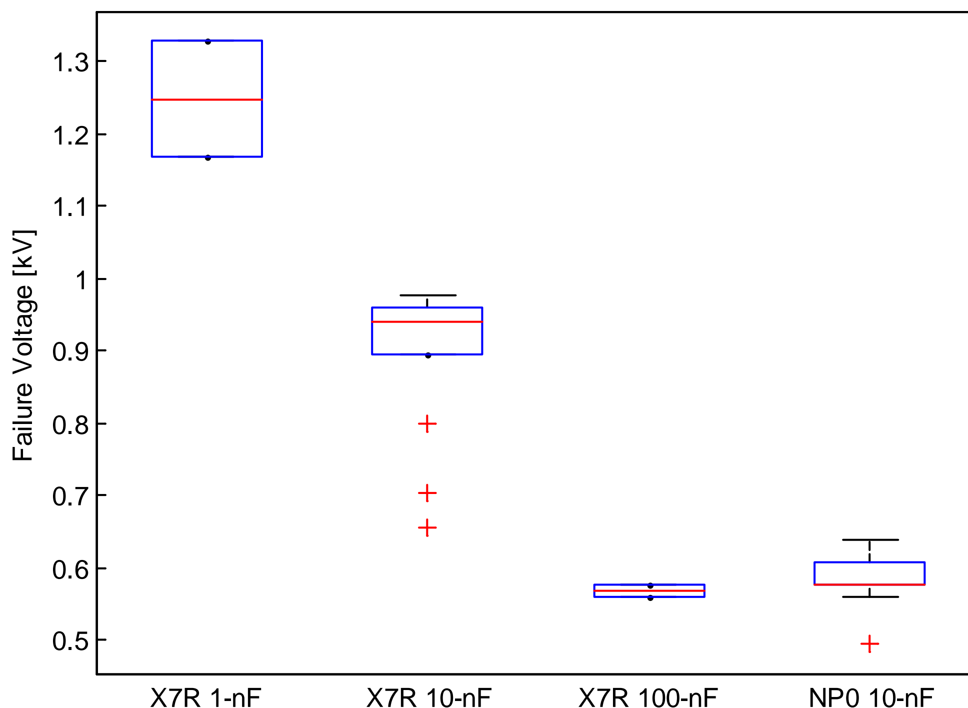


Fig. 4. Failure voltage of capacitors with different nominal values.

Eight capacitors of each type were evaluated by measuring the dielectric breakdown voltage (DBV) with a slowly ramping voltage. The average DBV for each type of capacitor is plotted in Fig. 5. As shown in the figure, higher valued X7R capacitors had a lower dielectric breakdown voltage. For lower-valued capacitors, the difference between the EFT failure voltage and the DBV is greater than it is for the higher-valued capacitors.

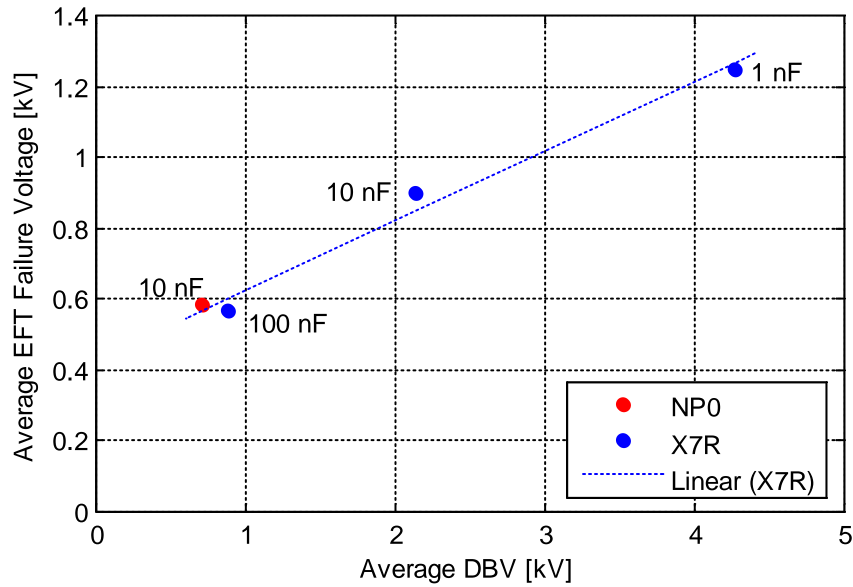


Fig. 5. Relationship of average EFT failure voltage to average dielectric breakdown voltage.

The value of the inductor used in the EFT test affects the resonant frequencies, but does not significantly affect the failure voltage for the various 10-nF capacitors in these tests. Fig. 6 shows the failure voltages for the 10-nF NP0 and X7R capacitors obtained with inductors of different values.

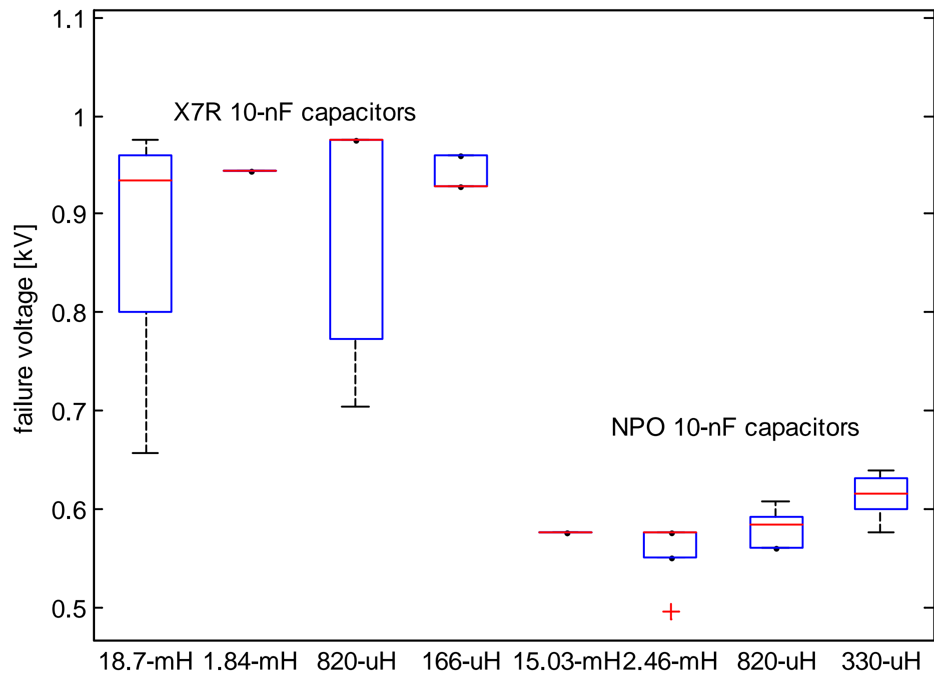
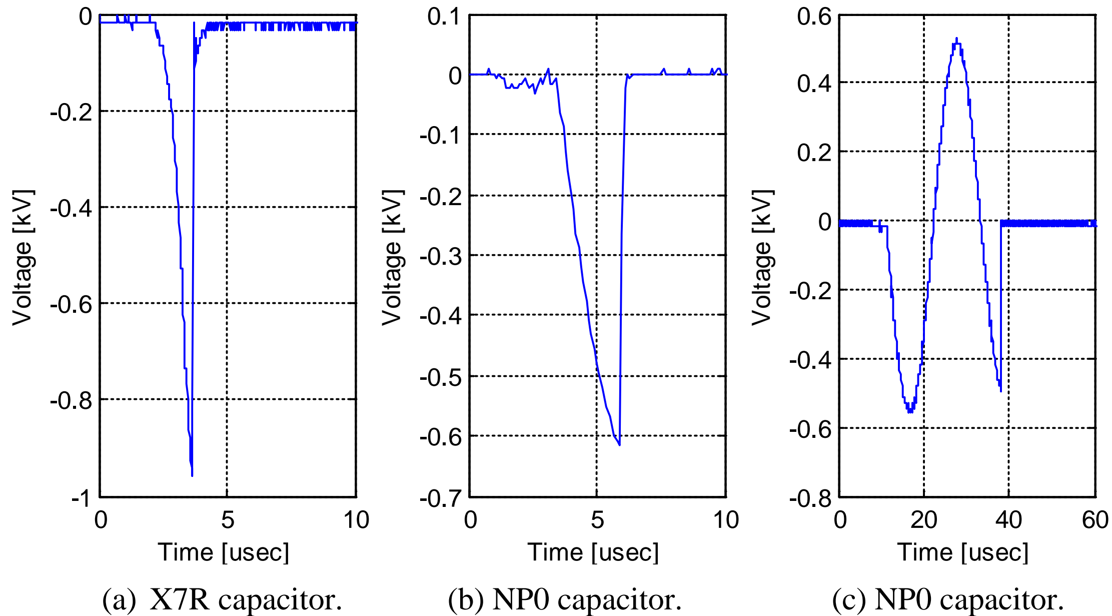


Fig. 6. Failure voltage of 10-nF capacitors grouped by value of the test inductor.

The waveform associated with the failure pulse varied depending on the type of capacitor. As shown in Fig. 7 (a), the failure of an X7R capacitor appears to occur at or before the first voltage peak. This was typical for X7R capacitors. Of the 22 failure waveforms recorded for NP0 capacitors, only 5 of them failed during the first voltage peak as shown in Fig. 7(b). The other capacitors survived the first voltage peak, which had the highest amplitude, and failed some time later as seen in Fig. 7(c). In one case, the test sample survived the first 4 cycles before shorting at a point where the voltage was at a relatively low level.



(a) X7R capacitor. (b) NP0 capacitor. (c) NP0 capacitor.

Fig. 7. Failure voltage waveforms.

4. Failure Characteristics

4.1 Degradation and recovery of post-failure resistance

One of the objectives of this study was to evaluate the degradation of insulation resistance that can occur when capacitors are subjected to high-voltage pulses. Fig. 8 shows the range of insulation resistances measured at 1 kHz with the LCR meter after the failure pulse. It indicates that the X7R capacitors generally failed with a resistance higher than 2 kΩ, while the NP0 capacitors failed with a much lower resistance (less than 1 Ω). Only 1 of the 25 NP0 capacitors tested failed with a high resistance (36 MΩ). The measured resistance of most X7R capacitors immediately after a failure was comparable to the measured value before the failure, but degraded quickly with subsequent pulses. X7R capacitors tended to behave like varistors or diodes after a failure, exhibiting a lower resistance when exposed to high voltages.

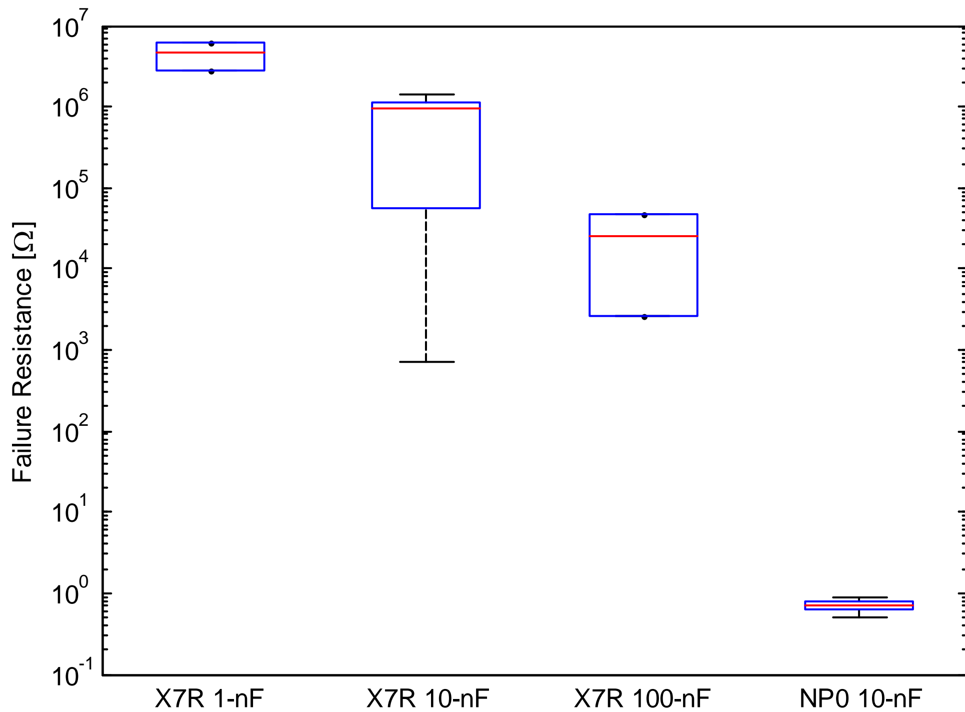


Fig. 8. Insulation resistance measured after the failure pulse.

The post-failure insulation resistance recovered fully or partially in 5 of the 25 10-nF X7R capacitors during the course of the testing. Fig. 9 shows that the insulation resistance of one X7R capacitor fully recovered from pulses #2200 to #2500 and from pulses #3000 to #3800 after the capacitor had failed at pulse #1500. A full recovery means that the measured resistance is at least as high as it was in the measurements before the failure. For NP0 capacitors, a full recovery was never observed. The insulation resistance only recovered partially and briefly as demonstrated in Fig. 10.

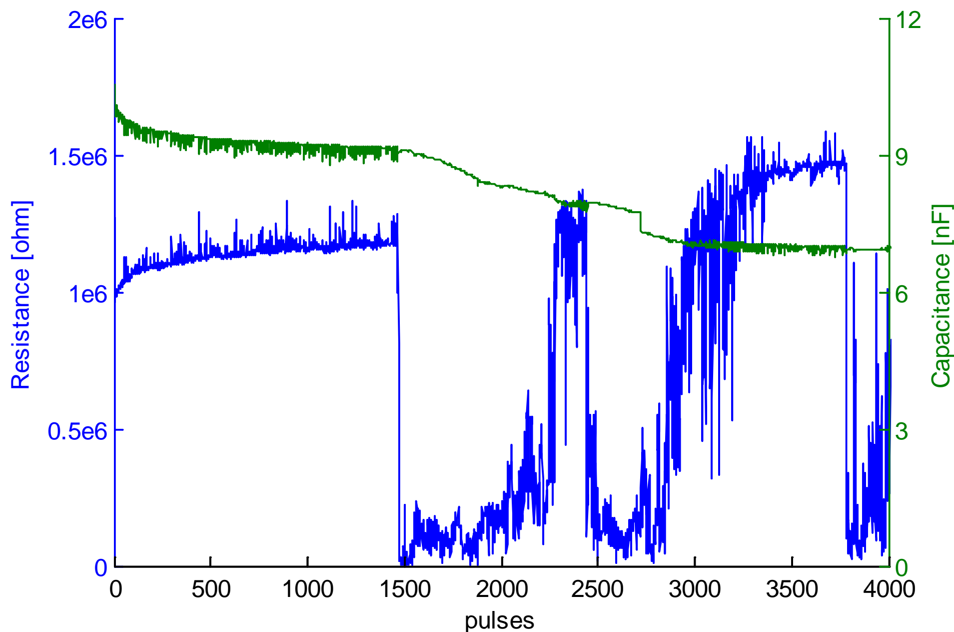


Fig. 9. Recovery of parallel resistance during the pulse testing of a 10-nF X7R capacitor.

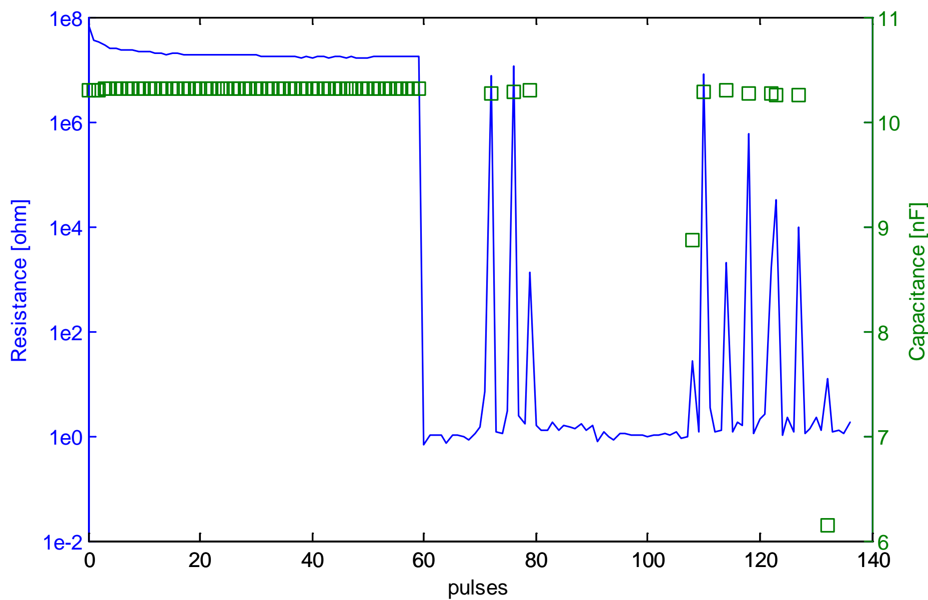


Fig. 10. Recovery of parallel resistance during the pulse testing of a 10-nF NP0 capacitor.

4.2 Degradation of capacitance

The capacitance of X7R capacitors was degraded during the course of the testing. Each of the X7R capacitors tested lost more than 10% of its initial capacitance after about 300 pulses. With the continued application of pulses after the failure pulse, four of the 10-nF X7R capacitors lost 90% of their initial capacitance, as shown in Fig. 11. For NP0 capacitors, no significant changes in the capacitance were observed during the course of the testing up to the point where a failure was observed. A degradation of capacitance after a failure could not be confirmed for the NP0 capacitors because the NP0 capacitors fail with a very low parallel resistance.

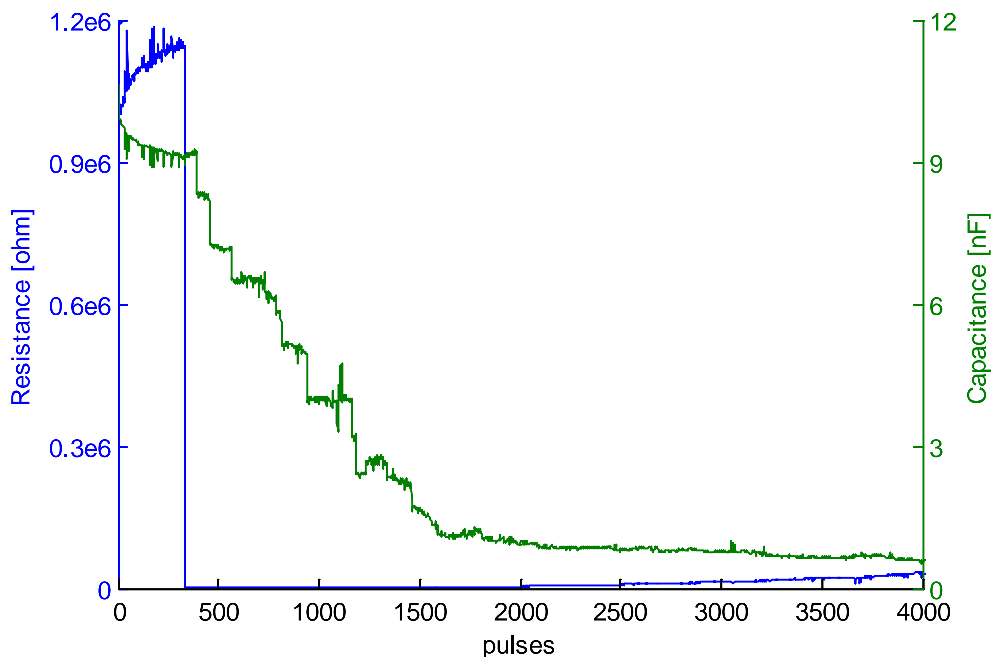


Fig. 11. Degradation of capacitance during the pulse testing of a 10-nF X7R capacitor.

4.3 Destructive physical analysis

Additional samples of 10-nF X7R and NP0 capacitors were tested and sectioned in order to gain insight to the possible causes of the EFT failures. The capacitors tested were soldered to a printed circuit board, subjected to EFT testing, and removed after the test by a hot air tool that increased the temperature gradually to avoid thermal stress. Loose capacitors were then potted in plastic matrix and slowly ground and polished to expose a cross-section of the internal layers. A control group of capacitors not subjected to EFT testing were mounted and removed from the printed circuit board using the same process. The control group capacitors were also sectioned and did not show any signs of thermal or mechanical stress.

Table 1. Results of electrical testing of sectioned capacitors.

Sample number	Capacitor type	Total pulses	Failure pulse number	Insulation resistance after the failure pulse (DC bias voltage)	Failure voltage
1	X7R	3560	70	677 kΩ (8.59 V)	899 V
2	X7R	56	15	18.4 kΩ (1.55 V)	892 V
3	X7R	180	172	128 kΩ (5.55 V)	890 V
4	X7R	5378	174	261 kΩ (7.14 V)	895 V
5	X7R	483	481	247 kΩ (7.03 V)	863 V
6	X7R	315	315	374 kΩ (7.79 V)	861 V
7	X7R	10	10	152 kΩ (5.97 V)	847 V
8	X7R	9	9	664 kΩ (8.57 V)	867 V
9	NP0	304	304	<1 Ω	528 V
10	NP0	99	99	<1 Ω	528 V
11	NP0	150	150	<1 Ω	551 V
12	NP0	241	238	<1 Ω	531 V
13	NP0	172	102	<1 Ω	528 V

The EFT test results are summarized in Table 1. The failure resistances of the X7R capacitors were generally more than 100 kΩ with the exception of sample number 2, which exhibited an 18.4-kΩ insulation resistance after failure. Samples #6, #7 and #8 were removed from the test immediately after the failure pulse. The sections of these capacitors were used to investigate how failures initiate. A section of sample #6 is shown in Fig. 12. The white arrows point out tiny cracks that have formed in the dielectric. They may be a) a secondary defect created by a large stress gradient due to the electrostrictive response when the part rapidly deformed during an electrical breakdown and discharge elsewhere within the device, or b) early stages of a primary defect where internal fractures form due to the electrostrictive response and/or adiabatic heating during the fast transient charging. These cracks then provide a breakdown path that effectively reduces the breakdown voltage between the electrodes. The location of the failure site is consistent with the conclusion drawn in [7] that electrical overstress failures are most likely to initiate at the ends of the internal electrodes. These locations have the highest electric field density and experience the greatest mechanical stress under transient voltages.

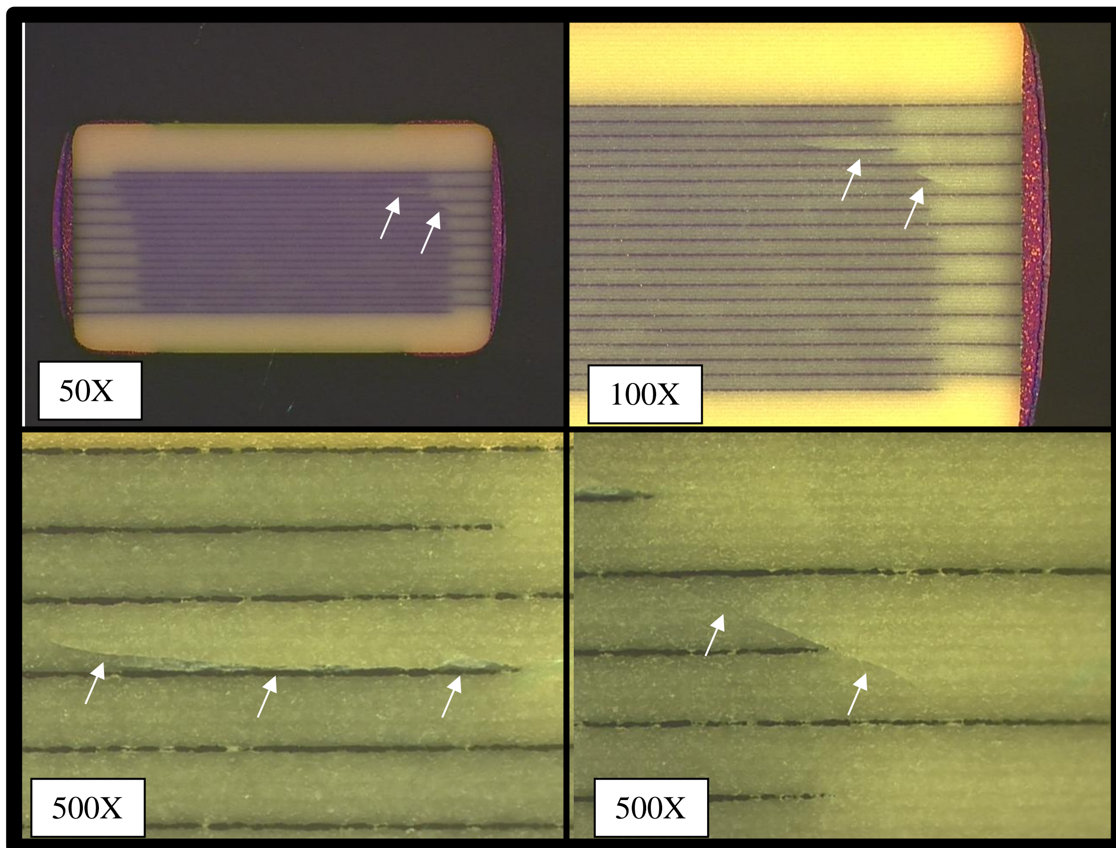


Fig. 12. Cracks at ends of internal electrodes of an X7R capacitor after a failure was observed.

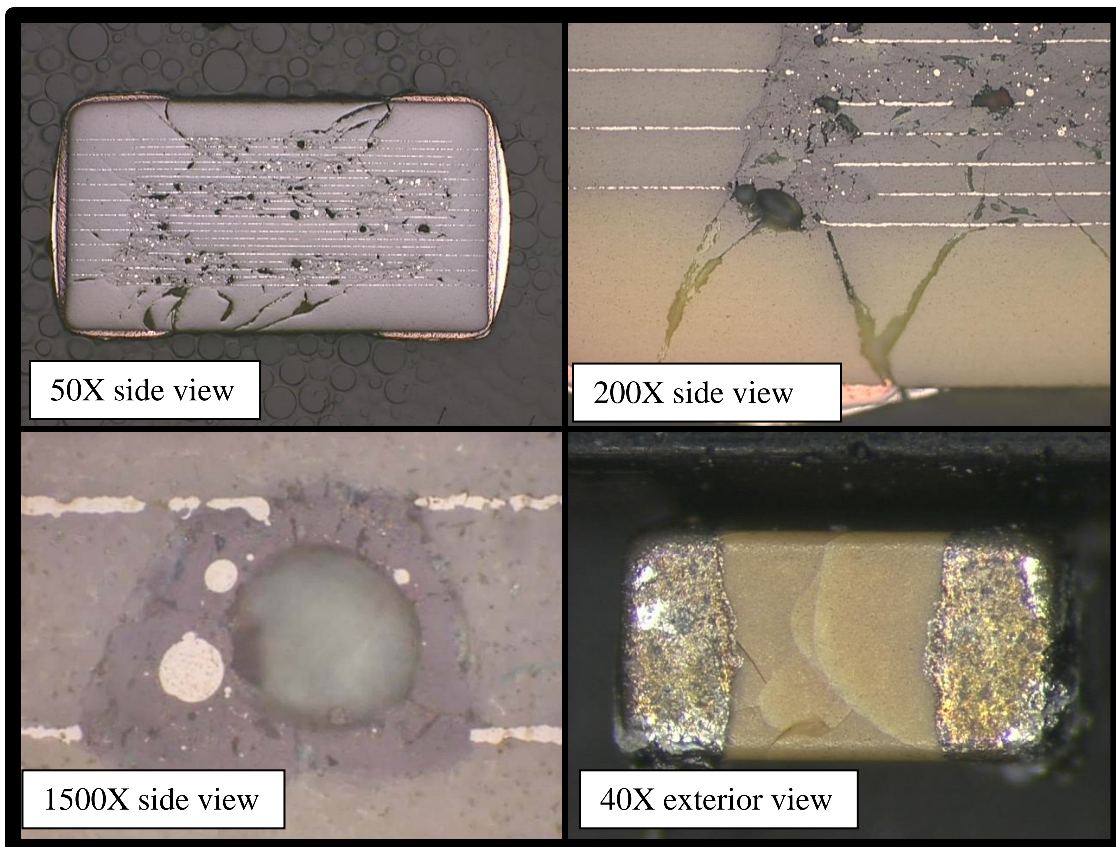


Fig. 13. Damage to an X7R capacitor exposed to 5000 pulses after the initial failure.

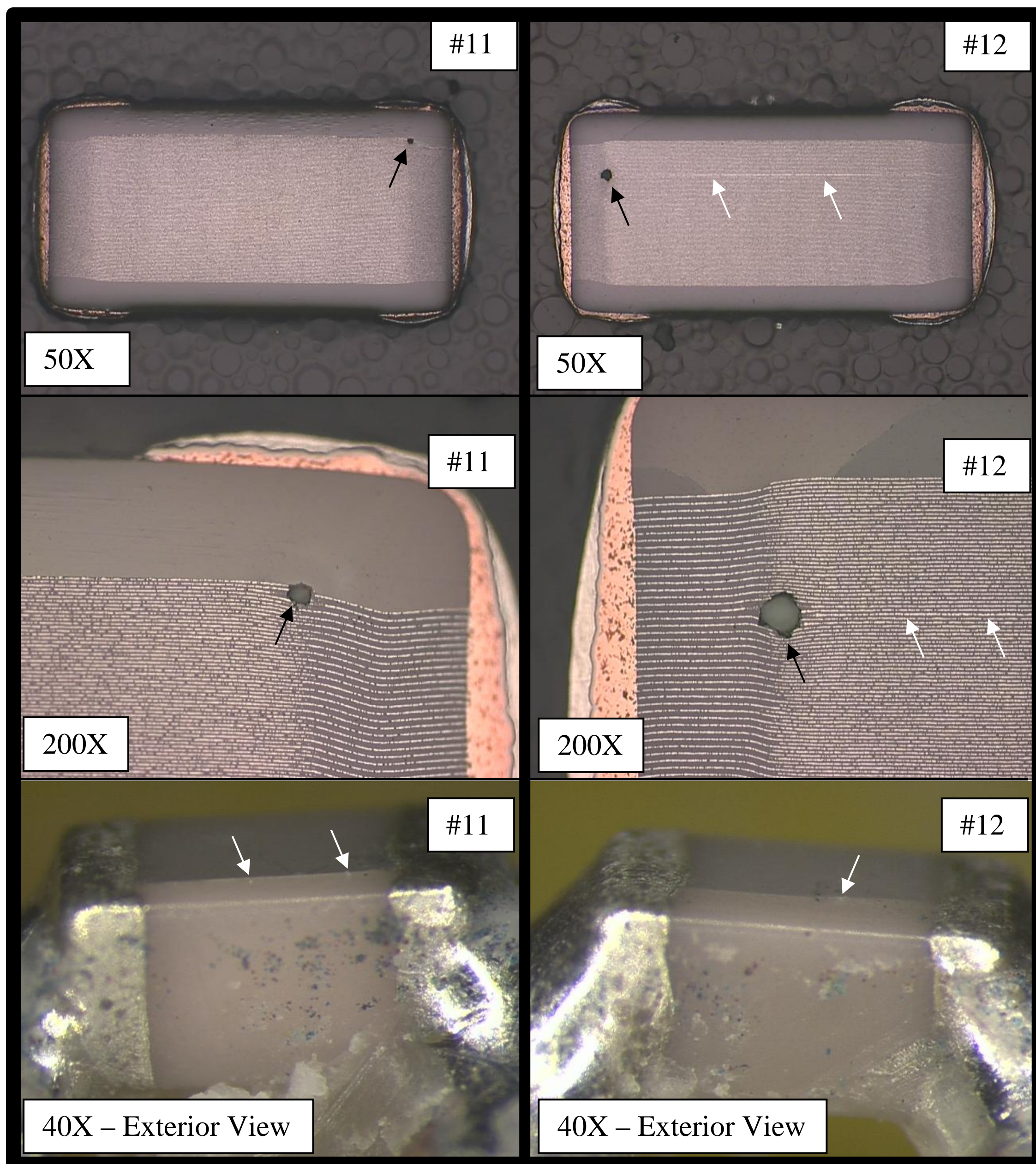


Fig. 14. Failure spots (black arrows) in NP0 capacitors after EFT pulses. White arrows indicate a crack along the ceramic-electrode interface, originating at the point defect at the high stress margin of termination electrodes.

With further pulses applied to a failed X7R capacitor, as seen in Fig. 13, severe cracks extended to the surfaces of the failed capacitor and evidence of very high temperatures were found in the interior of the device. High magnification views (esp. 1500x) of the failure region show an annular region around a spherical void formed in the dielectric between metal layers of opposing polarity (light-colored horizontal layers). Inclusions of spherical Ni metal (brighter areas) within the darker gray annulus (barium-rich region based on SEM-EDS analyses) derived from melted barium titanate dielectric provide evidence of extremely high temperatures caused by a spark discharge within the body of the capacitor. It is proposed that the areas of melted dielectric are chemically reduced, and thus contain a high concentration of oxygen-defect charge carriers. The insulation resistance of the failed X7R capacitor is controlled by the moderate resistance of the severely thermally damaged dielectric between the electrodes. Further, these regions likely are the source of the nonlinear resistance observed in post-

EFT IR testing due to the semiconductive behavior of reduced BaTiO3. Continued exposure of the degraded capacitor to EFT pulses causes the damaged areas to be “reworked”, extending the network of thermally induced fractures and melted regions of dielectric/metal. This accounts for the further degradation and the occasional recovery in the insulation resistance during EFT testing.

Fig. 14 shows the failure sites of two NP0 capacitors that were sectioned after the initial failure pulse. Both capacitors have a cavity / melted spot at the ends of the internal electrodes, which as noted earlier, is a region of very high electrical stress due to field concentration at the ends of the active electrodes. A parallel crack (as indicated by the white arrows in Fig. 14) formed along the internal electrodes associated with the failure spot, showing delamination of the capacitor in response to the point defect created by energy discharged at the end of the associated electrode. This crack is propagated to the exterior of the capacitor as a single planar fracture. In contrast to the X7R capacitors, where annular regions of melted BaTiO3 are observed around the cavity formed during the discharge, the more refractory zirconate-based dielectric in the NPO capacitor does not show severe localized melting around the cavity. It is postulated that vaporization and re-deposition of metal on the inner surface of the discharge cavity is the source of the low resistance path between closely spaced layers of alternating polarity in the failed NPO capacitors.

5. Equivalent Circuit Model

5.1 Circuit model

A plot of the I-V curve of a failed X7R capacitor shows that the insulation resistance is a function of the applied voltage. The resistance decreases with an increase in the bias voltage and is independent of the polarity of the bias voltage. This behavior can be modeled as two identical diodes with opposite polarities in parallel as shown in Fig. 15. The relationship between the current and voltage of the circuit can be expressed as,

$$I = I_S\left(e^{\frac{V}{nV_T}} - e^{-\frac{V}{nV_T}}\right) \tag{1}$$

where I_S is the saturation current of one diode, V_T is the thermal voltage with an approximate value of 26 mV at room temperature, and n is the emission coefficient. Fig. 16 shows how the curve-fit model results compare to the measured I-V curve of a failed X7R capacitor.

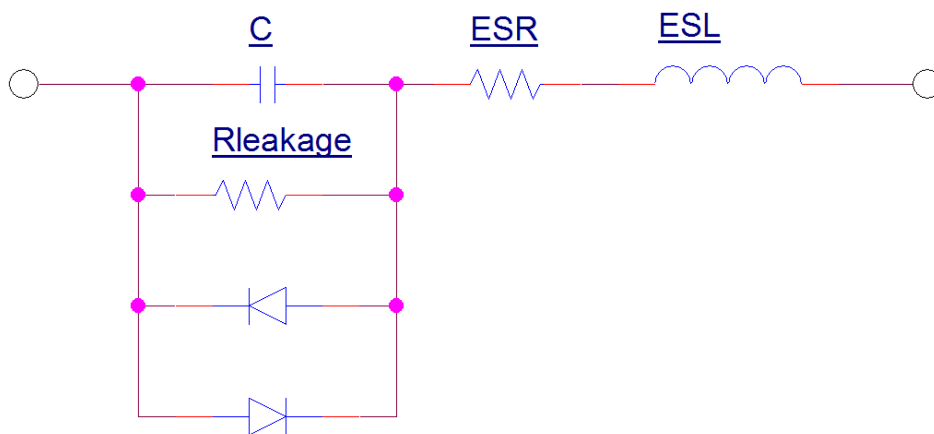


Fig. 15. Equivalent circuit of a failed X7R capacitor.

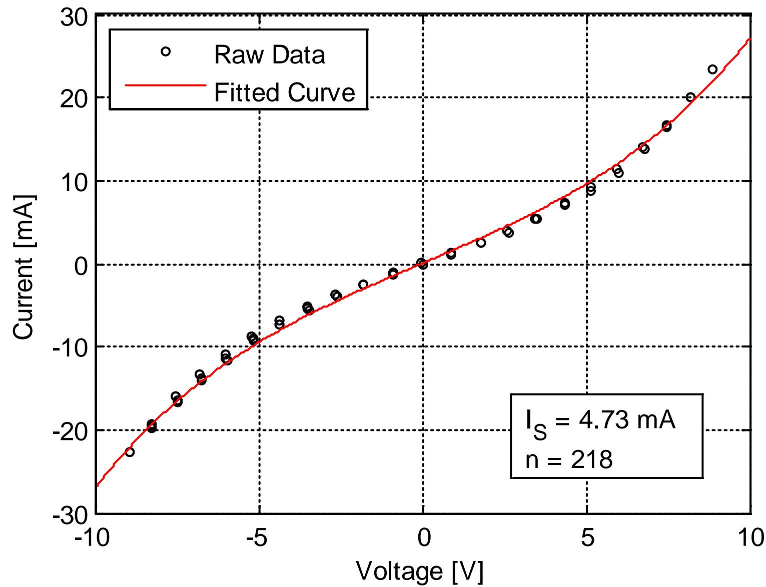


Fig. 16. Curve fit of an I-V characteristic for a failed 10-nF X7R capacitor.

5.2 Model validation

To evaluate the proposed circuit model of a failed X7R capacitor at frequencies other than DC, the passive low-pass filter circuit illustrated in Fig. 17 was measured with a failed capacitor and simulated using the two-diode model of Figs. 15 and 16. The input voltage was a sinusoidal waveform superimposed on a 4.67-V DC offset.

Fig. 18 plots the average voltage across C2 as a function of the peak-to-peak voltage of the applied sinusoidal waveform. At 0 Vp-p, the applied voltage is simply 4.67 VDC. The low insulation resistance of the failed capacitor reduces the output voltage to 3.36 VDC. As the amplitude of the applied sinusoidal waveform is increased, it is partially rectified by the non-linear capacitor impedance. The rectified waveform decreases the average value of the voltage dropped across C2. Higher rectification effects were observed at lower frequencies. As indicated in Fig. 18, the two-diode model simulation results are in close agreement with the measurement results.

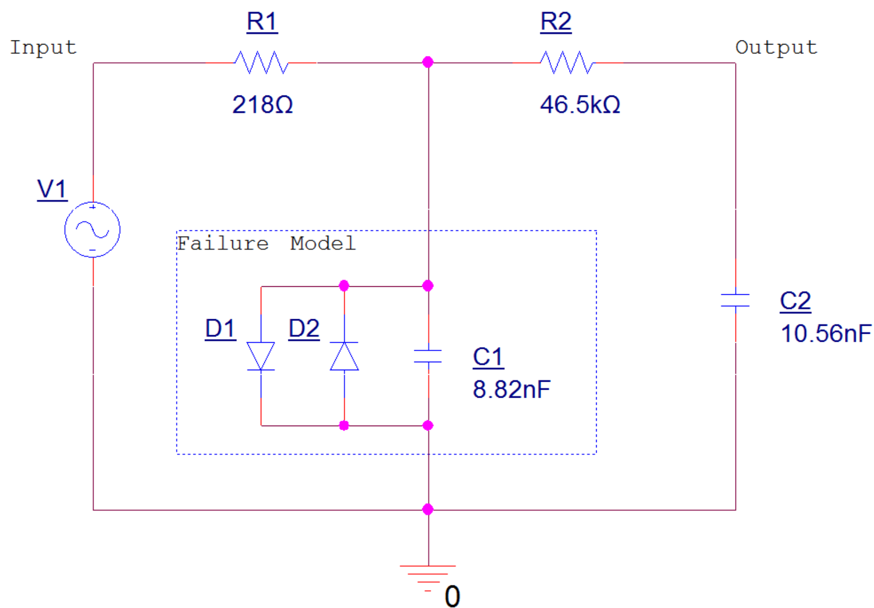


Fig. 17. Test circuit for validation of the failure model of X7R capacitors.

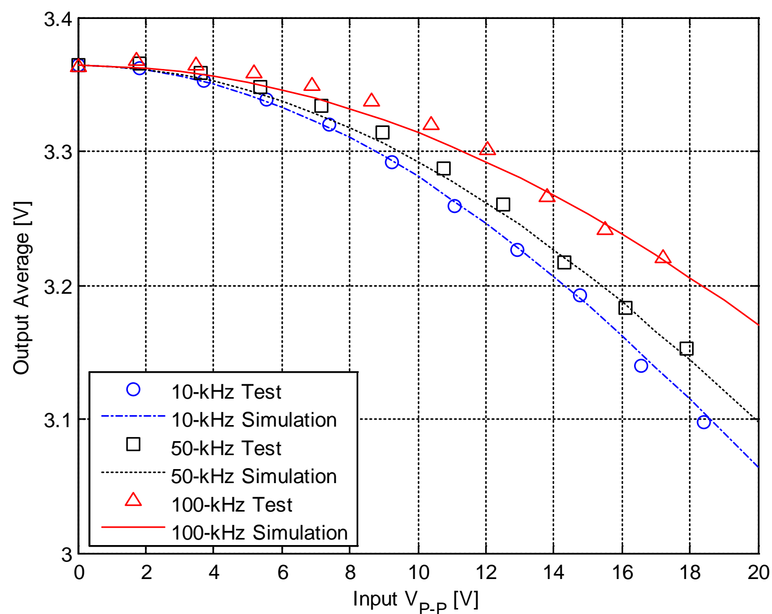


Fig. 18. Comparison between the measurement and the model simulation.

6. Conclusions

The failure voltages and failure modes of X7R and NP0 capacitors exposed to a series of electrical fast transients were analyzed in this paper. Most of the failures for X7R capacitors occurred at the peak of the applied voltage waveform. X7R capacitors with lower capacitances failed at higher voltages. Most of the X7R capacitors tested did not exhibit an obvious decrease in insulation resistance immediately following the failure pulse, though their resistance tended to drop significantly with the repeated application of pulses after the failure. X7R capacitors sometimes recovered their insulation resistance fully or partially during post-failure pulses. More than a 10% degradation in capacitance was commonly observed for X7R capacitors subjected to repeated EFTs. Some X7R capacitors lost about 90% of their initial capacitance during the course of the testing. Cracks were found at the ends of the

internal electrodes in a failed 10-nF X7R capacitor when testing was halted after the first indication of a failure. Regions of melted and recrystallized barium titanate are believed to be responsible for the non-linear relationship between the insulation resistance and the applied voltage. Further pulses applied to failed capacitors caused severe cracks and burned the dielectrics.

For a given capacitance (10-nF), NP0 capacitors failed at lower voltages than X7R capacitors. NP0 capacitors often failed as short circuits. NP0 capacitors were less likely to recover with the repeated application of pulses, and recovered only partially and briefly. Capacitance degradation was not observed in NP0 capacitors.

The failure resistance of X7R capacitors showed a nonlinear behavior. Increasing the bias voltage applied on the capacitor decreased the failure resistance. A simple model of this nonlinear behavior consisting of two identical diodes demonstrated a good fit with measured results.

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