CVEL

THE CLEMSON UNIVERSITY VEHICULAR ELECTRONICS LABORATORY

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Electrical Behavior of Multi-Layer Ceramic Capacitors Damaged by Electrostatic Discharge

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Abstract

This report investigates the electrical behavior of multi-layer ceramic (MLC) capacitors subjected to electrostatic discharge (ESD). The degradation of MLC capacitors subjected to repeated discharges manifests itself as a non-linear resistance. The leakage current in degraded capacitors increases exponentially with an applied voltage. The I-V characteristics of these capacitors are symmetric with voltage and independent of the polarity of the ESD discharges responsible for the degradation. A model for a degraded capacitor consisting of two parallel diodes with opposite polarities is proposed.

1. Introduction

Multi-layer ceramic (MLC) capacitors are widely used in electronic devices, especially in automotive electronics due to their high reliability, small size and low cost compared to other types of capacitors. With the increasing demands for a high-level of product integration and component miniaturization, MLC capacitor design is evolving and newer capacitors are made with ceramics that have a higher dielectric constant, higher number of stack layers, increasing overlap area between internal electrodes and thinner dielectric layers [1]. These changes require a renewed focus on the effects of electric overstress (EOS) such as electrostatic discharge (ESD). Also, the use of these capacitors in safety-critical systems has generated interest in modeling their electrical behavior after a failure has occurred.

In other studies examining the failure of MLC capacitors, efforts have been mainly focused on mechanical overstress (MOS) [2] and highly accelerated life tests (HALT) [3], [4], [5]. During HALT testing, ceramic capacitors experience degradation not only in their capacitance, but also in their insulation resistance due to Schottky barriers formed between the dielectric material and electrodes [6] and oxygen vacancies [7].

ESD is an important consideration when designing any electronic component or device that will perform a safety-critical role. However, the failure mechanisms of MLC capacitors under ESD stress has not been widely documented. There are only a few published studies on this topic. One of these studies, [8], concluded that the rate of failure (defined as not meeting the initial resistance requirements) increases with an increase in the cumulative maximum voltage on the capacitor during tests where charge was not removed from the capacitor between discharges. In this study, 1000 X7R capacitors (0805 1-nF and 1206 10-nF) were exposed to five ESD strikes of each polarity. The authors found no significant difference in failure rates when testing with a human body model (150-pF/1500-ohm) network or a machine model (200-pF/no resistive component). A study described in [9] was a further investigation of [8]. In this paper, continuously increasing voltage pulses were applied to capacitors, until the dielectric broke down and the capacitor became a short circuit. The authors demonstrated factors affecting a capacitor's vulnerability to ESD transients by testing capacitors with different voltage ratings, dielectric materials, and package sizes. The authors suggested using NP0 capacitors with high voltage ratings (preferably 200 V) and large package sizes (preferably 1206) for ESD protection.

In [10], an ESD test consisting of 10 discharges followed by another 10 discharges of opposite polarity at a frequency of 10 Hz was used to characterize NP0/X7R MLC capacitors with 50-V or 100-V ratings and packages sizes from 0402 to 0805. Failures were determined by a test sample's inability to meet capacitance, dissipation factor or insulation resistance requirements. It was found that capacitors with higher voltage ratings outperformed capacitors with lower voltage ratings, and capacitors with larger package sizes outperformed smaller ones. In [11], a degradation in capacitance was observed in tests where the ESD levels were gradually increased from +/- 0.5 kV to +/- 5.0 kV in 0.5-kV increments. In [12], resistive shorts occurred in 0603 MLC capacitors with nominal values of

680 pF and 10 nF subjected to a 15-kV ESD test. That paper proposed a model consisting of a capacitor and a shunt resistor to represent the defective capacitor.

This paper demonstrates that MLC capacitors that have failed due to ESD generally exhibit a highly non-linear behavior. The paper begins by describing the test and measurement procedures used to evaluate the capacitors in this study; then presents failure levels for MLC capacitors from different manufactures. The I-V characteristics of defective capacitors are presented and an equivalent circuit for modeling degraded capacitors is proposed.

2. Measurements

2.1 ESD test setup and samples

A human body model ESD stress was applied to MLC capacitors using a 150 pF/330 Ω ESD simulator configured as shown in Fig. 1. A contact discharge was used to minimize the variation of energy passing through the capacitor from one test to another. The capacitors were covered with silicone gel to avoid an air or surface discharge between the terminals of the capacitor. MLC capacitors with rated values of 1 nF, 10 nF and 100 nF were obtained from three manufacturers. All capacitors in this study were Type II X7R capacitors with 0603 packages and 50-V ratings. Tests were conducted on 8 samples of 1-nF and 10-nF capacitors and 3 samples of 100-nF capacitors.

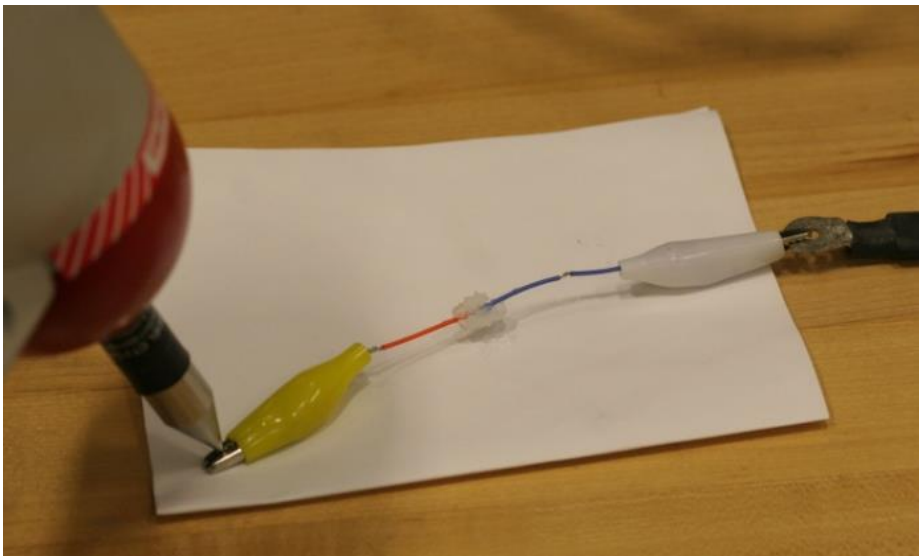


Fig. 1. ESD test setup with the capacitor under test covered with silicone gel.

2.2 Measurement procedure

A contact discharge was applied to the capacitor under test (CUT) starting at a voltage level that was not likely to destroy the test sample. These starting voltage levels were determined by trial tests in which no samples were damaged by a single strike at a given ESD level, for example, +2 kV for 1-nF capacitors. The voltage level was increased in steps of either +1 kV or +2 kV to determine the failure voltage for each capacitor. Table 1 shows the test sequence used for capacitors with different nominal values.

Table 1: Test sequence for capacitors with different nominal values

Step	1 nF	10 nF	100 nF
1	+2 kV	+8 kV	+18 kV
2	+3 kV	+ 9 kV	+20 kV
3	+4 kV	+ 10 kV	+22 kV
4	+5 kV	+ 11 kV	+24 kV
5	+6 kV	+ 12 kV	+26 kV
6	+7 kV	+ 13 kV	+28 kV
7	+8 kV	+14 kV	+30 kV
8	+9 kV	+15 kV	-
9	+10 kV	+16 kV	-
10	+11 kV	+17 kV	-

After each test, the DC resistance of the capacitor was measured using an LCR meter. The capacitor was considered to be damaged if the measured resistance was less than 10 MΩ. If it was not damaged, the test was continued at the next voltage level, and this was repeated until the capacitor was damaged. For example, on a 1-nF capacitor, the test was started at 2 kV and incremented in steps of 1 kV until reaching the observed failure voltage level, which ranged from 4 kV to 7 kV. Defective capacitors were connected to a voltage divider circuit as shown in Fig. 2. An applied DC voltage was varied from 0 to +60 V while measuring the voltage across and current through the capacitor to obtain the I-V curve. The capacitor was tested in both polarities, with the applied voltage magnitude represented by the waveform in Fig. 3. The current flow through the sample determined from the voltage across R2. The voltage was calculated from V1 and V2.

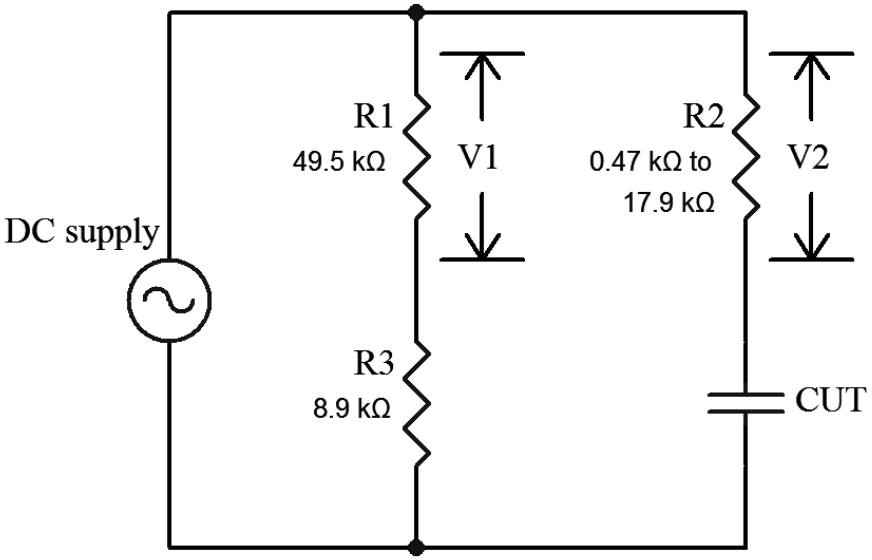


Fig. 2. Test circuit for evaluating degraded capacitors.

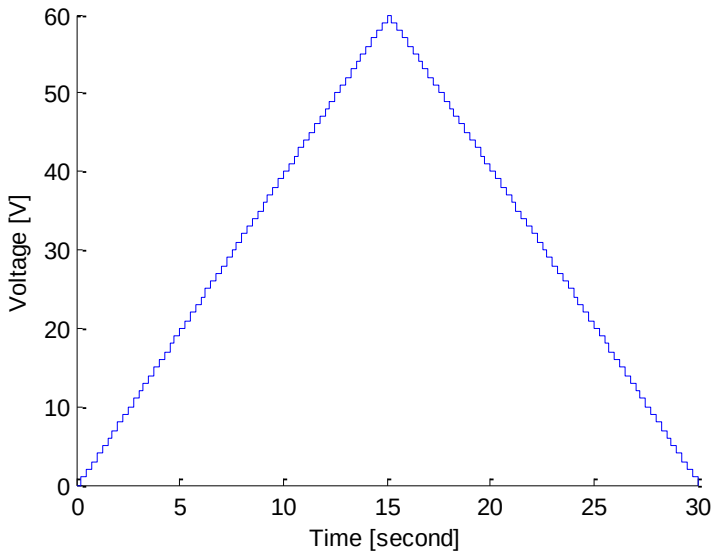


Fig. 3. Applied test waveform from the DC supply.

3. Results and Discussion

3.1 ESD test levels to degrade the capacitors

The failure voltage levels corresponding to ESD tests on capacitors with 1-nF and 10-nF rated values from different manufacturers are shown in Fig. 4 and Fig. 5, respectively. The results indicate consistent failure levels of 4 kV and 15 kV for 1 nF and 10 nF capacitors, respectively, from manufacturer B. For manufacturers A and C, there was some variation in the failure levels. None of the 100-nF capacitors tested were damaged at any level. All of them withstood the maximum 30-kV discharge.

Eight capacitors of each type from the same lots were tested to determine their dielectric breakdown voltage (DBV) using a slowly ramping applied voltage. The results are summarized in Fig. 6. 1-nF capacitors had higher DBVs but failed at lower ESD voltage levels than 10-nF capacitors. This is likely due to the fact that a 10-nF capacitor is able to hold more charge at a given voltage level. Thus with the same level of charge injection, the maximum voltage across a test capacitor during an ESD event is lower for larger-valued capacitors. As indicated in Fig. 6, there didn't appear to be any correlation between the DBV and the ESD failure level for capacitors of the same nominal value.

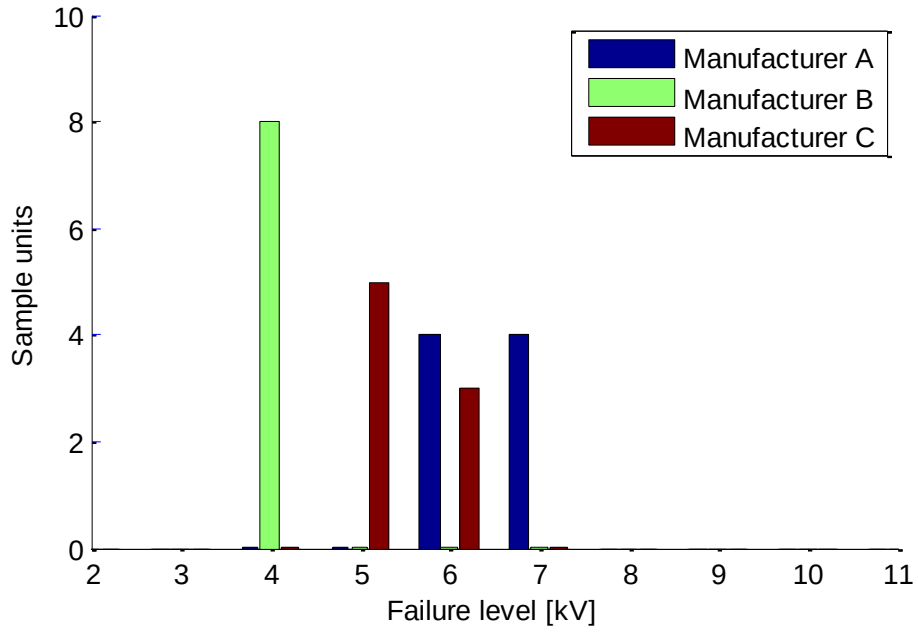


Fig. 4. Histogram of contact ESD failure voltage levels on 1-nF capacitors.

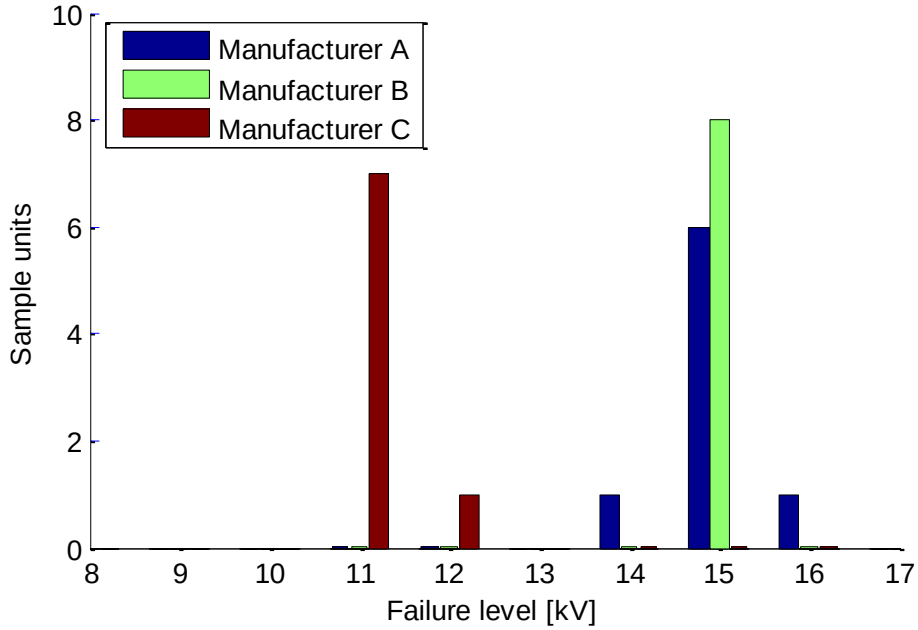


Fig. 5. Histogram of contact ESD failure voltage levels on 10-nF capacitors.

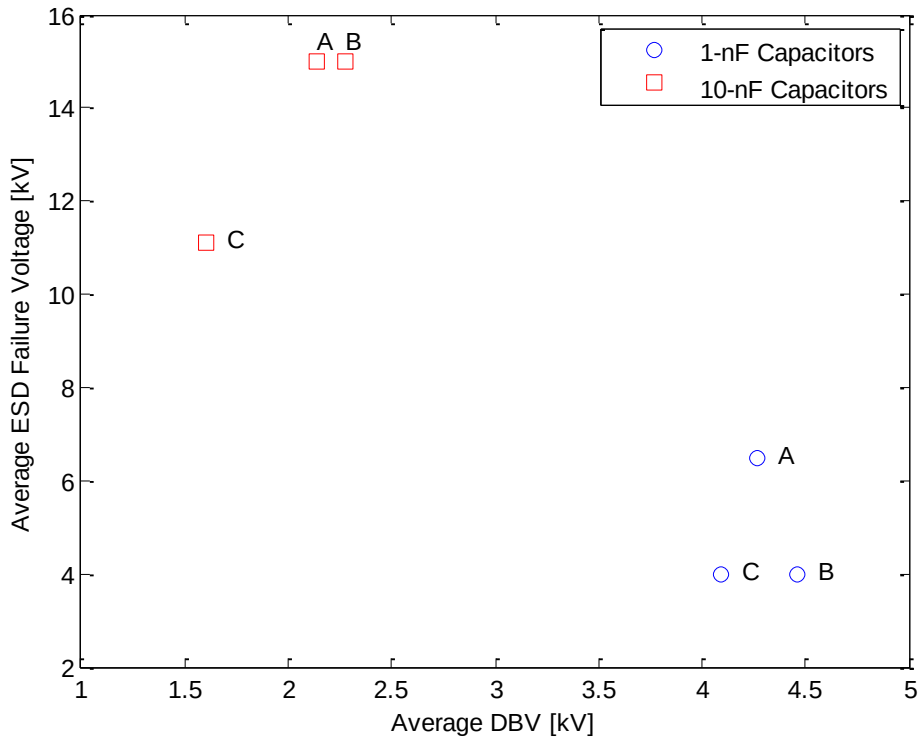
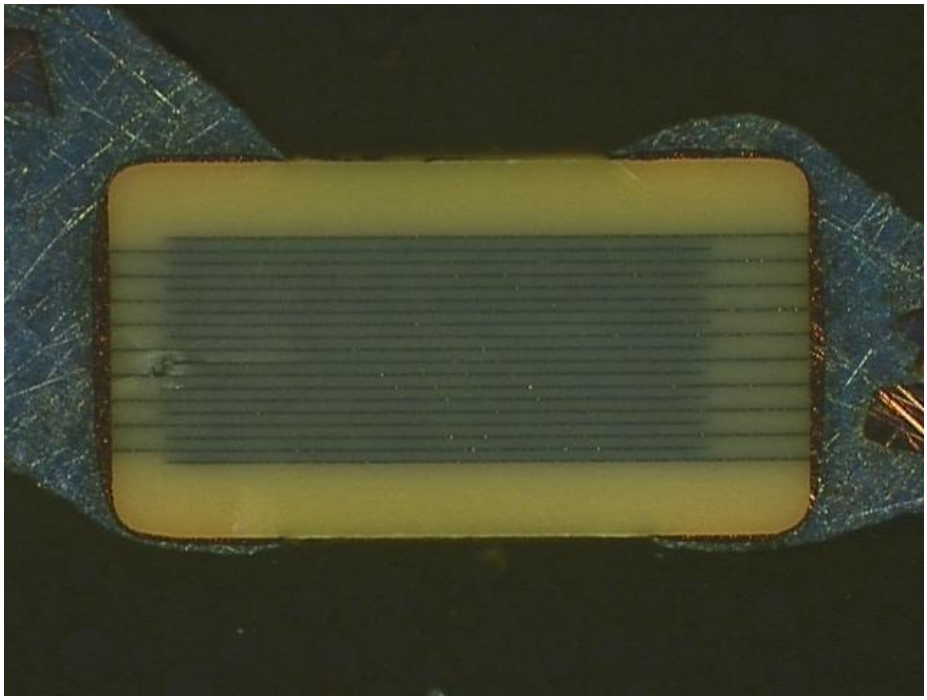


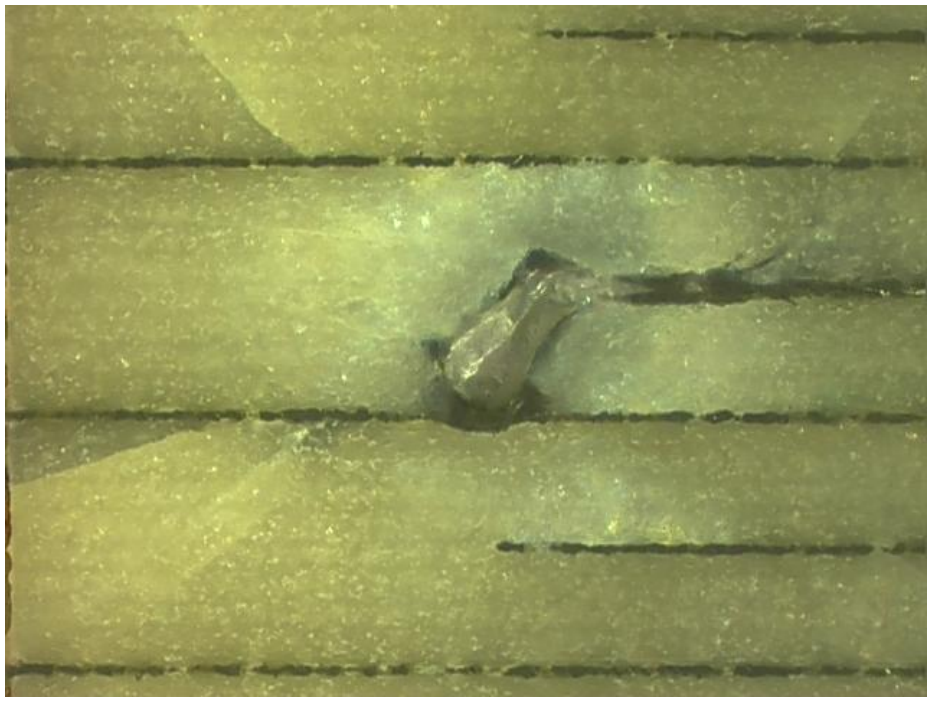
Fig. 6. Comparison between average ESD failure levels and average DBVs.

3.2 Destructive Physical Analysis

Three 10-nF capacitors from manufacturer A that had failed after being exposed to ESD transients were sent for a destructive physical analysis. The analysis involved grinding and polishing sections of these ceramic capacitors in order to identify possible defects in their structure. As indicated in Fig. 7, failed capacitors exhibited cracks in the dielectric at the edges of one or more internal electrodes. The locations of the failure sites indicate weak points in the capacitor in terms of electrical and mechanical stress during an ESD strike. This is in line with a simulation result in [13] that demonstrates that the ends of the internal electrodes exhibit the highest electric field density and mechanical stress under applied transient voltages.



(b) With a 50x amplification.



(b) With a 500x amplification.

Fig. 7. Site of an ESD failure in a 10-nF capacitor.

3.3 Non-linear resistive characteristics

The I-V characteristics of damaged 1-nF and 10-nF capacitors are shown in Fig. 8 and Fig. 9, respectively. In these figures, a non-linear resistance between the capacitor terminals is observed. The plots are highly symmetric as demonstrated by Fig. 10, which overlays plots of the current due to the forward and reverse voltages for two sample capacitors. Comparing Fig. 8 and Fig. 9, it is also worth

noting that the 10-nF capacitors from different manufacturers exhibited very different behavior, but the behavior was consistent for capacitors from any given manufacturer.

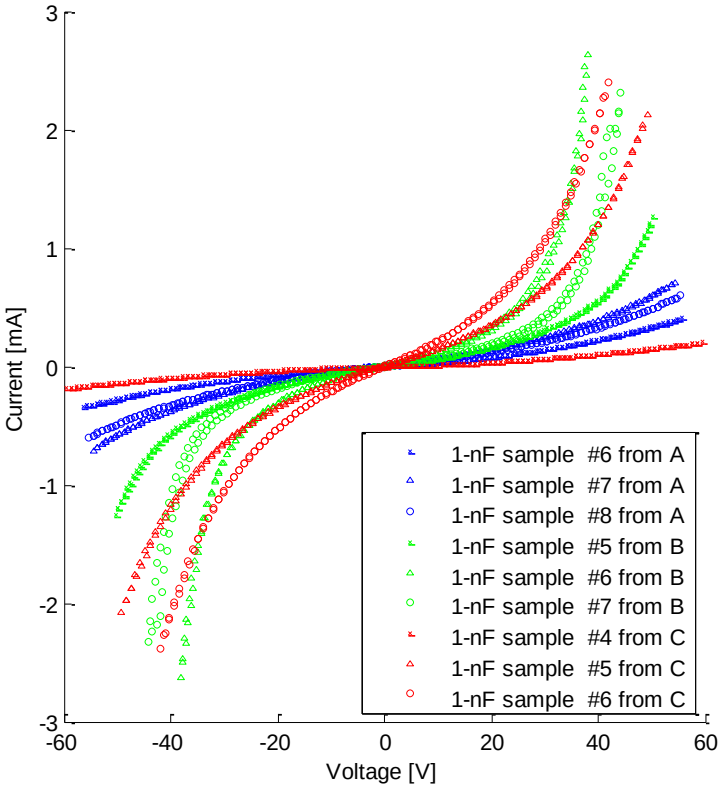


Fig. 8. I-V characteristics of 1-nF defective capacitors.

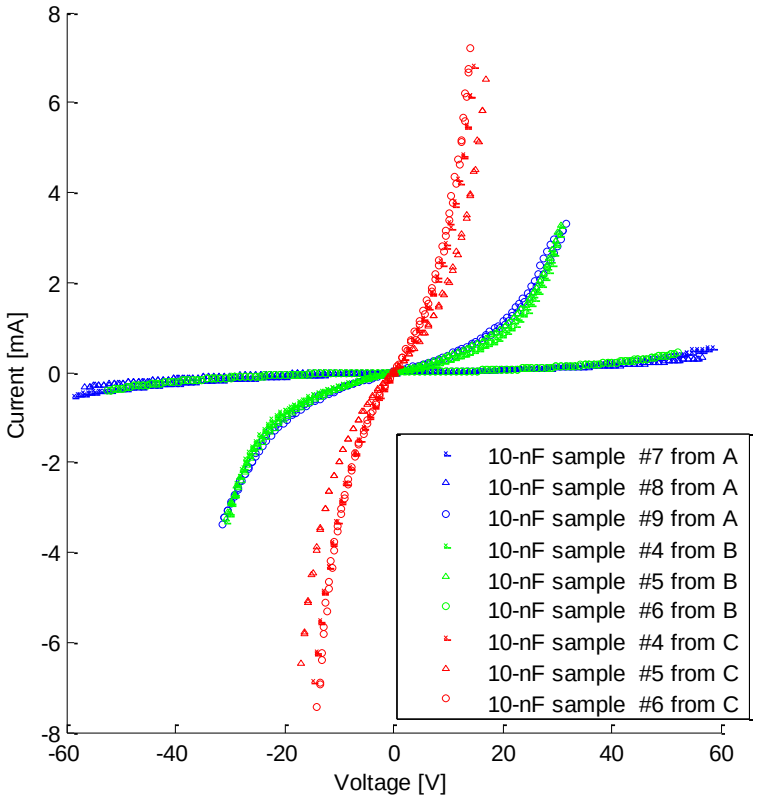


Fig. 9. I-V characteristics of 10-nF defective capacitors.

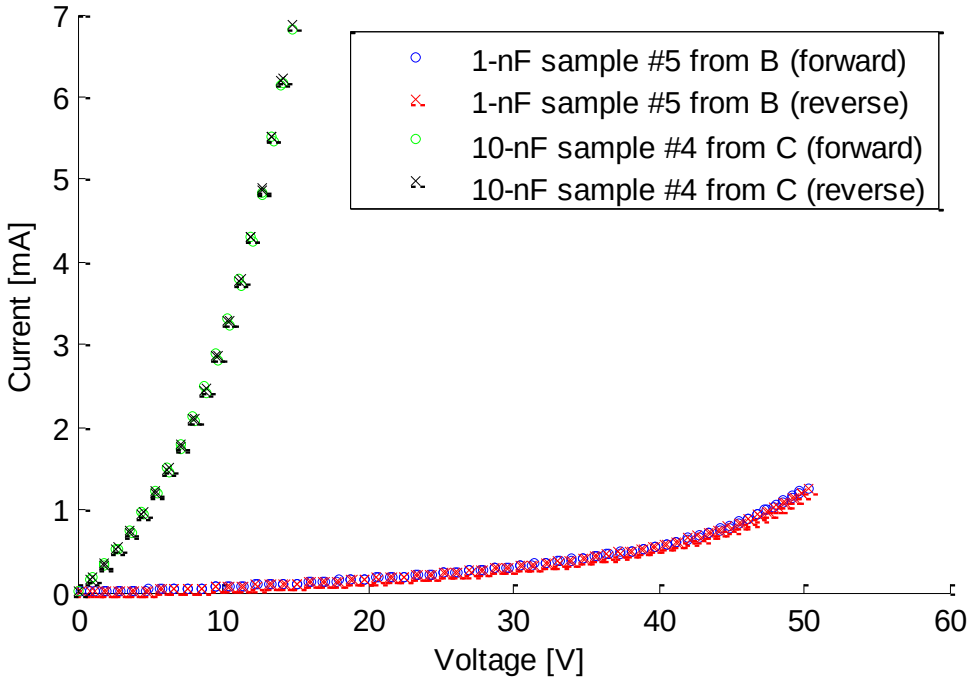


Fig. 10. Symmetric characteristics of the I-V curves.

3.4 Equivalent circuit of defective capacitors

Considering the exponential increase in current with the increase in applied DC voltage, the behavior of the degraded capacitors can be modeled with a pair of diodes as shown in Fig. 11.

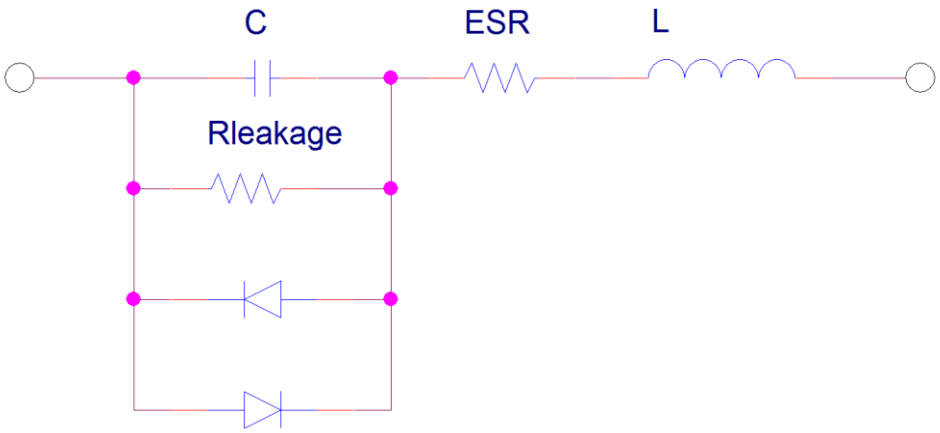


Fig. 11. Equivalent circuit of a degraded capacitor.

At very low frequencies, the connection inductance (L) and equivalent series resistance (ESR) are neglected. A large-valued shunt resistor ($R_{leakage}$) is used to model the initial leakage current (before the capacitor fails). In the degraded capacitor, this resistance can be neglected because the current flowing through the diodes in the model of the degraded capacitor is much higher than the leakage current represented by $R_{leakage}$. The I-V characteristics of the failed capacitors can then be modeled with two identical diodes. The relationship between the current and the voltage across these diodes can be written as,

$$I = I_S\left(e^{\frac{V}{nV_T}} - e^{-\frac{V}{nV_T}}\right) \quad (1)$$

where I_S is the saturation current of one diode, V_T represents the thermal voltage (with an approximate value of 26 mV at room temperature), and n is the emission coefficient. These parameters can be readily specified in SPICE diode models. Using a series expansion, Equation (1) can be approximated by eliminating the higher order components to yield,

$$I \approx \frac{2I_S}{nV_T}V. \quad (2)$$

Thus, the DC resistance R_{0V} with a small DC bias voltage applied is,

$$R_{0V} = \frac{nV_T}{2I_S}. \quad (3)$$

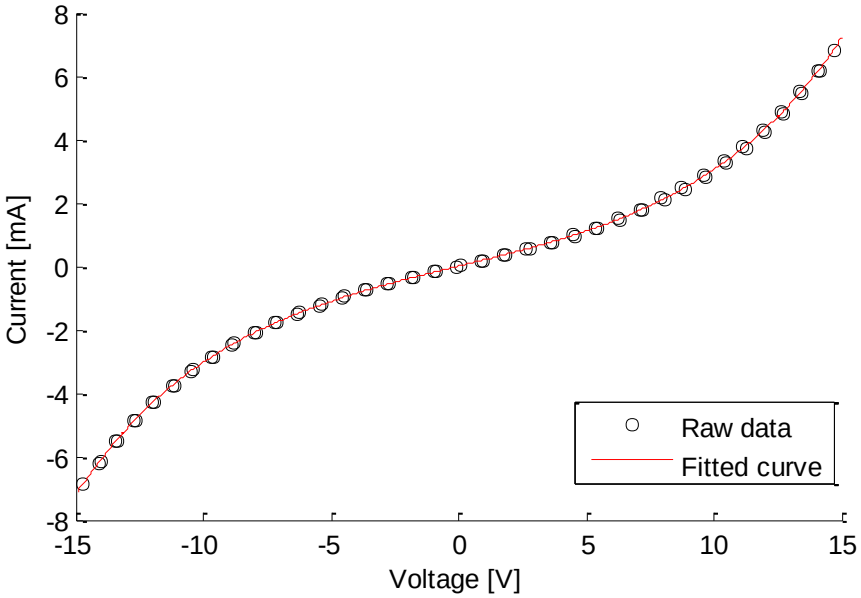


Fig. 12. Curve fit of I-V characteristics for the 10-nF sample capacitor #4.

The coefficients, I_S and R_{0V}, in the proposed model were derived for the degraded capacitors in this study. Assuming room temperature, the emission coefficient was obtained using Equation (3). The values obtained for the 1-nF and 10-nF capacitors from each manufacturer are provided in Table 2 and Table 3, respectively. Fig. 12, which shows the I-V characteristics of the 10-nF sample #4 from manufacturer C, shows that the model does a good job of fitting the measured data. The root-mean-square error (RMSE), defined as the square root of the mean square difference between the modeled and measured values, is also listed in the tables. The low values of RMSE indicate good fits of the model with the measurements. From the data in Table 2 and Table 3, it can be observed that, 10-nF capacitors are more likely to have low fault resistances at a small bias voltage than 1-nF capacitors.

Table 2: Model parameters (I_S and R_{0V}), model effectiveness (RMSE) and emission coefficient (n) for 1-nF capacitors

CUT	A #6	A #7	A #8	B #5	B #6	B #7	C #4	C #5	C #6
I_S (mA)	0.0477	0.0705	0.0742	0.0394	0.0177	0.0086	0.0244	0.1144	0.1466
R_{0V} (kΩ)	280.0	166.0	176.6	187.1	218.4	463.7	572.2	73.98	51.24
RMSE (mA)	0.0197	0.0074	0.0044	0.0212	0.0757	0.0943	0.0062	0.0139	0.0127
n	1057	927	1038	584	306	316	1105	670	595

Table 3: Model parameters (I_S and R_{0V}), model effectiveness (RMSE) and emission coefficient (n) for 10-nF capacitors

CUT	A #7	A #8	A #9	B #4	B #5	B #6	C #4	C #5	C #6
I_S (mA)	0.0381	0.0200	0.1574	0.0737	0.1197	0.0230	0.5942	0.3906	0.5354
R_{0V} (kΩ)	290.6	503.0	32.60	55.45	39.13	392.2	5.043	7.726	5.044
RMSE (mA)	0.0122	0.0047	0.0639	0.0621	0.0502	0.0061	0.0458	0.0527	0.1424
n	877	797	406	324	371	714	237	239	214

4. Conclusion

This paper describes and models the electrical behavior of MLC capacitors degraded by electrostatic discharge. Damaged capacitors exhibited a non-linear insulation resistance that could be accurately modeled using identical parallel diodes with opposite polarity. The proposed model for ESD

damaged capacitors can be readily implemented in circuit simulation software and employs diodes with only two extracted parameters.

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