

TECHNICAL REPORT: CVEL-15-067

Preliminary Investigation of Mounted Decoupling Capacitor Pole Locations with the Matrix Pencil Method

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Abstract

Tracking the pole location associated with the impulse response of a passive device can be an effective way of detecting component degradation. In this report, the impulse response of a test board with two decoupling capacitors is evaluated. The Matrix Pencil Method is used to extract the poles. The goal of this study is to establish whether the pole locations can be correlated with properties of the capacitors that might be used to identify a defect.

1. Introduction

Printed circuit boards can have dozens of decoupling capacitors connected to the power distribution bus in parallel with many active devices. It can be very difficult to detect when decoupling capacitors on a circuit board have been degraded (e.g. due to electrical transients or mechanical stress). This report investigates the possibility of detecting the degradation of mounted decoupling capacitors by tracking the poles associated with power bus resonances. Pole locations are identified using the Matrix Pencil Method (MPM) to analyze the power bus impulse response. In [1], a similar technique was used to identify degradation in MOSFET transistors.

As a first step towards ascertaining the effectiveness of this method, a simple case is investigated. This report presents measurements of the impulse response of a simple test board consisting of two solid planes and one or two mounted capacitors. The test board has two edge-mounted SMA connectors for pulse injection and observation. The board is pinged with a voltage step that has a very sharp rise time. This pinging caused the capacitors on the board to ring at a particular frequency with a certain damping factor. When this ringing is analyzed using the MPM, the complex poles associated with this ringing are identified [1]. The preliminary results presented in this report are intended to evaluate the concept of identifying poles associated with specific mounted decoupling capacitors.

2. Test Board Description

The test board is 4" x 3" and has mounting pads for five 0805 capacitors and two edge-mounted SMA connectors. One capacitor location is in the center of the board, and the rest are at various distances from the center. For each capacitor location, one of its pads is connected to the top plane and the other connects to the bottom plane through a via. Fig. 1 illustrates these connections in schematic form, while Fig. 2 shows the board layout. The spacing between the planes is approximately 0.060 inches, and the measured interplane capacitance of the board is approximately 230 pF.

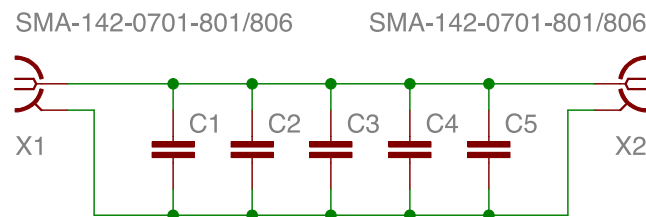


Fig. 1. Test board schematic.



Fig. 2. Test board layout.

3. Test Setup Description

Fig. 3 shows a picture of the test setup, which consists of a Picosecond Pulse Labs Model 2600 pulse generator, a 20-dB attenuator, two 50- Ω coaxial cables with SMA connectors, the test board, and a Tektronix oscilloscope. The 20-dB attenuator is placed between the test board and the oscilloscope to protect its input, and the built-in attenuator of the pulse generator was set to 20 dB to prevent overdriving the capacitors on the test board.

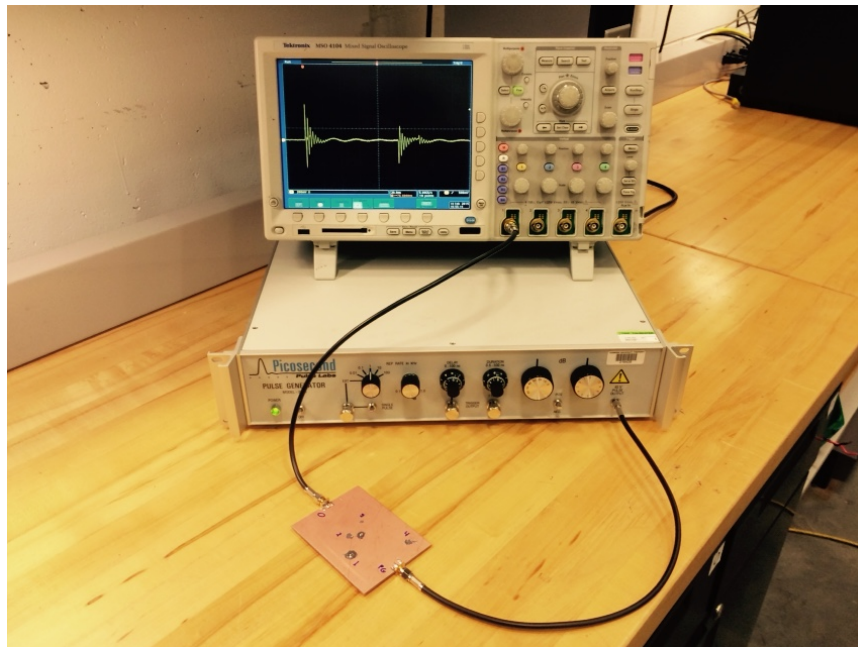


Fig. 3. Picture of test board and test setup.

To characterize the pulse source, the setup in Fig. 3 was used with a barrel connector in place of the test board. Fig. 4 shows the measured pulse from the source. The 10–90% risetime of the pulse is on the order of 0.5 ns.

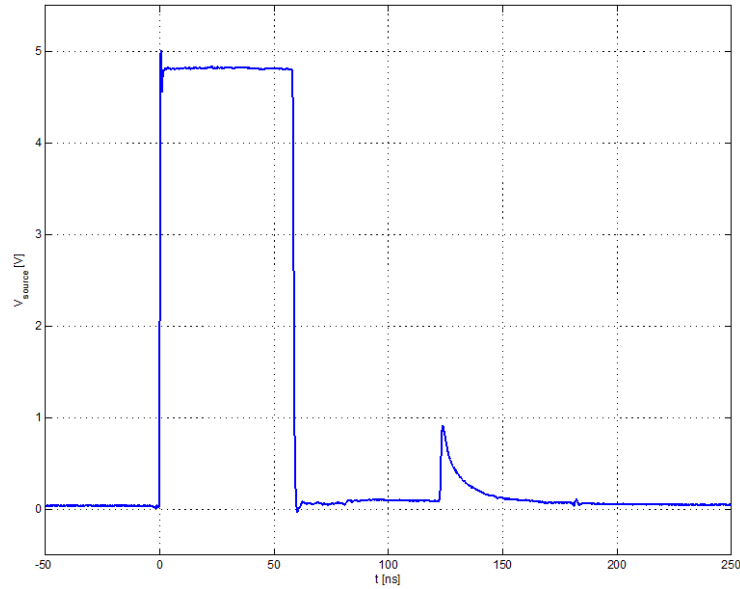


Fig. 4. Pulse source characterization.

The artifact in Fig. 4 at approximately 120 ns is a property of the pulse source. It remains present at 120 ns regardless of the length of cable between the source and oscilloscope. Because it is consistent in its location, this artifact can be easily identified and its impact minimized in these tests.

Fig. 5 shows the time-domain response of the test board with a 2.2-nF X7R capacitor in the center of the board, and a 1- μ F X5R capacitor in position 4. The blue portion of the waveform was captured and analyzed using the Matrix Pencil Method. The blue portion of the response begins 2 ns after the start of the low-to-high pulse transition. This was done to avoid the part of the waveform affected by the nonlinear source transition.

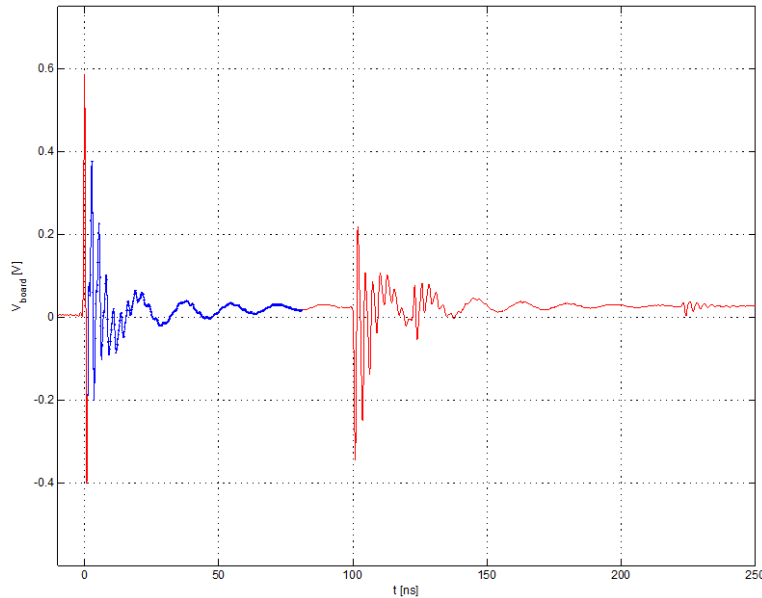


Fig. 5. Time-domain response of test board with 2.2-nF and 1- μ F capacitors.

The poles calculated using the MPM are shown in Fig. 6. The poles at approximately 370 MHz and 740 MHz are both cavity resonances associated with the planes. The pole at approximately 58 MHz is

due to the resonance of the 2.2-nF capacitor with the connection inductance of the 1-μF capacitor. The measurement suggests that this connection inductance is approximately,

$$L = \frac{1}{C \cdot (2\pi f)^2} = \frac{1}{(2.2 \text{ nF}) \cdot (2\pi \cdot 58 \text{ MHz})^2} \cong 3.4 \text{ nH} \quad (1)$$

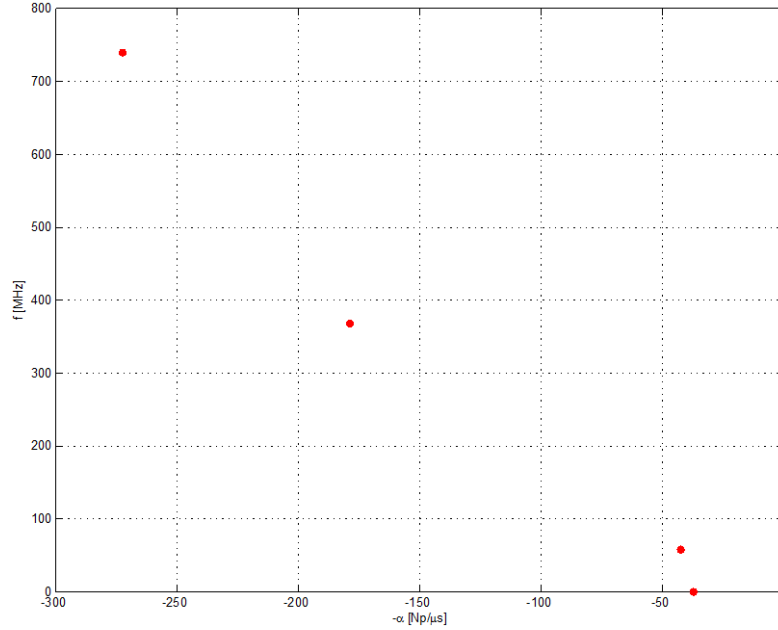


Fig. 6. MPM poles of test board with 2.2-nF and 1-μF capacitors.

Because the 58 MHz resonance is the one involving the two discrete capacitors, it will be the main pole of interest for the tests in the following sections. A close-up of this main pole of interest showing the frequency and damping constant values more accurately is provided in Fig. 7.

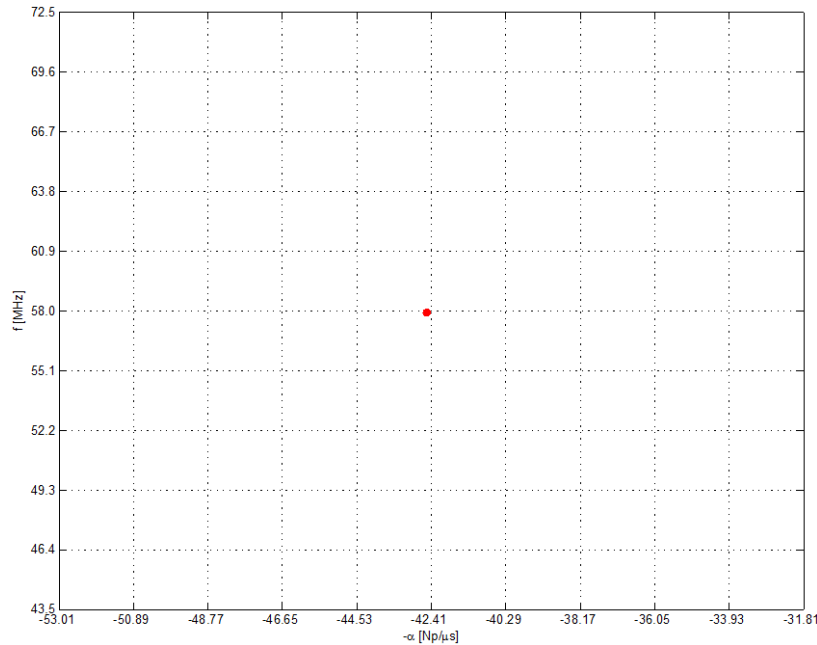


Fig. 7. Main MPM pole of interest of test board with 2.2-nF and 1-μF capacitors.

4. Changing the Pulse Strength

To determine the level at which the discrete capacitors would be driven into nonlinearity, the test setup described in the previous section was subjected to pulses with different amplitudes. Fig. 8 shows the step responses obtained with different settings of the pulse generator's built-in attenuator.

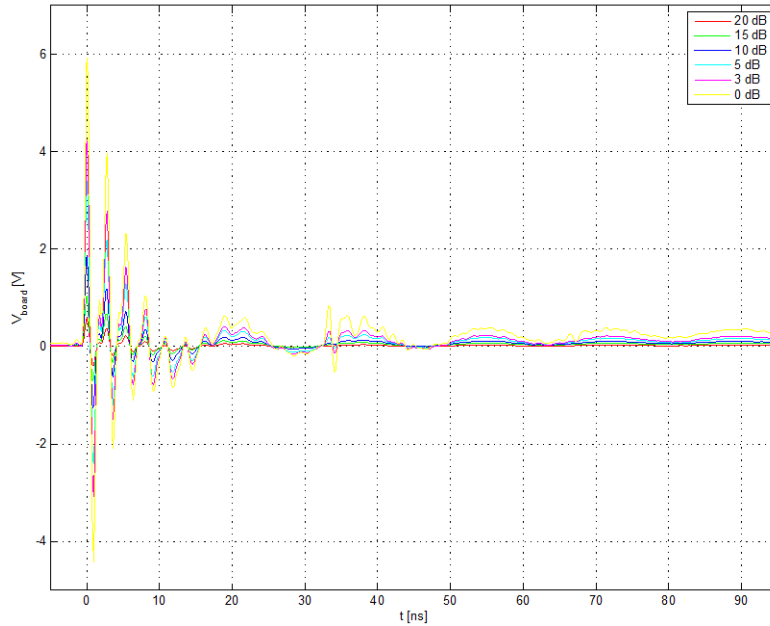


Fig. 8. Time-domain response of test board for different pulse strengths.

From Fig. 8, it appears that the test board responses for different levels of attenuation vary mostly in amplitude without much difference in the ringing frequency or damping. This is seen clearly in Fig. 9, which shows the MPM pole locations. The spacing between tick marks in Fig. 9 is approximately 5% of the nominal location for both frequency and damping. Overall, it appears that there is less than 1% variation in the frequency and less than 2% variation in the damping constant for these pole locations.

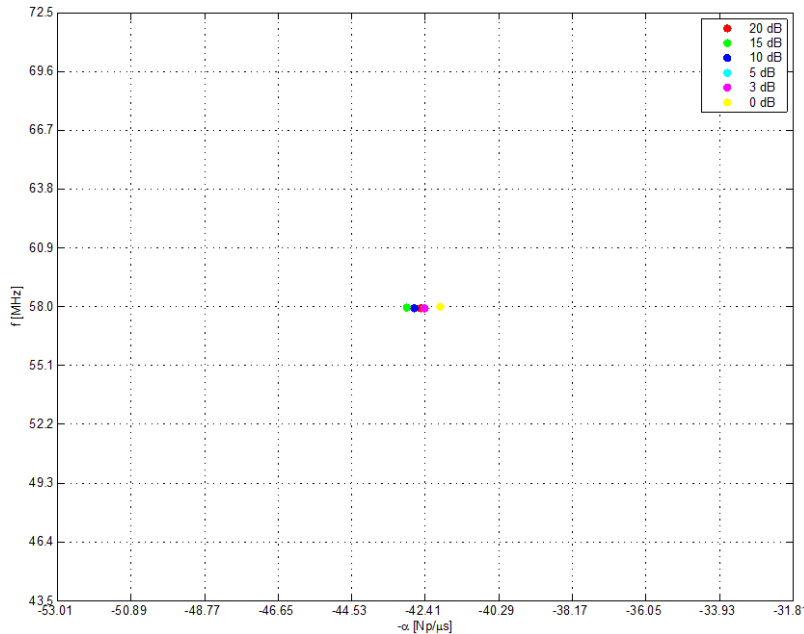


Fig. 9. MPM poles of test board for different pulse strengths.

5. Changing the Location of the Large Capacitor

With capacitor values of 2.2 nF and 1 μ F, the location of the 1- μ F capacitor was changed. The location numbers in Figs. 10 and 11 correspond to the numbered locations of Fig. 2. Fig. 10 shows the time-domain response, while Fig. 11 shows the resulting pole locations for this test.

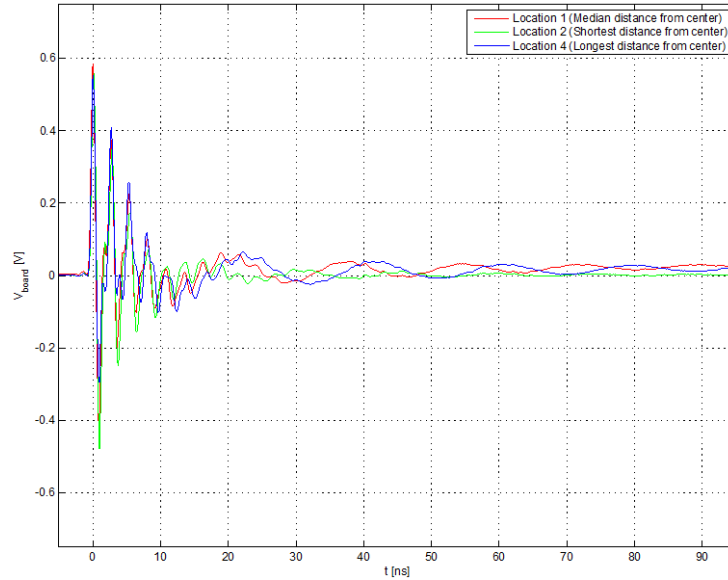


Fig. 10. Time-domain response of test board for different 1- μ F capacitor locations.

Since the spacing of the board planes is approximately 0.060 inches, changing the location of the 1- μ F capacitor should have a small but noticeable effect on the inductance that rings with the 2.2-nF capacitor. The estimated inductances, in order from largest to smallest, are location 4, location 1, and location 2. The estimated pole frequencies, from lowest to highest, should be in the same order. This is confirmed in Fig. 11, where the tick mark spacing is again 5% of the nominal value. While there is roughly 5% variation in damping, there is much more variation in frequency. The frequency of location 2 is approximately 30% higher than that of location 4, and approximately 20% higher than that of location 1.

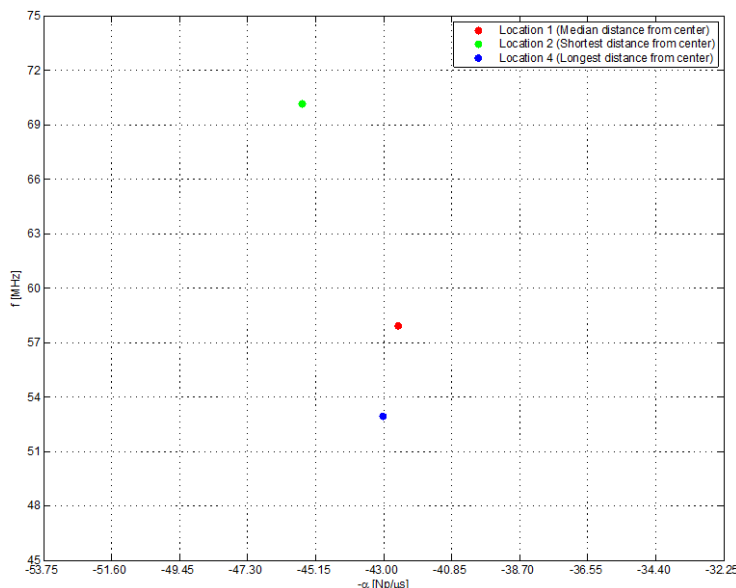


Fig. 11. MPM poles of test board for different 1 μ F capacitor locations.

Using the central capacitance of 2.2 nF and the measured pole frequency for location 1, the ringing inductance calculation is identical to (1), and the estimated inductance is 3.4 nH. With this estimated inductance and the measured damping of 42.54 Np/μs, the ringing resistance can be estimated as,

$$R = 2\alpha L = 2 \cdot (42.54 \text{ Np}/\mu\text{s}) \cdot (3.4 \text{ nH}) \cong 290 \text{ m}\Omega \quad (1)$$

Similarly, the estimated inductance and resistance for location 2 are 2.3 nH and 210 mΩ, respectively, and for location 4, 4.1 nH and 350 mΩ.

6. Changing the Capacitance of the Large Capacitor

Since the main pole of interest is due to the resonance of the 2.2-nF capacitor and the connection inductance of the 1-μF capacitor, changing the value of the 1-μF capacitor should have very little effect on the pole frequency. To verify this, three different large capacitors were mounted in location 4 on the test board. Fig. 12 shows the time-domain response, while Fig. 13 shows the resultant pole locations.

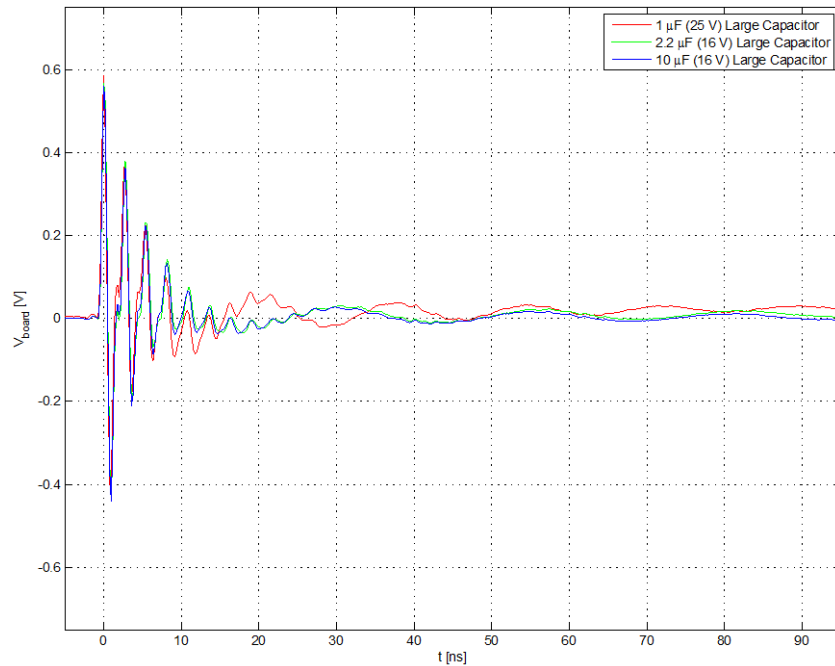


Fig. 12. Time-domain response of test board for different large capacitor values.

It should be noted that the voltage rating of the 1-μF capacitor was 25 V, while the rating of the 2.2-μF and 10-μF capacitors was 16 V. The two capacitors with similar voltage ratings show poles with similar locations. The pole location for the 25-V capacitor is different, suggesting that it may have a lower connection inductance.

The damping of the 25-V, 1 μF capacitor is approximately 18% greater than that of the 16-V rated capacitors, and its ringing frequency is approximately 38% greater than the 16-V capacitors. By substituting the pole frequencies from Fig. 13 into (1), the estimated connection inductance of the 25-V rated capacitor is 3.4 nH, while the 16-V rated capacitors have an estimated connection inductance of 7.3 nH. Applying the damping values from Fig. 13 and (2), the estimated resistance of the 25-V capacitor is 290 mΩ, and the estimated resistance of the 16-V capacitors is 510 mΩ.

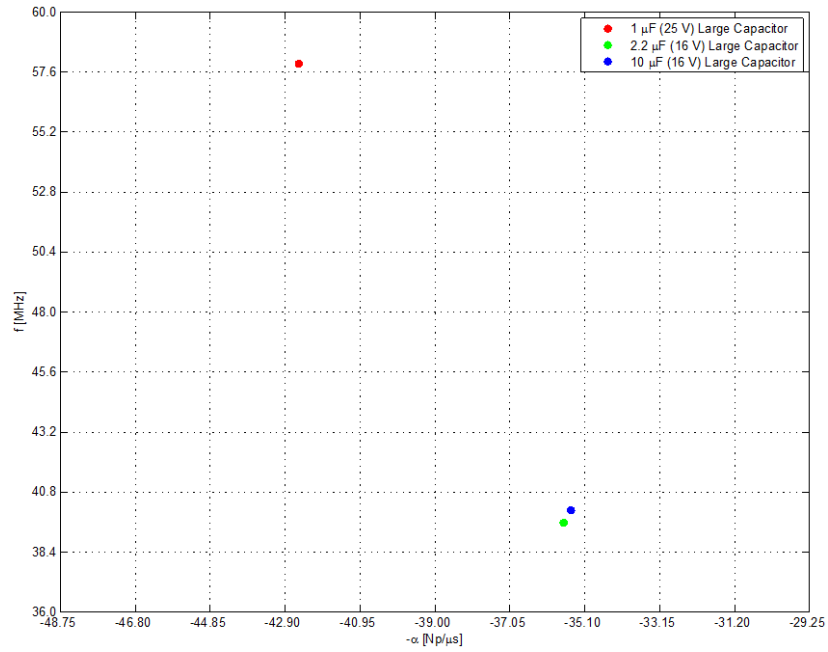


Fig. 13. MPM poles of test board for different large capacitor values.

7. Changing the Capacitance of the Small Capacitor

To ensure that the 2.2-nF capacitor was involved in creating the main pole of interest, its value was changed while the value and location of the 1-μF capacitor in location 4 were held constant.

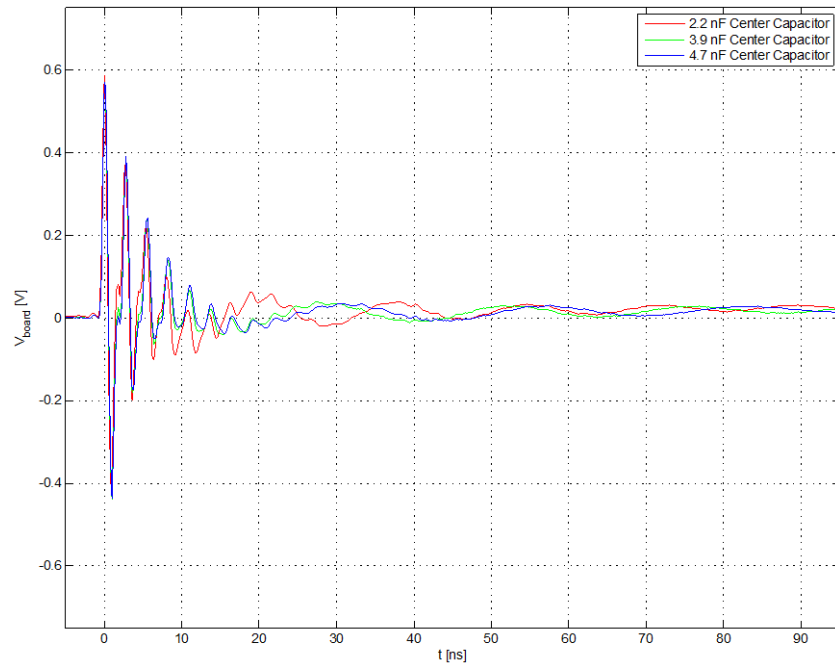


Fig. 14. Time-domain response of test board for different central capacitor values.

Based on the estimated connection inductance of 3 nH and the different central capacitor values, the 2.2-nF capacitor should have a pole at approximately 58 MHz, the 3.9-nF capacitor should have a pole around 43 MHz, and the 4.7-nF capacitor should have a pole at roughly 39 MHz. These were determined by substituting the expected inductance and capacitances into (1). Fig. 15 confirms the expected pole frequencies.

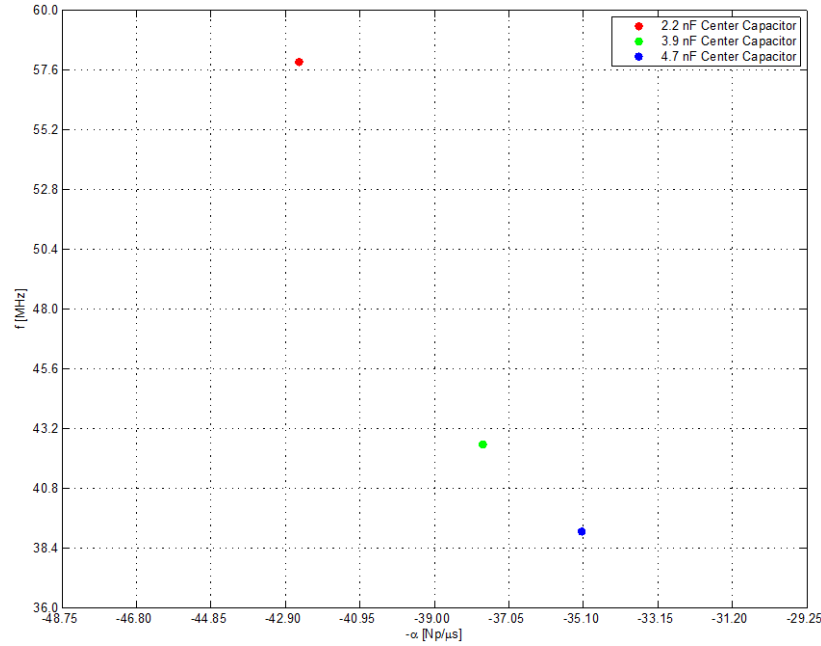


Fig. 15. MPM poles of test board for different central capacitor values.

The frequency of the 2.2-nF capacitor pole is approximately 40% higher than that of the 4.7-nF capacitor, and approximately 33% higher than that of the 3.8-nF capacitor. This again coincides with the expected pole behavior. The damping of the 2.2-nF capacitor is approximately 13% greater than that of the 3.9-nF capacitor, and approximately 19% greater than that of the 4.7-nF capacitor.

Using the pole frequencies with their respective central capacitor values and (1), all three capacitors have a connection inductance of approximately 3.5 nH. With the damping values and (2), the estimated resistance of the 2.2-nF capacitor is 290 mΩ, the estimated resistance of the 3.9-nF capacitor is 270 mΩ, and the estimated resistance of the 4.7-nF capacitor is 250 mΩ.

8. Conclusion

It was found that the main pole of interest in the case of the simple test board was caused by the capacitance of the smaller-valued, centrally located capacitor ringing with the connection inductance of the larger-valued capacitor. It is not known for certain without further experimentation, but the resistance contributing to the damping appears to be a combination of the ESRs of both capacitors, with some resistance also due to the planes. The resistance of the planes will depend on the distance between the two capacitors, so the total resistance may be dominated by one or both ESRs if the distance is sufficiently small. Overall, the measurements presented in this paper correctly identify the expected pole locations. The next step is to evaluate boards with one or more capacitors that have been degraded by exposure to voltage transients. Since this degradation normally manifests itself as a decrease in capacitance or a sharp change in the ESR, it should be possible to detect the presence of a degraded capacitor by observing a shift in its pole location.

References

- [1] J. H. Hayes and T. Hubing, "Monitoring Transistor Degradation in Power Inverters Through Pole Shifts," *IEEE Transactions on Electromagnetic Compatibility*, Accepted for Publication Dec. 2014.