**TECHNICAL REPORT: CVEL-18-072**

**Application of Imbalance Difference Method to the EMC Design of Automotive Wire Harnesses**

Jongtae Ahn and Dr. Todd Hubing

Clemson University

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# Abstract

Common mode currents induced on wiring harnesses often play a key role in the electromagnetic compatibility of automotive components and systems. Designing the electrical balance of the harness to match the electrical balance of the circuit board prevents mode conversion from taking place at the board-cable interface. This paper describes how wire harnesses can be designed to have imbalance factors that match typical circuit board geometries.

# I.    Introduction

Unwanted radiated emissions can present significant challenges to the designers of automotive electronics. A primary source of these radiated emissions is the common-mode (or antenna-mode) current induced on the wire harnesses. Even small cars today can have a thousand meters of wire harnesses, and luxury cars may have more than four times that amount [1]. Wire harness emissions can cause disturbances to numerous HF devices (e.g. FM radio, Bluetooth, GPS and GSM devices)[2]. However, shielded wires or coaxial cables are rarely used in automotive environments due to cost, weight, flexibility and bonding issues. It is important therefore, to address the issue of unintended radiated emissions from wire harnesses without shielding whenever possible.

At the frequencies where radiated emissions are measured, the signals in a wiring harness are propagated as differential-mode currents, while the radiated emissions primarily result from the common-mode currents. The generation of CM currents from differential-mode (DM) signals has been studied extensively. A very powerful method for modeling differential-mode to common-mode conversion was introduced in [3, 4]. This approach is commonly referred to as the Imbalance Difference Theory (IDT). IDT defines the concept of electrical balance in a transmission line (TL) and an imbalance factor (or current division factor) that precisely quantifies this balance [5, 7]. IDT demonstrates that changes in the electrical balance on TLs results in a conversion between DM propagation and CM propagation. The amplitude of the induced voltage driving the CM propagation can be accurately

expressed as the product of the DM voltage and the change in the imbalance factor at any given point along a transmission line. IDT provides great insight into the DM-to-CM conversion mechanism and provides an easy way of modeling this conversion in many practical situations.

In [6], a method for computing the per-unit-length generalized capacitance matrix in a multi-conductor transmission line such as a wire harness was presented. This capacitance matrix can be used to calculate the imbalance factor associated with any given signal propagation mode.

This paper explores the possibility of designing wire harnesses that mimic the imbalance factors that the signals experience as they propagate along circuit board traces. This approach prevents differential-mode signals that propagate from a circuit board to a wiring harness from generating common-mode currents on the harness. Section II explains the calculation of the capacitances in a multi-conductor system using 2D field solvers, then derives the current division factor based on these capacitances. Section III compares the calculated current division factors for various wire bundle cross-sections and discusses the effect of various parameters on the calculation results. Section IV validates the concept presented in the paper using experimental results. Finally, the discussion is summarized in Section V.

## II.   Current Division Factor Calculation

In a wire harness with N wires, we can define a self-capacitance for each wire and a mutual capacitance between each wire pair. The self- and mutual-capacitances per unit length of each wire can be calculated using a 2D electric field solver. For the calculations in this paper, we used a free solver called ATLC2. ATLC2 does not solve for the self- and mutual-capacitances directly, but it can calculate the total capacitance between any two sets of conductors. The generalized capacitance matrix can be expressed as below.

$$\begin{bmatrix} Q_1 \\ Q_2 \\ . \\ . \\ . \\ Q_n \end{bmatrix} = \begin{bmatrix} c_{11} & c_{12} & \cdots & c_{1n} \\ c_{21} & c_{22} & \cdots & c_{2n} \\ \cdots & \cdots & \cdots & \cdots \\ c_{n1} & c_{n2} & \cdots & c_{nn} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ . \\ . \\ . \\ V_n \end{bmatrix} \qquad (1)$$

Coefficients of the form $c_{ii}$ represent the self-capacitance of the $i^{th}$ conductor. Coefficients of the form $c_{ij}$ where $i \neq j$ are referred to as coefficients of induction. These coefficients satisfy the relation $c_{ij}=c_{ji}$. The relation between these coefficients and the mutual capacitance between the $i^{th}$ and $j^{th}$ conductor is $C_{ij}=-c_{ij}$. For a harness with N wires, there are $N^2$ matrix elements, however since $c_{ij}=c_{ji}$, the number of independent variables is $N(N+1)/2$. The number of variables needed to solve a system with N conductors are shown in Table 1.

Table 1. Number of variables needed to solve a system with N conductors

| N | Number of variables |
|---|---|
| 2 | 3 |
| 3 | 6 |
| 4 | 10 |
| 5 | 15 |

To calculate the mutual and self-capacitances using a 2D capacitance solver, a non-zero voltage is assigned to one wire while the other wires are held to zero potential (ground). The 2D solver calculates the charge density induced on the wire with non-zero voltage and uses that to obtain its capacitance per unit length. For example, if the non-zero voltage is applied only to Wire 1, the capacitance per unit length obtained using a 2D solver represents the capacitance per unit length of Wire 1 to all other wires and infinity, which is $C_1 = c_{11} + c_{12} + c_{13} + ... + c_{1n}$. Repeating this calculation for the remaining wires yields N equations in a harness with N wires. Secondly, if the same non-zero voltage is applied to Wire 1 and Wire 2 while the remaining wires are grounded, the calculated capacitance represents the quantity $C_{total} = c_{11} + c_{13} + c_{14} + ... + c_{1n} + c_{22} + c_{23} + c_{24} + ... + c_{2n}$. Note that mutual capacitance $c_{12}$ vanished because conductor 1 and 2 is regarded as connected which means same potential between the two

conductors. Likewise, repeating this calculation for the remaining wires yields by putting non-zero voltage to two conductors among N conductors is $_N C_2 = \dfrac{N \cdot (N-1)}{2}$. Therefore, total number of the equations is $N + \dfrac{N \cdot (N-1)}{2} = \dfrac{N(N+1)}{2}$, which equals the number of variables. To reduce numerical error associated with these calculations, redundant equations are added in order to create an over-determined system. Additional equations that three conductors are the positive non-zero voltage are used to make the system to be over-determined.
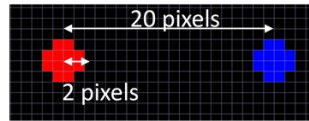


d:5mm, a=0.5mm, ratio(d/2a)=10

| Distance(cm) | Diameter(mm) | Capacitance | | Variance(pF) | | ratio(d/2a) |
| --- | --- | --- | --- | --- | --- | --- |
| | | ATLC2(pF) | Calculated values(pF/m) | | | |
| 0.3 | 0.64 | 12.68 | 12.49 | 0.19 | | 4.69 |
| 0.4 | 0.64 | 11.25 | 11.04 | 0.21 | | 6.25 |
| 0.5 | 0.64 | 10.34 | 10.13 | 0.21 | | 7.81 |
| 10 | 10 | 9.44 | 9.29 | 0.15 | | 10.00 |
| 15 | 10 | 8.29 | 8.18 | 0.11 | | 15.00 |
| 1 | 0.64 | 8.21 | 8.08 | 0.13 | | 15.63 |
| 2 | 0.64 | 6.80 | 6.73 | 0.07 | | 31.25 |
| 15 | 4 | 6.51 | 6.44 | 0.07 | | 37.50 |
| 3 | 0.64 | 6.19 | 6.13 | 0.06 | | 46.88 |
| 15 | 3 | 6.10 | 6.04 | 0.06 | | 50.00 |
| 4 | 0.64 | 5.81 | 5.76 | 0.05 | | 62.50 |
| 15 | 2 | 5.59 | 5.55 | 0.04 | | 75.00 |
| 15 | 1 | 4.88 | 4.88 | 0.00 | | 150.00 |
| 10 | 0.64 | 4.84 | 4.84 | 0.00 | | 156.25 |
| 20 | 1 | 4.62 | 4.64 | 0.02 | | 200.00 |
| 15 | 0.64 | 4.48 | 4.52 | 0.04 | | 234.38 |
| 30 | 1 | 4.26 | 4.35 | 0.09 | | 300.00 |
| 60 | 2 | 4.26 | 4.35 | 0.09 | | 300.00 |
| 50 | 1 | 3.77 | 4.03 | 0.26 | | 500.00 |
| 70 | 1 | 3.24 | 3.84 | 0.60 | | 700.00 |

Fig. 2. Validation of ATLC2 capacitance calculation.

Fig. 2 shows ATLC2 calculations for the capacitance of a twin-wire pair using ATLC2 and an analytical calculation. ATLC2 uses screen pixels to define the cross-section geometry. For these calculations, the number of conductor pixels is twelve. One pixel represents a square that is 0.25 mm on a side. The mutual capacitance between the wires can be calculated analytically as,

$$C = \frac{\pi \varepsilon}{\cosh^{-1}(d/2a)} \; . \tag{2}$$

The 'd' represents center-to-center distance between the conductors and the 'a' represents the conductor

radius. The results in Fig. 2 indicate that ATLC2 calculates a capacitance within 2% of the analytical

value. In ATLC2, the voltage on the wire is represented by the color. The red color represents a positive

voltage, blue is negative, and green is ground or zero potential. The general process to calculate the self-

capacitance using ATLC2 is:

1) Define the geometry of the test environment.

2) Draw the conductors and any dielectric insulators.

3) Assign a positive voltage or a zero potential to each conductor.

4) Run the program to calculate the total capacitance.

5) Repeat this process with different voltage assignments until you have enough data to build a

capacitance matrix to derive self-capacitance of each conductor.
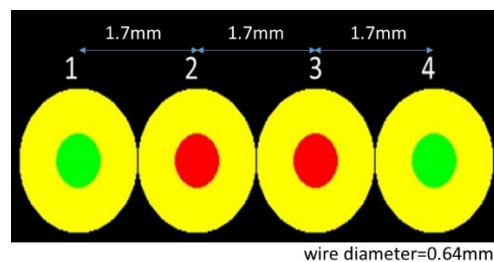


Fig. 3. Ribbon cable consisting of 4 wires.

Fig. 3 shows a ribbon cable that has 4 wires with a polystyrene insulator ($\epsilon_r$=2.5). The inner two

wires have a positive voltage represented by their red color. The outer two (green) wires represent the

conductors used for return current. Note that in this configuration (and the remaining configurations to

be examined in this paper) the "differential mode" currents flow in the same direction on a pair of

conductors and return on other conductors (normally labeled "ground"). This represents currents that are

normally labeled as the common-mode components of a differential signal, but do not result in significant radiated emissions because they return on a nearby "ground" conductor. The common-mode currents that we are concerned with in this paper are the currents induced that flow in the same direction on all of the conductors. These currents are sometimes referred to as "antenna mode" currents [5].

The current division factor (CDF) for the configuration in Fig. 3 can be calculated using the self-capacitance terms (i.e. capacitances to infinity) as below,

$$CDF = \frac{c_{22} + c_{33}}{c_{11} + c_{22} + c_{33} + c_{44}}. \tag{3}$$

For calculating the self and mutual capacitances using ATLC2, we need at least 10 equations to complete the capacitance matrix.

| Geometry and Charges | Results |
|---|---|
|  | Conductor 1 only $c_{11} + c_{12} + c_{13} + c_{14} = 34.237$ (1) |
|  | Conductor 2 only $c_{12} + c_{22} + c_{23} + c_{24} = 52.459$ (2) |
|  | Conductor 3 only $c_{13} + c_{23} + c_{33} + c_{34} = 52.460$ (3) |
|  | Conductor 4 only $c_{14} + c_{24} + c_{34} + c_{44} = 34.238$ (4) |
|  | Conductor 1&2 $(c_{11} + c_{22}) + c_{13} + c_{14} + c_{23} + c_{24} = 37.016$ (5) |
|  | Conductor 1,2,&3 $(c_{11} + c_{22} + c_{33}) + c_{14} + c_{24} + c_{34} = 36.684$ (6) |
|  | Conductor 1&3 $(c_{11} + c_{33}) + c_{12} + c_{23} + c_{14} + c_{34} = 79.628$ (7) |
|  | Conductor 1&4 $(c_{11} + c_{44}) + c_{12} + c_{13} + c_{34} + c_{24} = 61.945$ (8) |
|  | Conductor 2&4 $(c_{22} + c_{44}) + c_{12} + c_{23} + c_{14} + c_{34} = 79.629$ (9) |
|  | Conductor 2,3,&4 $(c_{22} + c_{33} + c_{44}) + c_{12} + c_{13} + c_{14} = 36.686$ (10) |
|  | Conductor 2&3 $(c_{22} + c_{33}) + c_{12} + c_{13} + c_{24} + c_{24} = 58.895$ (11) |
|  | Conductor 3&4 $(c_{33} + c_{44}) + c_{13} + c_{23} + c_{14} + c_{24} = 37.018$ (12) |
|  | Conductor 1,3,&4 $(c_{11} + c_{33} + c_{44}) + c_{12} + c_{23} + c_{24} = 57.608$ (13) |
|  | Conductor 1,2,&4 $(c_{11} + c_{22} + c_{44}) + c_{13} + c_{23} + c_{34} = 57.607$ (14) |

Fig. 4. Capacitance calculation results using ATLC2.

Fig. 4 shows the calculated capacitances between various sets of conductors. N=4, so there are 4(4+1)/2=10 independent coefficients to be determined. Four redundant simulations were performed to reduce the simulation error.

$$
\begin{bmatrix}
34.237 \\ 52.459 \\ 52.460 \\ 34.238 \\ 37.016 \\ 36.684 \\ 79.628 \\ 61.945 \\ 79.629 \\ 36.686 \\ 58.895 \\ 37.018 \\ 57.608 \\ 57.607
\end{bmatrix}
=
\begin{bmatrix}
1&1&1&1&0&0&0&0&0&0 \\
1&0&0&0&1&0&0&1&1&0 \\
0&0&1&0&0&1&0&1&1&0 \\
0&0&0&1&0&0&1&0&1&1 \\
1&0&1&1&1&1&1&0&0&0 \\
1&0&0&1&1&0&1&1&1&1 \\
1&1&0&1&0&1&0&1&1&0 \\
1&1&1&0&0&0&1&0&1&1 \\
0&1&0&1&1&1&0&0&1&1 \\
0&1&1&1&1&1&0&1&0&1 \\
0&1&1&0&1&0&1&1&1&0 \\
0&0&1&1&0&1&1&1&0&1 \\
1&1&0&0&0&1&1&1&0&1 \\
1&0&1&0&1&1&0&0&1&1
\end{bmatrix}
\begin{bmatrix}
c_{11} \\ c_{12} \\ c_{13} \\ c_{14} \\ c_{22} \\ c_{23} \\ c_{24} \\ c_{33} \\ c_{34} \\ c_{44}
\end{bmatrix}
\Rightarrow
\begin{bmatrix}
c_{11} \\ c_{12} \\ c_{13} \\ c_{14} \\ c_{22} \\ c_{23} \\ c_{24} \\ c_{33} \\ c_{34} \\ c_{44}
\end{bmatrix}
=
\begin{bmatrix}
1&1&1&1&0&0&0&0&0&0 \\
1&0&0&0&1&0&0&1&1&0 \\
0&0&1&0&0&1&0&1&1&0 \\
0&0&0&1&0&0&1&0&1&1 \\
1&0&1&1&1&1&1&0&0&0 \\
1&0&0&1&1&0&1&1&1&1 \\
1&1&0&1&0&1&0&1&1&0 \\
1&1&1&0&0&0&1&0&1&1 \\
0&1&0&1&1&1&0&0&1&1 \\
0&1&1&1&1&1&0&1&0&1 \\
0&1&1&0&1&0&1&1&1&0 \\
0&0&1&1&0&1&1&1&0&1 \\
1&1&0&0&0&1&1&1&0&1 \\
1&0&1&0&1&1&0&0&1&1
\end{bmatrix}^{-1}
\begin{bmatrix}
34.237 \\ 52.459 \\ 52.460 \\ 34.238 \\ 37.016 \\ 36.684 \\ 79.628 \\ 61.945 \\ 79.629 \\ 36.686 \\ 58.895 \\ 37.018 \\ 57.608 \\ 57.607
\end{bmatrix}
$$

Fig. 5. Capacitance calculation matrix with the simulation results

Fig. 5 shows the capacitance matrix obtained from the simulation results. We have 14 equations and 10 variables so the matrix is not rectangular. MATLAB was used to solve the over-determined system using the 'mldivide' ('\') function, which provides a least-squares solution minimizing the length of the vector $AX - B$. The calculated self-capacitances in this example are,

$$c_{11} = 2.749, c_{22} = 1.224, c_{33} = 1.224, c_{44} = 2.749, \tag{4}$$

and the current division factor (CDF) is,

$$CDF = \frac{c_{22} + c_{33}}{c_{11} + c_{22} + c_{33} + c_{44}} = 0.3081. \tag{5}$$

If the wire insulation is changed to Teflon ($\epsilon_r$=2.02), the calculated self-capacitance of each wire and the current division factor become,

$$c_{11} = 2.6039, c_{22} = 1.2053, c_{33} = 1.2058, c_{44} = 2.6049 \tag{6}$$

and,

$$CDF = \frac{c_{22} + c_{33}}{c_{11} + c_{22} + c_{33} + c_{44}} = 0.3164 . \tag{7}$$

The transmission line is more balanced when the relative permittivity of the insulation is lower. Higher permittivity dielectrics capture more of the electric field from the outer conductors making their self-capacitances closer to the self-capacitances of the inner conductors.
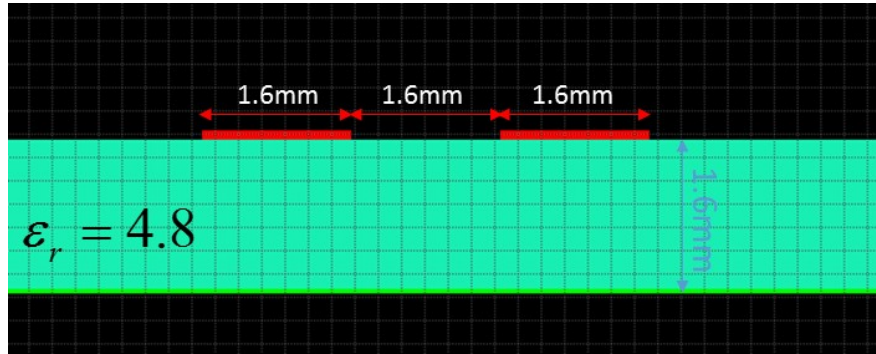


Fig. 6. PCB board traces over a return plane.

Fig. 6 shows an example of a printed circuit board (PCB) cross section. In this example current flows out on a pair of traces and returns on a solid plane 1.6 mm below the traces. The traces are separated by 1.6 mm. The trace width is 1.6 mm and the insulation material is FR4 ($\epsilon_r$=4.8). The traces are conductors 1 and 2. The return plane is conductor 3. The calculated self-capacitances and current division factor are,

$$c_{11}=0.2940, \, c_{22}=0.2940, \, c_{33}=7.1220 \tag{8}$$

and

$$CDF = \frac{c_{11} + c_{22}}{c_{11} + c_{22} + c_{33}} = 0.0763 \tag{9}$$

If the return plane is moved farther from traces, the current division factor increases, which means the circuit is more balanced. For example, the calculated current division factor increases to 0.0844 when the return plane is 2.6 mm away from traces.

# III.  The Wire Harness Design for Twisted Pair and Ground Wires

Based on the calculation of the self-capacitances in a multi-conductor wire harness, the current division factor can be optimized to match the current division factor of the components on each end to eliminate differential-mode to common-mode current conversion.



| # | parameters (mm) | | | CDF |
|---|---|---|---|---|
| | Spacing | Width | Distance | |
| 1) | 1.6 | 1.6 | 1.6 | 0.0763 |
| 2) | 1.6 | 1.6 | 0.8 | 0.0771 |
| 3) | 1.6 | 1.6 | 0.4 | 0.0919 |
| 4) | 3.2 | 1.6 | 1.6 | 0.0855 |
| 5) | 3.2 | 0.8 | 1.6 | 0.0642 |
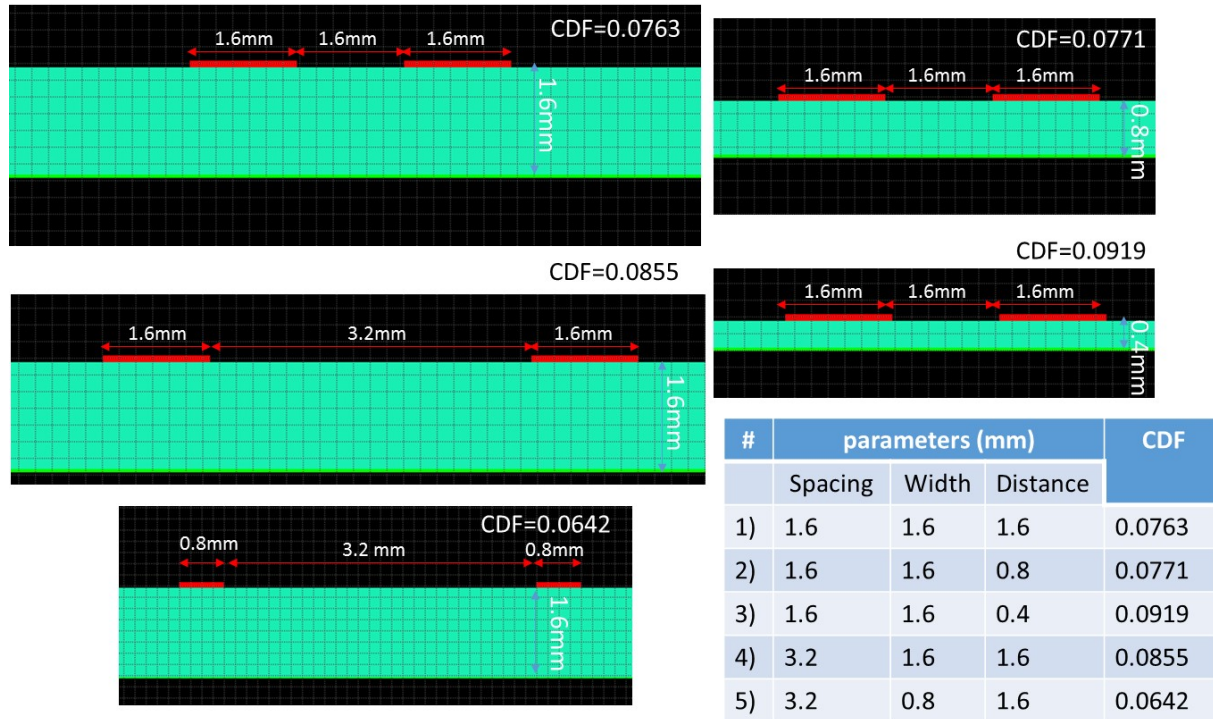
Fig. 7. PCB configurations and corresponding current division factors.

Fig. 7 shows the current division factors calculated for several PCB geometries. All of the geometries are fairly unbalanced with CDFs ranging from 0.0642 to 0.0919. The different configurations demonstrate that parameters of the PCB geometry can be adjusted to influence the current division factor. Structures with wider return planes are more unbalanced. (A theoretical circuit board with an infinitely wide return plane would be perfectly unbalanced with a CDF of 0.0) When the trace spacing is greater, the circuit is more balanced. When the trace width becomes smaller, the circuit becomes more unbalanced.
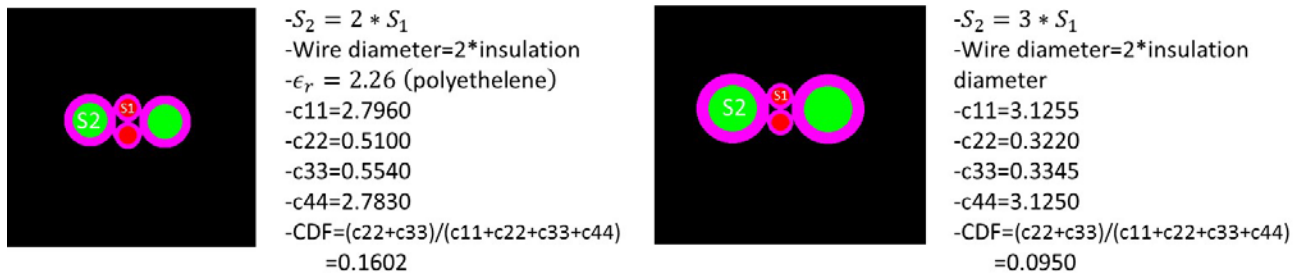
Fig. 8. Wire bundle configurations and corresponding current division factors.

Fig. 8 shows two wire bundle configurations and their corresponding current division factors. The one on the right has a current division factor similar to that of typical PCB configurations. The cross-sectional area of the return path wires is greater than that of the signal wires. The return wires are located next to the signal wires to capture as much of the electric field from the signal wires as possible and reduce the CDF of the wire bundle.
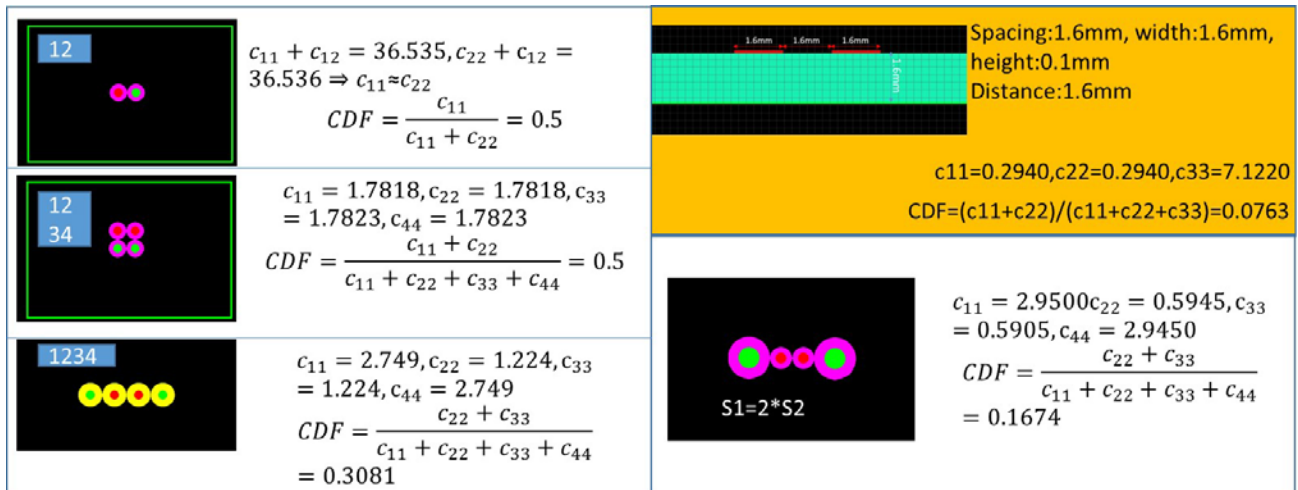


Fig. 9. CDFs of four-wire bundles compared to the PCB configuration.

Fig. 9. Shows the calculated current division factors for various wire harness geometries. As expected, the symmetric geometries are perfectly balanced (CDF = 0.5). The current division factor is reduced if the return wires are thicker than the signal wires. The ribbon cable is more unbalanced than the wire bundle even though the return wires are thicker due to the lack of close proximity between the signal and return conductors.

$c_{11} = 22.7300, c_{22} = 22.7300, c_{33} = 0, c_{44} = 22.7305, c_{55} = 22.7305$

$$CDF = \frac{c_{11} + c_{33}}{c_{11} + c_{22} + c_{33} + c_{44} + c_{55}} = 0.2500$$

Spacing:1.6mm, width:1.6mm, height:0.1mm
Distance:1.6mm

c11=0.2940,c22=0.2940,c33=7.1220
CDF=(c11+c22)/(c11+c22+c33)=0.0763

$c_{11} = 1.3823, c_{22} = 1.6818, c_{33} = 0.5496, c_{44} = 1.0488, c_{55} = 2.1106$

$$CDF = \frac{c_{33} + c_{44}}{c_{11} + c_{22} + c_{33} + c_{44}} = 0.2360$$

S1=2*S2

$c_{11} = 2.3827, c_{22} = 1.6437, c_{33} = 0.0471, c_{44} = 0.2537, c_{55} = 2.1826$

$$CDF = \frac{c_{33} + c_{44}}{c_{11} + c_{22} + c_{33} + c_{44} + c_{55}} = 0.0462$$
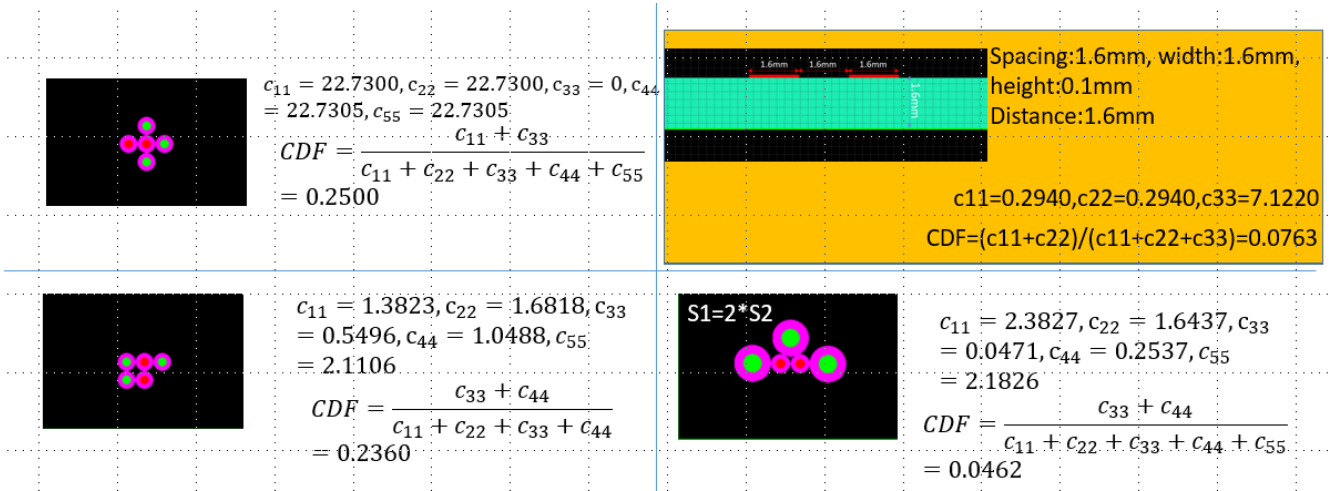
Fig. 10. The other types of wire bundle with five wires and comparison with the PCB configuration.

Fig. 10 shows the calculated current division factors for five additional wire bundles. These wire bundles are more unbalanced than the previous four wire bundles. Nevertheless, the imbalance of the wire harnesses is not enough to match the current division factor for the PCB unless the return wires are much thicker than the signal wires. Circuit board and wire harness parameters that affect the CDF are listed in Table 2.

Table 2. Circuit board and wire harness parameters that affect the CDF

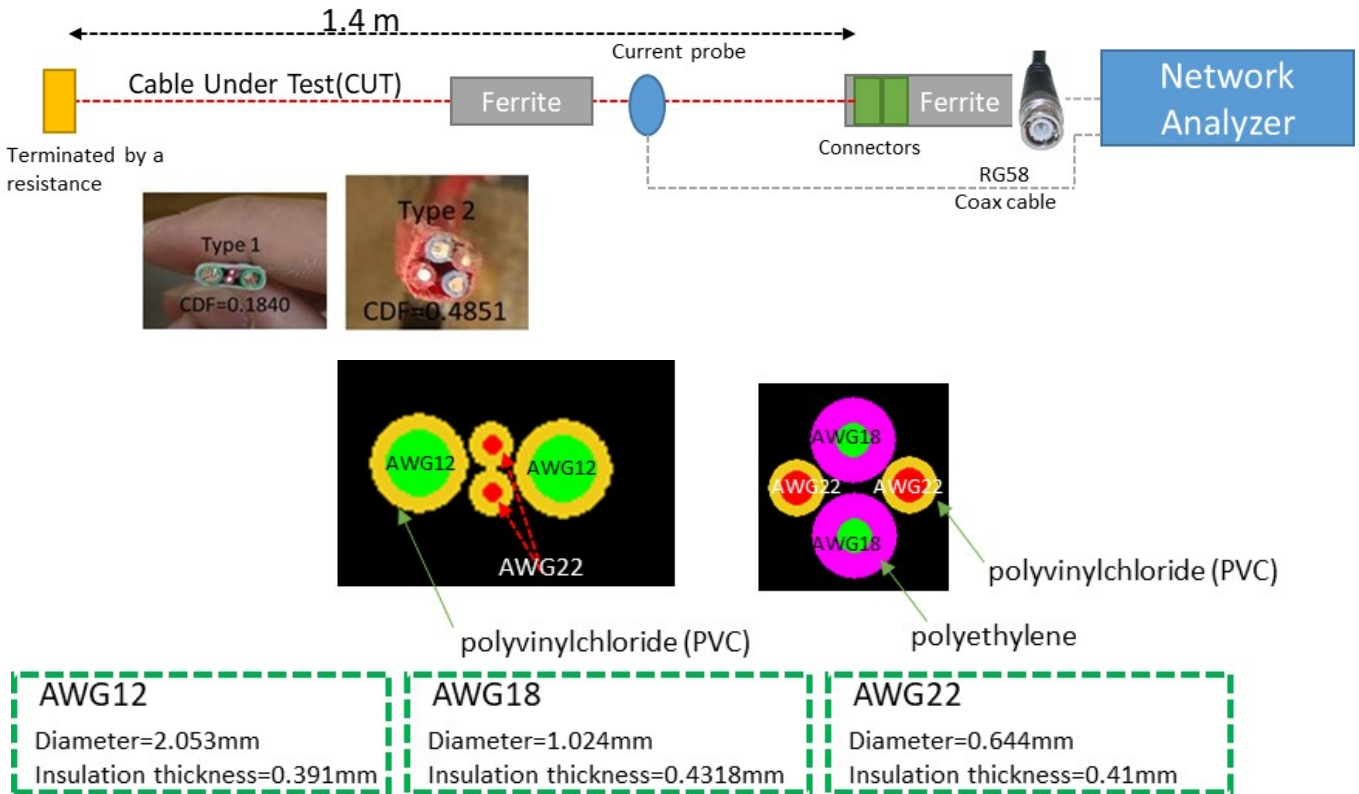| PCB board | Wire harness |
|---|---|
| Material of the substrate | Insulation material of wires |
| Separation width between traces | Wire geometry |
| Distance between traces and ground plane | Wire thickness |
| Trace width | Number of return conductors |

# IV.    Measurement Results



Fig. 12. Test set-up and cross sections of wire harnesses

Generally speaking, signals propagating on circuit board traces over a current return plane have very low CDFs (i.e. are very unbalanced). Therefore, to reduce the common-mode current induced on a wire harness attached to a circuit board, it is desirable for the harness to have a CDF that is as low as possible. To illustrate this, the test set-up in Fig. 12 was used to measure the common-mode current induced at the interface between a coaxial cable (CDF = 0.0) and two different wire harnesses. The one on the left is made with AWG12 and AWG22 wires (CDF=0.1840). The one on the right is made with AWG12 and AWG22 wires (CDF=0.4851). The current division factors for the two harnesses were calculated using the method described in Section II.

For this measurement, the network analyzer sends a signal through a coaxial cable (CDF=0.0), which connects to one the wire harness being evaluated. A current probe measures the common-mode current induced on the wire harness due to the change in the imbalance that occurs at the coax-to-wire-harness

interface. The wire harness termination is matched to the characteristic impedance of the harnesses being evaluated (68 ohms in both cases) and ferrites are places on the cables to dampen sharp resonances.

The change in the CDF at the interface between the coaxial cable and wire harness being evaluated equals the current division factor of the wire harness because the current division factor of the coaxial cable is zero. The harness with the lower CDF is expected to generate less common-mode current, because it is better matched to the coax. The difference in the common-mode current induced by the two harnesses should be equal to the difference in their CDFs. Expressed in decibels, this difference is,

$$\Delta h_1 = 0.1840, \Delta h_2 = 0.4851 \tag{10}$$

$$20\log(\Delta h) = 20\log(\frac{\Delta h_2}{\Delta h_1}) = 7.88\,\text{dB} \tag{11}$$
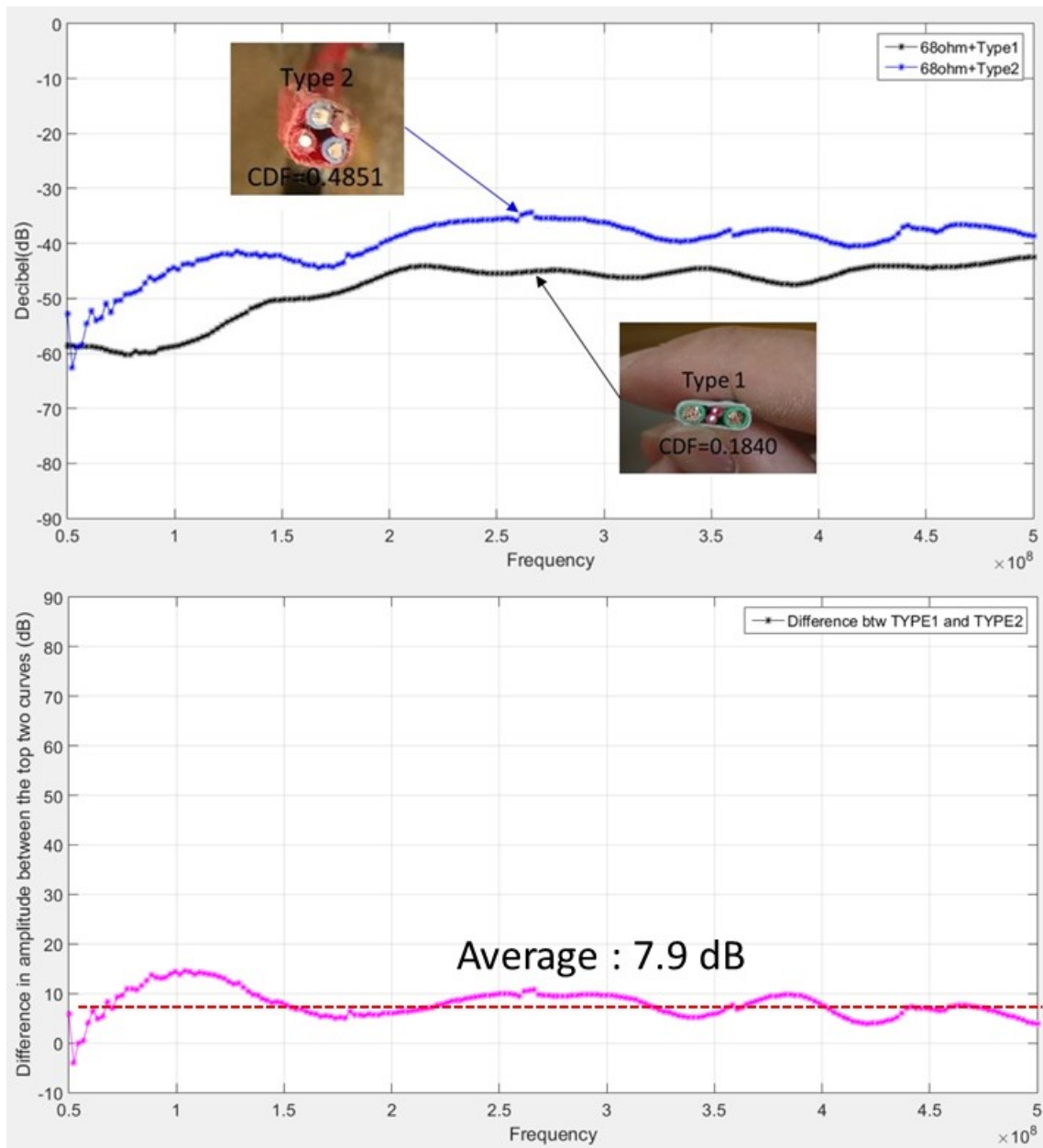
Fig. 13. The results of antenna mode currents in two wire harnesses

The two curves in the upper plot in Fig. 13 show the measured common-mode currents obtained with the two wire harnesses relative to the signal input ($S_{21}$ on the network analyzer) as a function of frequency. The lower plot shows the difference between the two curves in the upper plot. As expected, the ratio of antenna mode currents averages about 7.9 dB. There are some fluctuations due to slightly different harness resonances, but the results show that the common-mode currents are proportional to the change in the current division factors.

# V. Conclusion

Matching the imbalance of a wire harness to the imbalance of its source and termination reduces the amount of common-mode current induced on the harness. A method for determining the imbalance (CDF) of wire harnesses using a simple electric-field solver has been presented. Wire harnesses with a pair of signal wires surrounded by thicker "ground" or return wires were shown to be capable of having CDFs comparable to typical printed circuit board configurations with a pair of signal traces over a return plane.

Measurements of two harness configurations demonstrated that common-mode currents are proportional to the changes in the current division factor. It is worth noting that the "ground" wires in these simulations and measurements do not have to literally connect to ground. For the purposes of determining the CDF, any wires in the harness that can freely carry current are "ground" wires. This includes wires that may be carrying currents associated with other signals in the harness.

# References

[1]    D. Crolla, *Encyclopedia of Automotive Engineering*. John Wiley & Sons, 2015.

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