Quantifying Decoupling Capacitor Location

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Abstract: Decoupling capacitor location in DC power bus design is a critical design choice for which proven guidelines are not well established. The mutual inductance between two closely spaced vias can have a great impact on the coupling between an IC and a decoupling capacitor. This coupling is a function of the spacing between the IC and capacitor, and spacing between power and ground layers. The impact of the mutual inductance on decoupling, i.e., local versus global decoupling, was studied, using a circuit extraction approach based on a mixed-potential integral equation. Modeling indicates that local decoupling has benefits over global decoupling for certain ranges of IC/capacitor spacing and power layer thickness. Design curves for evaluating local decoupling benefits were generated, which can be used to guide surface mount technology (SMT) decoupling capacitor placement.

I. Introduction

Decoupling capacitor location in printed circuit board DC power bus design is a critical design choice for which proven guidelines are not well established. Most schools of thought advocate some form of global bulk decoupling. A traditional view also advises the use of decoupling capacitors placed very close to individual integrated circuits [1] [2] [3]. The rationale for this approach may be rooted in the inductance of the interconnects for capacitors and power routing on traces as opposed to planes. A more recently published study of decoupling capacitors and printed circuit boards as ensembles concluded that for printed circuit boards with both power and ground planes, all decoupling capacitors are shared in the frequency range in which they are effective; hence, the location of the decoupling capacitor on the board is unimportant [4]. This study considered multi-layer boards with closely spaced layers and its conclusions may have been extended beyond the region of validity of the study. This paper examines the magnetic field coupling between vias in close proximity, and the associated ability of decoupling capacitors near an integrated circuit (IC) to transfer charge to the IC more effectively than decoupling capacitors farther from the IC.

A decoupling capacitor spaced close to an IC can be tightly coupled to the power pins of an IC as a result of mutual inductance between the vias of the IC and decoupling capacitor [5]. This mutual inductance results from magnetic flux due to currents on these vias sharing a common area, as shown in Figure 1. When there is a current draw from the active device, the decoupling capacitor can provide charge, acting as a local source. These currents, flowing through vias between power and ground layers, generate magnetic flux between the layers. There is a common area of magnetic flux linkage from one of the vias to the edge of the board. This mutual flux determines the mutual inductance between two vias and the effectiveness of a decoupling capacitor closely spaced to an IC. The mutual inductance is a function of the IC/decoupling capacitor spacing, spacing of the power and ground layers in the layer stackup, and the proximity of the IC/decoupling capacitor pair to the PCB edge.

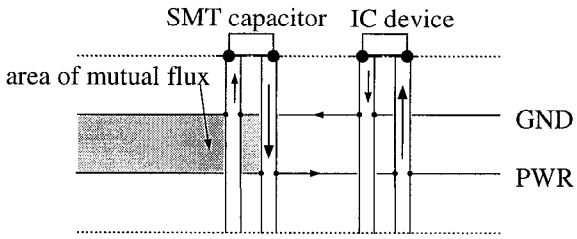

Figure 1: Vias associated with a decoupling capacitor near an IC produce a region of shared magnetic flux and a mutual inductance.

Measurements are presented herein to demonstrate the mutual inductive coupling. The mutual inductance was studied using a lumped circuit model, as well as a full-wave power bus model. Design curves for SMT decoupling capacitor placement in a high-speed digital design were generated based on the modeled results.

II. Experimental Results

Two Port $|S_{21}|$ measurements for a functioning high-speed design show that coupling between two widely spaced vias differ significantly from that between two closely spaced vias. $|S_{21}|$ is related to $|Z_{21}|$ for a power bus on a multi-layer PCB by adding approximately 28 dB [6]. Then, $|Z_{21}|$ simply relates the voltage at Port 2 that results from a current at Port 1. The lower $|S_{21}|$, the smaller the noise voltage that can be induced at Port 2 from the noise current at Port 1. Figure 2 (a) and (b) show two cases with the two test ports either widely or closely

spaced. In Figure 2(a), spacing between two test ports was larger than 30 cm, while in Figure 2(b), the two test ports were located 5 mm apart. The board was fully populated. At low frequencies, the $|S_{21}|$ is solely determined by bulk capacitors on the board, and the total value of the SMT capacitors is normally too small to affect the response. When the frequency reaches the point where the lead inductance associated with the bulk capacitors dominates their impedance, the SMT decoupling capacitors begin to play an important role. They are effective until the parasitic inductance associated with the SMT capacitor interconnects dominates their impedance as frequency increases. The impedance of the board is then dominated by the inter-plane capacitance and the board distributed behavior. As shown in Figure 2(a), an increase of $|S_{21}|$ occurred in a frequency range after the total value of SMT decoupling was reduced by removing SMT capacitors. This frequency range is the SMT effective frequency band. However, when two vias were closely spaced, the phenomenon was quite different. As shown in Figure 2(b), no obvious SMT effective frequency band is observed. The measured $|S_{21}|$ barely changed with the removal of SMT decoupling capacitors, and, further, the coupling between the input and output port increased at a rate of 20 dB/decade at frequencies from approximately 15 to 1500 MHz. This phenomenon can be explained by the mutual inductance between the two vias associated with two corresponding test ports, embedded in the power layer. When the spacing between them is sufficiently small, this mutual inductance becomes the dominant coupling mechanism between the two ports. Hence, the $|S_{21}|$ in Figure 2(b) was mainly determined by the inductive coupling of the two test ports, i.e., magnitude increased at the rate of 20 dB/decade, and the removal of SMT capacitors had little effect. If, instead of two test ports, an IC chip and a decoupling capacitor are located closely enough, in terms of current draw from the IC, it can be dominated by the current drawn from the decoupling capacitor that is placed near the IC.

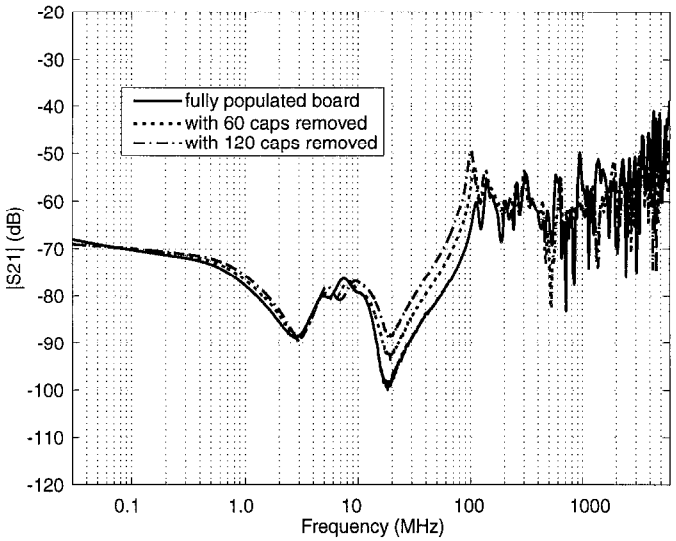

Figure 2 (a): $|S_{21}|$ measurements for two widely spaced test ports in a functioning high-speed digital design.

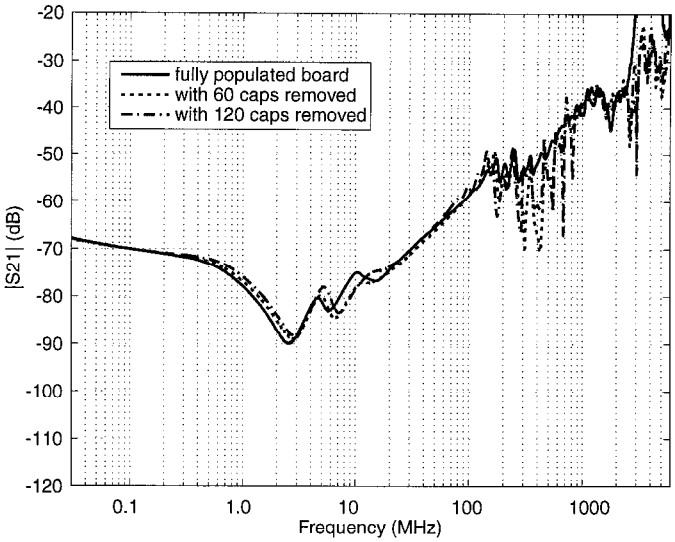

Figure 2 (b): $|S_{21}|$ measurements for two closely spaced test ports in a functioning high-speed digital design.

III. Lumped Circuit Model

The $|S_{21}|$ measurements on the functioning high-speed board demonstrate the existence of mutual inductance between two closely spaced vias. A lumped circuit model for the input impedance of a power bus structure can be constructed as in Figure 3, where L_{probe} is the test port inductance, C_p is the inter-plane capacitance, C_{b1}, ..., C_{bm} are bulk capacitors and L_{b1}, ..., L_{bm} are their corresponding lead inductances, C_{d1}, ..., C_{dn} are SMT capacitors and L_{d1}, ..., L_{dn} are the parasitic inductances associated with their interconnects. There will also be a mutual inductance between two Ls if the corresponding two vias are located closely enough. This model is valid below distributed board resonances [6].

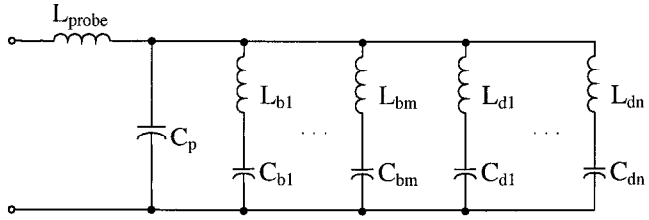

Figure 3: Lumped circuit model for the input impedance of a power bus structure below distributed resonances.

An experiment was designed to investigate the mutual inductance using the lumped circuit model. As shown in Figure 4(a), the experimental geometry was a two-layer board with two solid layers representing power and ground planes, respectively. A shorting post simulated a via. The input impedance was measured looking into an SMA test probe using an impedance analyzer. The location of the shorting post was fixed while the test probe was changed from Location 1 to Location 4 so that the spacing between the two vias, i.e., the shorting post and the test probe, was varied.

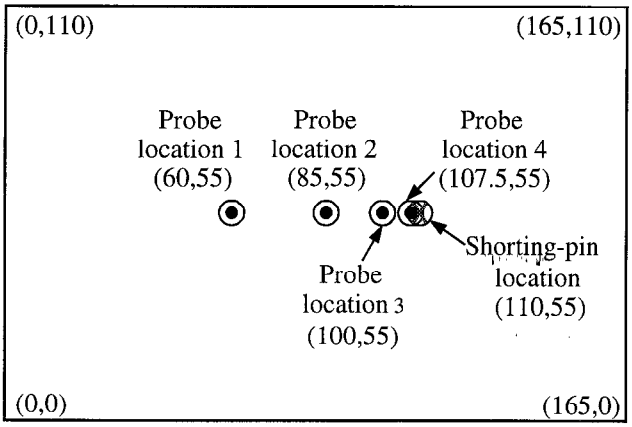

Figure 4(a): Locations of the test probe and the shorting post on the test PCB.

The lumped circuit model for this geometry was simplified as shown in Figure 4(b). The first pole and zero frequencies are given by

$$f_{pole} = \frac{1}{2\pi\sqrt{L_{short} C_p}}, \quad (1)$$

$$f_{zero} = \frac{1}{2\pi\sqrt{\frac{L_{short} L_{probe} - M^2}{L_{short} + L_{probe} - 2M} C_p}}. \quad (2)$$

From (1) and (2), a change of the mutual inductance will only affect the first zero frequency, and the pole frequency will be unchanged. The more closely spaced two vias are, the larger the mutual inductance, thus the lower the zero frequency. Further, the low frequency impedance is mainly determined by L_{short}, L_{probe}, and their mutual inductance M as

$$Z_{in} \approx j\omega(L_{short} + L_{probe} - 2M). \quad (3)$$

Hence, the low frequency magnitude decreases as the mutual inductance increases.

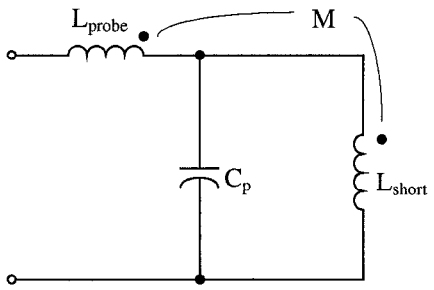

Figure 4(b): Simplified lumped circuit model for the power bus structure shown in 4(a).

Figure 5 shows the measured input impedance results for a test board with layer thickness of 60 mils. The lumped circuit model explained the behavior, including the low-frequency magnitude, the first pole and zero frequencies. Equations (1), (2), and (3) also provide a means of extracting the circuit element values, L_{short}, L_{probe}, and M, from measurements, provided C_p is measured or calculated using a simple parallel-plate capacitor model. Extracted circuit element values for the 60 mil test board are listed in Table 1. The mutual inductance can then be quantified for various configurations with different via spacing versus layer thickness.

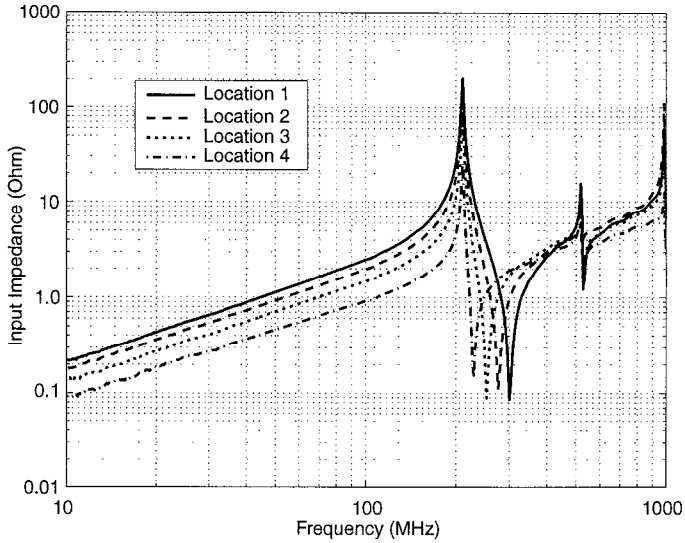

Figure 5: Measured input impedance for the power bus structure shown in 4(a).

Table 1: Circuit element values extracted from measurements for a 60 mil board shown in Figure 4(a).

Spacing between the probe and the shorting post	L_{probe} (nH)	L_{short} (nH)	M (nH)	Coupling coefficient K
2.5 mm	1.8	1.59	0.997	0.5893
10 mm	1.8	1.59	0.522	0.3086
25 mm	1.8	1.59	0.162	0.0956
50 mm	1.8	1.59	0	0

IV. Distributed Power Bus Modeling and Design Curves

Mutual inductive coupling between an IC chip and a decoupling capacitor closely spaced to it can have a profound impact on high-frequency decoupling behavior, which cannot be addressed by the lumped circuit model. A full-wave modeling approach, denoted CEMPIE, for a Circuit Extraction approach based on a Mixed-Potential Integral Equation formulation, has been developed [7] [8]. This approach formulates the power bus design from first principles with a mixed-potential integral equation, and then extracts a SPICE compatible circuit model that is valid to high frequencies. Other well-developed SPICE models, such as sources, loads, and transmission lines, etc., can be incorporated into the extracted circuit model, and various kinds of simulations can

then be performed with SPICE. Both the planar conductors and vertical discontinuities, such as vias and test ports, are formulated from the first principles; hence, decoupling problems, including mutual inductive coupling between closely spaced vias, can be addressed. Comparisons of measured and modeled results for various power bus structures demonstrate the modeling approach [9] [10].

CEMPIE was then used to evaluate the effectiveness of a closely spaced decoupling capacitor. Three simple cases, a bare board, a remotely located decoupling capacitor (Figure 6(a)), and a closely spaced decoupling capacitor (Figure 6(b)), were studied using the modeling approach. The $|Z_{21}|$ between two ports was investigated, since it directly gives the noise voltage at Port 2 when current at Port 1 is injected. Figure 6(c) shows the modeled results. The closely spaced decoupling capacitor provided more than a 10 dB decrease in $|Z_{21}|$ than the remotely located decoupling capacitor up to 1.5 GHz. This benefit resulted from the mutual inductance between the SMT capacitor and Port 1. Also, except near the first pole, the closely spaced decoupling had a lower $|Z_{21}|$ than the bare board up to several GHz. This means that the mutual inductance also enabled the decoupling capacitor to be effective even far beyond the series resonance with its interconnect. The remotely spaced capacitor was only effective up to approximately 300 MHz as shown in Figure 6(c). So, for certain criterion, placing an SMT capacitor as closely as possible to an active device can be benificial.

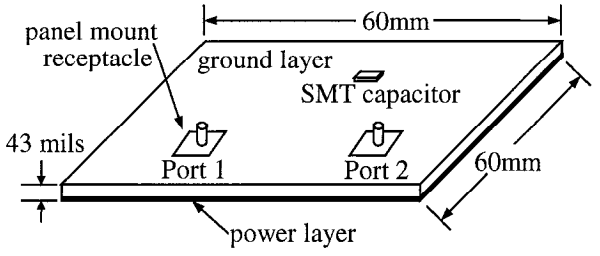

Figure 6(a): The modeled structure for global decoupling.

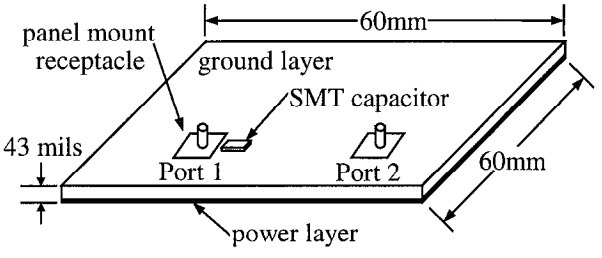

Figure 6(b): The modeled structure for local decoupling.

Decoupling capacitors located sufficiently closely to an IC chip to have a significant mutual inductive coupling effect with the IC are denoted *local decoupling capacitors* with regard to the IC. They can effectively supply charge for the IC's switching even at higher frequencies than the series resonance with their interconnects. Otherwise, the decoupling capacitors are designated as *global decoupling capacitors* with regard to the IC, and they will begin losing their effectiveness after the series resonance frequency.

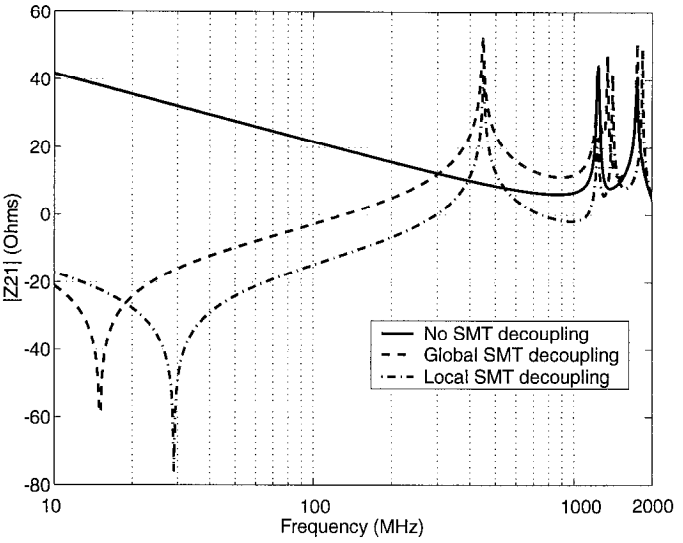

Figure 6(c): Comparison of the modeled $|Z_{21}|$ for the bare board, global decoupling, and local decoupling.

Local decoupling capacitors can be effective in mitigating power bus noise depending on proximity to an IC, and the power layer thickness. However, when the capacitors are located near the IC, they may limit the routing flexibility. Tradeoffs must be made to achieve design requirements. Therefore, quantifying the benefits of local decoupling based on the IC/capacitor spacing and layer thickness is desirable to facilitate the design.

A 6″×9″ two-layer PCB was the power bus structure modeled using CEMPIE for the SMT decoupling capacitor placement study. As shown in Figure 7, SMT decoupling capacitors with individual value of 0.01 μF were uniformly distributed over the board. The spacing between capacitors was 1″. The input port was located on the board with the spacing to the left edge and the bottom edge equal to 2″, as shown in Figure 7. This port location was carefully chosen to avoid specific board resonance locations. Five output ports were selected so that an average response could be calculated to avoid non-general cases. Either one or four decoupling capacitors were added adjacent to the input port. For the latter case, all the four capacitors were located on the circle centered at the input port. The spacing between these local capacitors and the input port, as well as the board thickness, varied, and the effect of the local decoupling compared with the case without local decoupling was quantified.

$|Z_{21}|$ between input and output ports was modeled. As indicated previously, $|Z_{21}|$ is a transfer impedance that determines the noise voltage at the output port for a given noise current at the input port. A larger $|Z_{21}|$ indicates a larger noise voltage results at the output port for a given injected current at the source port. Figure 8 shows the modeled results

for a 44 mil PCB with the structure shown in Figure 7, and only one local decoupling capacitor present. The cases with 4 local decoupling capacitors are shown in Figure 9. Both figures indicate that the local decoupling did exhibit lower magnitudes than the case without local decoupling. Further, the decrease in magnitude was approximately frequency-independent in the whole frequency range from 100 MHz to 2 GHz. The $|Z_{21}|$ also decreased with the spacing between the local decoupling capacitor(s) and the input port. The number of local decoupling capacitors greatly improved the local effect, which can be explained by an increase in the mutual inductive coupling between multiple vias. The frequency-independent shift in the curves can be explained in terms of the self- and mutual-inductances of the input port and local decoupling capacitor vias using a hybrid lumped element model for the vias and distributed Z-parameters for the board and other global decoupling capacitors.

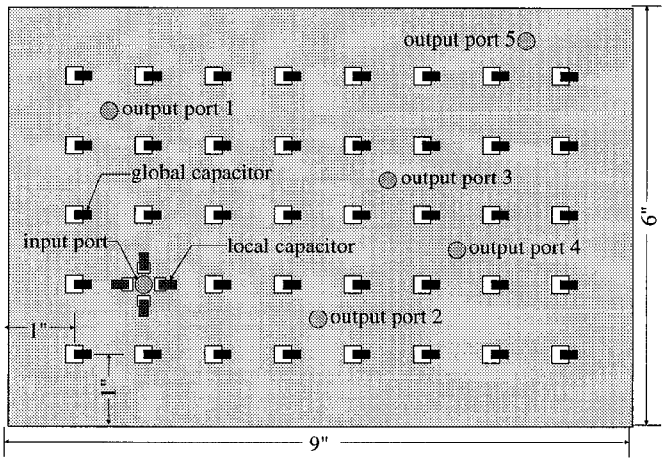

Figure 7: Modeling structure for the local decoupling study.

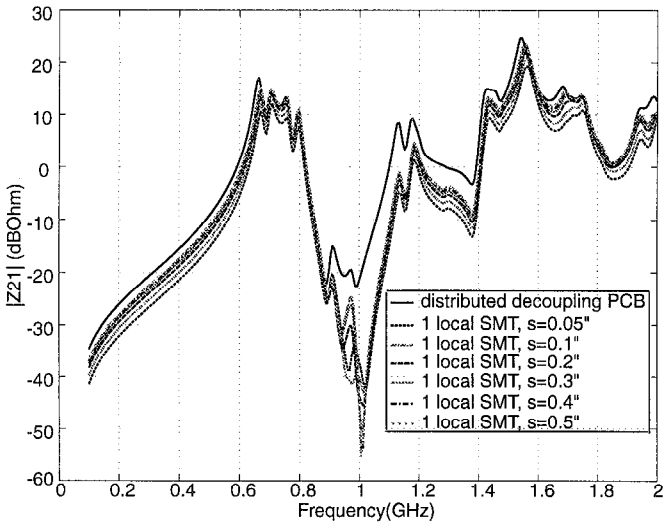

Figure 8: Modeled results for a 44 mil PCB with one local decoupling capacitor.

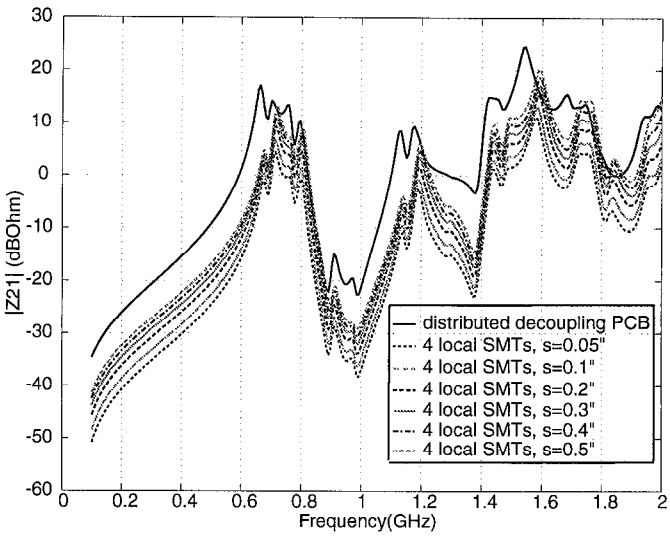

Figure 9: Modeled results for a 44 mil PCB with four local decoupling capacitors.

Since the $|Z_{21}|$ decrease due to local decoupling was frequency-independent in the frequency range of interest (100 MHz to 2 GHz), an average magnitude difference with regard to the baseline case without the local decoupling over all the frequency points can be used to quantify the local decoupling effects. This average was also taken over the five output ports indicated in Figure 7. Several cases with different spacing between the input port and local decoupling, as well as layer spacing between the power and ground planes, were modeled with CEMPIE. The average $|Z_{21}|$ differences were quantified, and design curves based on these results were generated. These curves can be used to determine whether a local decoupling effect is achievable for a given power bus geometry, and to compromise between the benefits from local decoupling and routing flexibility near IC chips.

Figure 10 shows the average $|Z_{21}|$ decrease due to local decoupling versus the spacing between the local decoupling and the input port. Three different boards with layer spacings of 30, 44, and 60 mils were modeled. The board material was FR-4 with a relative dielectric constant of $\varepsilon r=4.7$, and loss tangent of $\tan\delta=0.02$, for all the three PCBs. Either one or four local decoupling capacitor(s) were present on the board. As mentioned previously, the four local capacitors were symmetrically located on the circle centered at the input port. In practical design, however, it may not be feasible to place capacitors around the IC power pin. Therefore, the modeled results give an upper bound on the benefit that can be achieved with four local decoupling capacitors. Every data point is an average number over the whole frequency band from 100 MHz to 2 GHz, and over the five output ports as well.

From Figure 10, it is clear that the local decoupling is more dominant in a thicker power layer, and multiple local capacitors greatly enhance the local effect. In the design phase, when the minimum spacing between a local decoupling SMT and the IC chip is determined after careful evaluation of

other important issues such as routing flexibility, PCB manufacturing, component assembling, etc., the reduction on power bus noise with the local decoupling can be approximated using the curves shown in Figure 10, provided that the layer spacing has already been specified. If several dB of reduction is achievable, locating the decoupling capacitor in proximity to an IC is beneficial, otherwise locating the decoupling capacitor where minimal inductance interconnects can be achieved is sufficient.

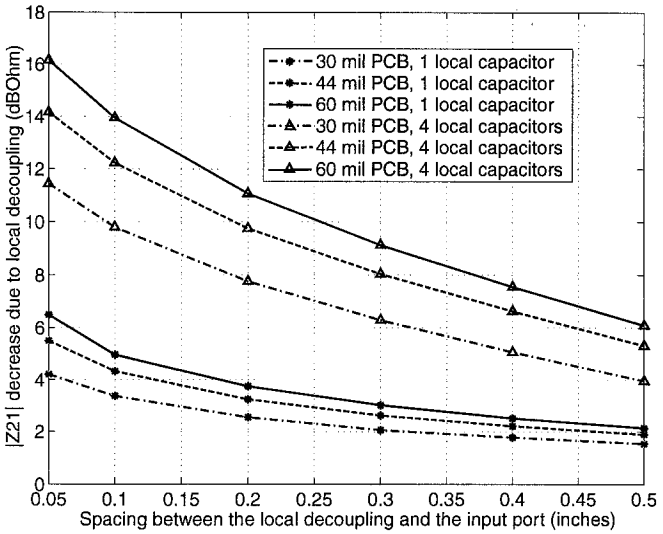

Figure 10: Decrease in $|Z_{21}|$ versus spacing between the local decoupling and the input port.

V. Conclusions

Mutual inductance between two closely spaced vias exists, and plays an important role in local decoupling, demonstrated herein with both populated PCB measurements and power bus modeling. Local decoupling capacitors can effectively supply charge to IC's switching at high frequencies, even beyond their series resonance frequency. The effect on power bus noise reduction in terms of $|Z_{21}|$ due to local decoupling was studied. Design curves for thick power layers were generated for power bus and SMT decoupling designs. For thin power layers, the local decoupling effect is not as significant as for the thick power layers, and achieving local decoupling benefits is impractical.

VI. References

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