# Inductance Calculations For Advanced Packaging in High-Performance Computing

Hocheol Kwak, Haixin, Ke, Todd Hubing
The Clemson Vehicular Electronics Laboratory,
Dept of ECE, Clemson University,
Clemson, SC, U.S.A

Byoung Hwa Lee
EMC Team, Samsung Electro-Mechanics
Suwon, Gyeonggi, Korea

***Abstract*— Effective decoupling is crucial for the optimum performance of the power distribution network in an electronic system. As component packaging technologies evolve enabling tighter integration and faster operation of electronic systems, it is important to develop better decoupling strategies. This paper describes several new or proposed packaging structures and evaluates the connection inductance associated with possible decoupling capacitor locations. As expected, connections made on the chip tend to have a lower inductance than connections made on the package; and connections made on the package tend to have a lower inductance than connections made to the board. This illustrates the importance of providing decoupling capacitance as close to the chip as possible in order to maximize the effective bandwidth of the power distribution network.**

***Keywords-decoupling capacitor; power distributed network; advanced packaging; connection inductance;***

## I. INTRODUCTION

Power bus decoupling issues in electronic systems are shifting from the printed circuit board level to the component packaging level. This trend is being driven by the miniaturization of electronic systems and the shift of the package manufacturing process to the IC foundry level. Traditional wire bonding technology is steadily being replaced by area array (bump) interconnections and three-dimensional silicon integration technologies.

The evolution of advanced packaging techniques is being driven by two electronic device platforms; mobile communication applications with an emphasis on miniaturization, and computing applications with an emphasis on high performance. High-density integration is required for both platforms. Ultimately, the roadmap of both platforms calls for the implementation of SOC (System-on-Chip) or SOP (System-on-Package) structures including; 3D chip stacks, silicon carrier packaging, silicon interconnection or bonding, cu-to-cu stud bonding and integrated decoupling capacitors [1].

Advanced packaging includes wafer-level and 3D stacked IC as well as traditional packaging technologies [2]. Vertical interconnection technology for different packaging levels is evolving from traditional wire bonding and flip-chip bumping to wafer-level packaging and cu-to-cu bonding. Key design parameters for power bus decoupling of advanced packaging structures can be categorized depending on the location or type of decoupling capacitor. Decoupling capacitors can be discrete, singulated or distributed. They can be individual local capacitors or global arrays.

## II. DECOUPLING SCHEMES FOR HIGH-PERFORMANCE ADVANCED PACKAGING

Figure 1 illustrates five possible locations for the decoupling capacitors in a high-performance package;

- stacked on chip
- stacked on si-carrier
- top side of package substrate
- bottom side of package substrate, and
- embedded in the package substrate.

The current paths, including the dominant factors affecting the loop inductance, are described for each location.

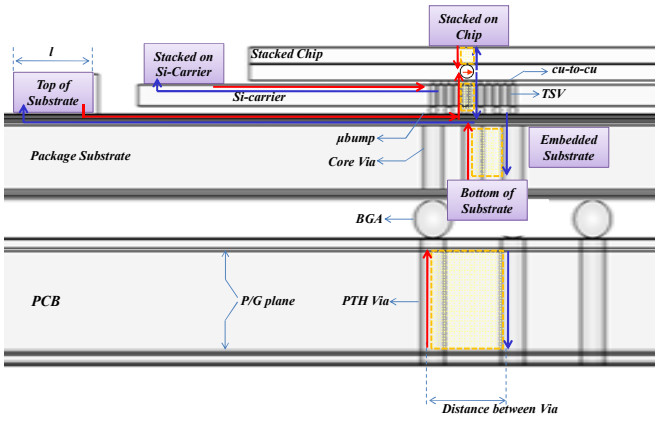


Figure 1. Possible locations of decoupling capacitors in high-performance packaging.

### A. Loop inductance of two vias by different packaging levels

As illustrated in Figure 1, the 'stacked on chip' location is closest to the source and permits the lowest possible connection inductance. A typical inductance calculation for a 'stacked-on-chip' decoupling capacitor is determined by modeling the current path as a pair of vias between two solid planes. This

978-1-4244-1699-8/08/$25.00 ©2008 IEEE

model is reasonable because the on-chip grids that connect to the vias are relatively wide and contribute little to the overall path inductance. For example, suppose that the radius of the through-silicon vias is 5 µm, the distance between adjacent vias is 50 µm, and the height of die is about 200 µm. Via inductances associated with vias can be calculated using the following formula:

$$L_{via\ between\ planes} = \frac{\mu_0 h}{2\pi} \ln\left(\frac{s}{r}\right) \quad (1)$$

where h is via length, r is the via radius and s is the spacing between the two vias [11]. In this case, the connection inductance would be 92 pH. The via resistance would be, $R=2h/\sigma\pi r^2 = 89m\Omega$. The inductance would be more important than the resistance at frequencies above about 150 MHz.

Table I shows the inductance of two vias between planes for different interconnection levels and typical values of capacitance available at each of these leads. Figure 2 illustrates this trend schematically.

TABLE I.
Comparison of typical capacitance and loop inductance of two vias by different packaging levels.

| Packaging level | Via types | Vertical scaling, h (µm) | s (µm) | r (µm) | L (nH) | C | Operating Frequencies |
|---|---|---|---|---|---|---|---|
| PCB | PTH | 1200 | 1000 | 150 | 0.5 | 2.2 µF | 72 kHz - 320 MHz |
| Package Substrate | Core via | 800 | 75 | 125 | 0.3 | 0.1 µF | 1.6 MHz - 530 MHz |
| Si-Carrier | TSV | 300 | 100 | 35 | 0.06 | 0.01 µF | 160 kHz - 2.6 GHz |
| IC | TSV | 200 | 100 | 5 | 0.2 | 0.01 µF | 160 kHz – 800 MHz |

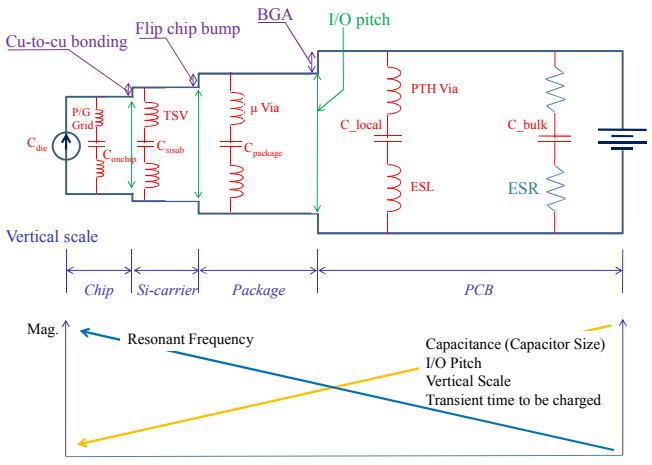


Figure 2. Equivalent circuit diagrams by different packaging levels.

Note that the connection inductances tend to get lower as we locate the decoupling capacitors nearer the source on the chip. This suggests that capacitors within the packaging structure will be more effective than capacitors on the board at higher frequencies.

The amount of capacitance available limits the low-frequency effectiveness of the decoupling. The connection inductance limits the high frequency effectiveness. For a given target impedance, we can calculate the range of frequencies that a given capacitor is expected to be effective,

$$\frac{1}{2\pi |Z_{target}| C} < f < \frac{Z_{target}}{2\pi L} \quad (2)$$

Operating frequencies for a target impedance of 1 ohm are shown in the last column of Table I. Note that these are typical values. In many applications the target impedance will be different than 1 ohm and the effective frequency range of the various package levels will vary.

### *B. Loop inductance in top/bottom-side of package substrate*

Design strategies for mounting decoupling capacitors on either side of the package substrate can be divided into two cases depending on the distance between the power planes of a multi-layer package substrate [6].

On circuit boards with closely spaced power planes, ~ 0.3 mm or less, the location of the local decoupling capacitors is not critical. To minimize the connection inductance, all local decoupling capacitors should be mounted on the face of the board nearest to the planes. Capacitors should be connected directly to the planes without using traces. Vias should be in or adjacent to the capacitor mounting pads as close to each other as possible. When a chip and decoupling capacitor are both mounted on the top side of the package substrate, the inductance of the loop can be expressed as the sum of the inductances of the two half-loops above the top plane and the inductance of the loop between the planes.

When the spacing between the planes is less than ~0.3 mm, the inductance of the loop between the planes tends to be small relative to the connection inductance above the planes. When the spacing between the planes is greater than ~0.5 mm, the inductance between the planes is no longer negligible. In fact, by placing the vias that carry current to and from the lower plane near each other, it is possible to take advantage of the mutual inductance between these vias to force the current to be drawn from the decoupling capacitor rather than the planes. This reduces the noise on the power planes [6]. Therefore, when the planes are >0.33 mm apart, it is important to locate the decoupling capacitors near the source.

When the capacitor is mounted on the same side of the board as the device it is decoupling, it can share the via connecting to the lower plane with the active device. When the capacitor is on the opposite side of the board, the calculation of the inductance is done using the same formulas used when the capacitor is on the same side as the active device. However, the currents flowing on the vias in between the planes are now being drawn from different planes. The rules for locating the decoupling capacitors are the same, except it is no longer possible to share the via that carries current between the planes. Therefore, the active device and the capacitor should each have their own vias connecting to the planes (i.e. they should not share vias).

## III. INDUCTANCE CALCULATIONS FOR MLCCS ON A PACKAGING SUBSTRATE

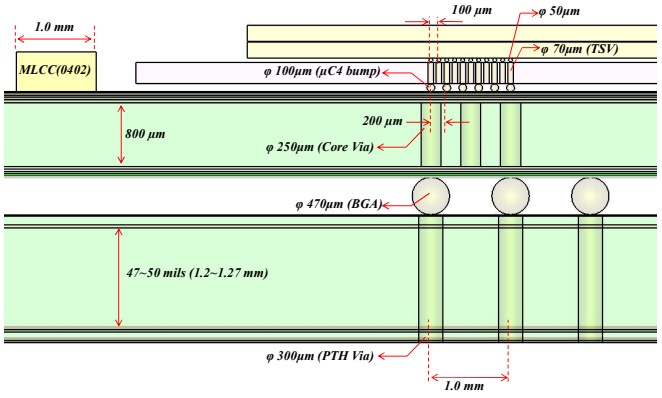


Figure 3. An example of advanced packaging in a computing application.

Figure 3 shows an example of a package structure in a high-performance computing application. The stacking order from the bottom up is the printed circuit board, then the package substrate (organic interposer), and finally the silicon-carrier package and possibly stacked dies. The possible interconnection technologies are solder bump, flip-chip bumping, through-silicon vias and cu-to-cu bonding. Multi-layer decoupling capacitors may be mounted on or in the circuit board, on or in the interposer, or between the stacked dies. Figure 3 illustrates how the vertical scaling reduces as one moves from the bottom to the top of the geometry.

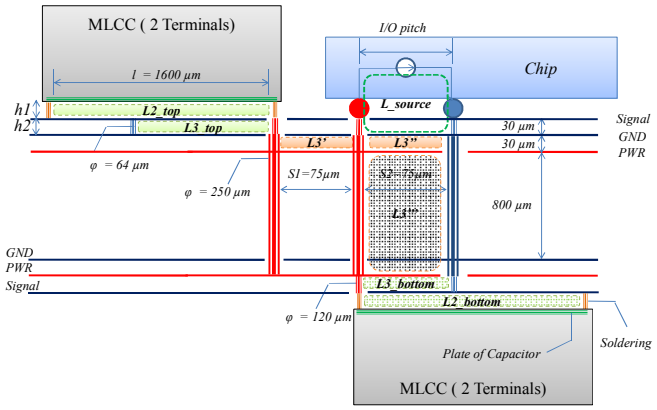


Figure 4. Possible locations of the decoupling capacitors on a packaging substrate.

Figure 4 illustrates how two 1608-size decoupling capacitors would typically be located on the top or the bottom of a packaging substrate. We can determine which position has the lower connection inductance by using simple analytical formulas for determining connection inductance [12].

TABLE II.
Inductance calculation of current packaging structure.(l > 5h, h<<a, w >> h)

| Location | Total inductance (nH) | L2_top (bottom) (nH) | L3_top (bottom) (nH) | L3' (nH) | L3" (nH) | L3"' (nH) |
|---|---|---|---|---|---|---|
| On the Top side | 0.12 | 0.1 | 0.01 | 0.01 | - | - |
| Bottom side | 0.43 | 0.1 | 0.01 | 0.01 | 0.01 | 0.30 |

In the case of the top-side location, the total connection inductance is equal to the sum of the loop inductances denoted as L2_top, L3_top, L3' and L_source. In the case of the bottom-side location, the total connection inductance is equal to the sum of L2_bottom, L3_bottom, L3'', L3''' and L_source. If there is no metal plane on the signal layer adjacent to the decoupling capacitor, L2_top and L3_top must be considered one loop instead of a two separate loops. Even though this L2_top-L3_top loop is not rectangular, a good estimate of the inductance can be obtained by approximating the loop as a rectangle with an equivalent area.

In the top-mounted case, the total connection inductance (L2_top + L3') was about 0.12 nH compared to 0.43 nH (L2_bottom + L3" + L3"') on the bottom. In this case, the decoupling capacitor located on the top side has a lower connection inductance than the capacitor on the bottom side. The difference is primarily due to the inductance associated with the loop area between the inner planes, L3'''.

## IV. CONCLUSIONS

Power bus decoupling inductance for high performance packaging in computing applications is decided primarily by the loop area formed by the current path from the switching device to the decoupling capacitor and to a lesser extent by the effective radius of the connecting conductors. The spacing between the power and ground layers in the packaging substrate, the height of through-silicon vias in the silicon carrier substrate and the solder ball diameter for flip-chip bumping are all key factors when calculating the connection inductance. Another important factor is the horizontal distance between the vias carrying current to and from the decoupling capacitor. Vias should be placed close to each other to reduce the inductance of the path.

In general, the inductance of structures on the chip is lower than the inductance of structures in the package and package inductances tend to be lower than inductances on the board. Therefore, it is important to have at least some amount of decoupling capacitance at each level of packaging to meet the broadband decoupling requirements of high-speed devices.

## REFERENCES


[1] John U. Knickerbocker, Chirag S. Patel, "Three Dimensional Silicon Integration Using Fine Pitch Interconnection, Silicon Processing and Silicon Carrier Packaging Technology," *IEEE 2005 Custom Integrated Circuits Conference*, pp. 659-662, Sep. 2005.

[2] Philip Pieters, Eric Beyne, "3D Wafer Level Packaging Approach Towards Cost Effective Low Loss High Density 3D Stacking," *7th International Conference on Electronics Packaging Technology*, pp. 1-4, Aug. 2006.

[3] J.U. Knickerbocker, P.S. Andry, "Development of next generation system-on-package (SOP) technology based on silicon carriers with fine-pitch chip interconnection," *IBM Journal RES. & DEV.* vol.49, no. 4, Jul. 2005.

[4] Larry E. Mosley, "Capacitor Impedance Needs for Future Microprocessors," pp. 193-203, *CARTS USA*, Apr. 2006.

[5] Tadahiro Kuroda, "System LSI: Challenges and Opportunities," *IEICE Transactions Electron*, vol. E89-C, no.3, Mar. 2006.

[6] Todd Hubing, "Effective Strategies for Choosing and Locating Printed Circuit Board Decoupling Capacitors," *IEEE International Symposium on EMC,* vol. 2, pp. 632–637, Aug. 2005.

[7] James L. Knighten, et. al., "PDN Design Strategies II. Ceramic SMT Decoupling Capacitors – Does Location Matter?" *IEEE EMC Society Newsletter*, pp. 56–67, winter 2006.

[8] Sudhaker Bobba, Tyler Thorp, "IC Power Distribution Challenges", *IEEE/ACM International Conference on Computer Aided Design*, pp. 643-650, Nov. 2001.

[9] J. Fan et al., "Quantifying SMT Decoupling Capacitor Placement in DC Power-Bus Design for Multi-Layer PCBs", *IEEE Transactions on Electromagnetic Compatibility*, vol. 43, no. 4, pp. 588-599, Nov. 2001.

[10] C. Wang et al., "An Efficient Approach for Power Delivery Network Design with Closed-Form Expressions for Parasitic Interconnect Inductance," *IEEE Transactions on Advanced Packaging*, vol. 29, no.2, pp. 320-334, May 2006.

[11] Todd H. Hubing, T.P Van Doren and J. L. Drewniak, "Identifying and Quantifying Printed Circuit Board Inductance", *IEEE International Symposium on EMC,* pp. 205-208, Aug. 1994.

[12] T. Zeeff, "Estimating the Connection Inductance of a Decoupling Capacitor," *UMR EMC Laboratory Technical Report*, TR01-1-030, University of Missouri-Rolla, Jun. 2001.