Monitoring Transistor Degradation in Power Inverters Through Pole Shifts

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Abstract— *In a power inverter configuration with pull-up and pull-down transistors, ringing that occurs on the high-to-low and low-to-high transitions can be used to track aging and predict failures. As the transistors age or are damaged, changes in their equivalent resistance and capacitance can affect the frequency and damping factor of the characteristic ringing detected on the inverter's output. The Matrix Pencil Method can be used to locate the poles associated with this ringing and detect shifts in position that indicate transistor degradation.*

Keywords— Matrix Pencil Method, Transistor Degradation, Ringing, Failure Prediction Introduction

I. Introduction

When an inverter circuit has both pull-up and pull-down transistors, some ringing will occur on both the high-to-low and low-to-high transitions of the output. This ringing is due to the resistance, capacitance, and inductance of a current loop formed by the inverter pair [1],[2].

The Matrix Pencil Method (MPM) is a technique for plotting the pole locations associated with a ringing waveform. The pole locations describe both the ringing frequencies and damping factors, making them more useful than an FFT, which provides amplitude and phase information for the various spectral components.

As the inverter's transistors age or are damaged, changes in their capacitance and resistance can cause a change in the frequency and damping of the inverter's characteristic ringing. This change produces a shift in pole locations that can be detected and quantified using the matrix pencil method.

II. Test Circuit Description

In the test bed circuit shown in Fig. 1 [3], the high-side transistor is driven with a PWM signal. The period and duty cycle of the PWM can be varied to examine the behavior of ringing under different operating conditions. Note that in this test circuit, the gate of Q2 is permanently tied low, causing Q2 to remain off at all times. This causes the low-side transistor to remain in a known state at all times. The ringing current in this instance is expected to follow the path shown in blue in Fig. 1.

This ringing characteristic is dependent upon the manner of operation. For example, in Fig. 1 when Q1 is on and Q2 is off, the output is in a high state. Turning off Q1 results in a high-to-low transition. A transistor that has been switched on is modeled as the resistance $R_{DS(ON)}$. A transistor that is off is modeled as the series combination of its output capacitance, C_{OSS}, and resistance, R_{OSS} [1]. The lower body diode (LBD) is modeled as a current-dependent resistance. When the LBD isn't conducting, its equivalent resistance is very high. When it is conducting, its equivalent resistance is relatively low and is a function of the amount of drain current.

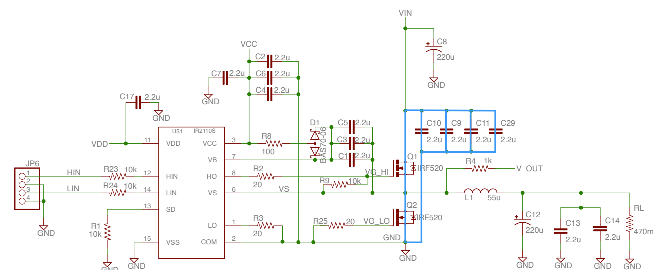

Fig. 1. Ringing current path in MOSFET test bed.

When the circuit of Fig. 1 is constructed on a circuit board, the loop shown in blue has an associated area resulting in a loop inductance. This loop inductance acts in conjunction with the transistor resistance and capacitance to create ringing on V_o. If the LBD is still switched on during the low-to-high transition, the series combination of resistance and capacitance of the lower transistor is in parallel with the LBD impedance.

III. Ringing Equivalent Circuit

A circuit board layout corresponding to the circuit in Fig. 1 is shown in Fig. 2. A picture of the constructed test bed is provided in Fig. 3. While the size of the loop outlined in Fig. 1 is relatively small as implemented in this circuit board, the transistor sockets that facilitate the rapid testing of multiple transistors add inductance to this loop. The loop inductance with the transistor sockets included is approximately 10 nH.

While the loop inductance is a very important factor contributing to the ringing, it does not change over time or with transistor degradation. It is also the same for both high-to-low and low-to-high transitions. The equivalent resistance and

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capacitance of the loop depend on transistor age, damage, operating voltages, and on which transition is monitored. Fig. 4 shows the equivalent circuit for a low-to-high transition of V_o.

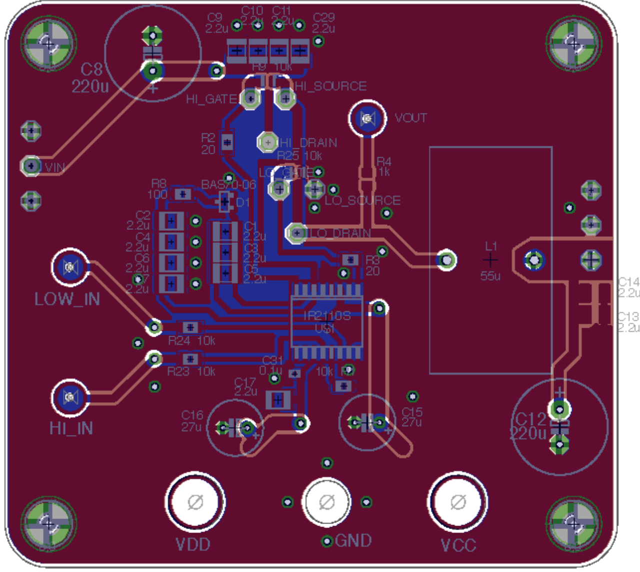

Fig. 2. Board layout of MOSFET test bed.

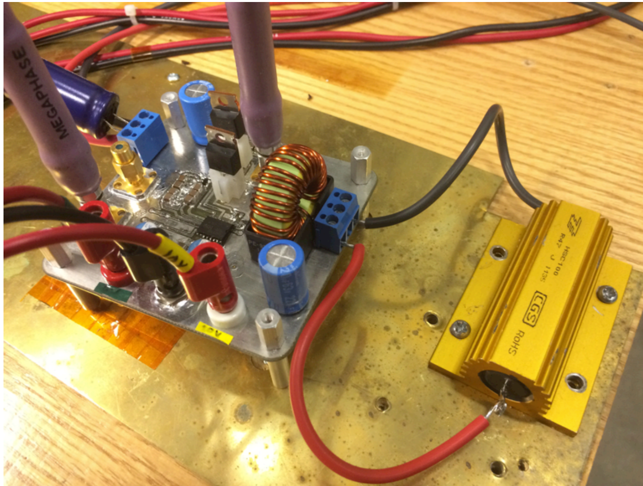

Fig. 3. MOSFET test bed.

For this transition, the high-side transistor is switched on while the low-side transistor remains in its permanent (for this application) off state. The low-side transistor can be modeled as a series RC, and because the PWM period and duty cycle have been chosen such that the LBD is not conducting on the subsequent pulse, the effect of the LBD can be neglected. The high-side transistor is on for this transition and can be modeled simply as a resistor.

Low-to-High Transition of V_o

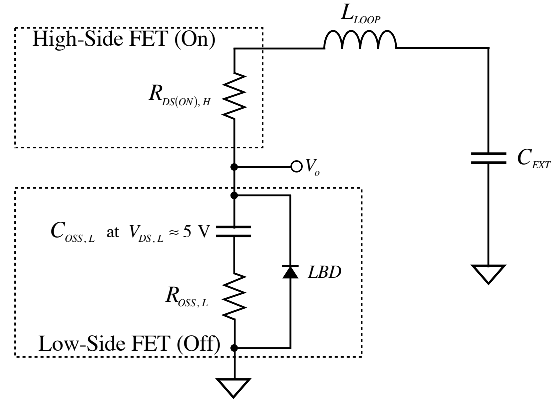

Fig. 4. Equivalent circuit for low-to-high transition of V_O.

The equivalent decoupling capacitance, C_{EXT}, is large compared to C_{OSS}, and since it is in series with C_{OSS}, it can be neglected in most circumstances. C_{OSS} is dependent upon V_{DS}, which is approximately 5 V for the lower transistor on the low-to-high transition. In the case of the low-to-high ringing, the ringing frequency is approximately

$$f_{lh} \approx \frac{1}{2\pi\sqrt{L_{LOOP} \cdot C_{OSS,L\ (V_{ds} \approx 5\ \mathrm{V})}}}, \tag{1}$$

while the damping coefficient can be approximated by

$$\alpha_{lh} \approx \frac{R_{DS(ON),H} + R_{OSS,L}}{2L_{LOOP}}. \tag{2}$$

For the high-to-low transition, the equivalent circuit is shown in Fig. 5.

High-to-Low Transition of V_o

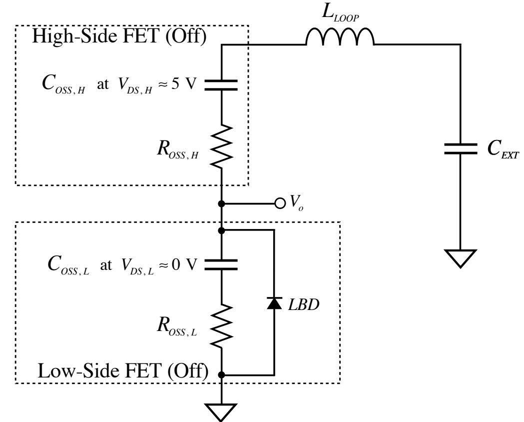

Fig. 5. Equivalent circuit for high-to-low transition of V_O.

As with the low-to-high transition, the low-side transistor can be modeled as a series RC, neglecting the LBD. Because the high-side transistor is off for this transition, it can also be modeled as a series RC. For the high-to-low transition, the $V_{DS,L}$ is different than that of the low-to-high transition. This means that the low-side transistor will not have the same equivalent capacitance for both transitions; however, the high-side transistor on the high-to-low transition will have approximately the same equivalent capacitance as the low-side transistor during the low-to-high transition. L_{LOOP} again represents the equivalent inductance of the loop, and C_{EXT} can be ignored because of its relatively large value. Similar to the low-to-high case, the frequency of the high-to-low transition can be approximated by

$$f_{hl} \approx \frac{1}{2\pi\sqrt{L_{LOOP}\cdot\left[\frac{\left(C_{OSS,H\ (V_{ds}\approx 5\text{ V})}\right)\left(C_{OSS,L\ (V_{ds}\approx 0\text{ V})}\right)}{\left(C_{OSS,H\ (V_{ds}\approx 5\text{ V})}\right)+\left(C_{OSS,L\ (V_{ds}\approx 0\text{ V})}\right)}\right]}} \quad (3)$$

and the damping coefficient is approximately

$$\alpha_{hl} \approx \frac{R_{OSS,H}+R_{OSS,L}}{2L_{LOOP}} . \quad (4)$$

IV. Description of the Matrix Pencil Method

A decaying transient response can be represented by a linear combination of complex exponentials. The Matrix Pencil Method provides an easy way of extracting the complex poles associated with these waveforms [4]. It is similar to the Pencil of Functions approach, but has improved noise immunity. It also has better performance than the polynomial method [5]. The pole locations indicate both the ringing frequencies and damping factors associated with the spectral components. In the case of complicated systems with multiple resonances, the Matrix Pencil Method is able to extract more than one pole at a time. The exact number of poles that can be extracted is determined by the noise floor, and is closely related to the precision of the measured data.

In our tests, the output voltage of the inverter circuit was recorded with an oscilloscope and processed in Matlab. The captured waveforms were windowed and filtered before the matrix pencil method was applied to calculate the complex poles. Some of the poles observed are due to noise and slight, low-frequency variations in the waveform. Based on the estimated resistance, capacitance, and inductance of the ringing current loop, the main pole of interest can be separated from the rest. The real part of the pole represents its damping factor, while the imaginary part represents its ringing frequency.

The plot in Fig. 6 shows the output voltage of the test bed from Fig. 3 when an unaged transistor is placed in the high-side transistor socket. The plot on the left in Fig. 6 shows a spike in V_o at roughly 75 µs, when the LBD stops conducting, which is before the subsequent pulse. This makes analysis of the resultant MPM poles easier [3].

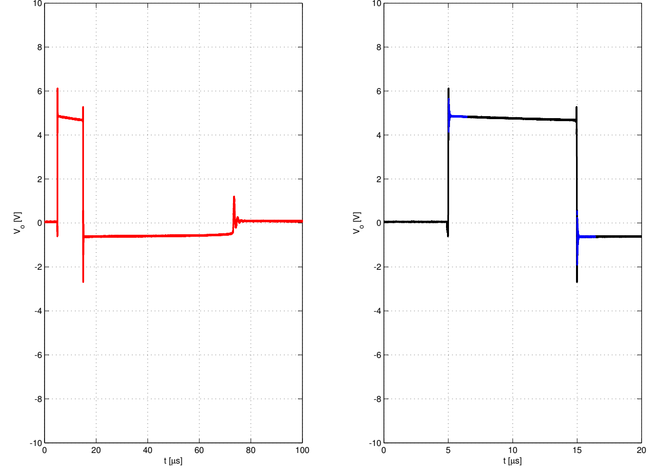

Fig. 6. V_O for an unaged transistor.

The plot on the right in Fig. 6 is a zoomed-in view of the plot on the left showing the ringing on the high-to-low and low-to-high transitions. The ringing on each transition was captured and processed, and the resultant poles are shown in Fig. 7.

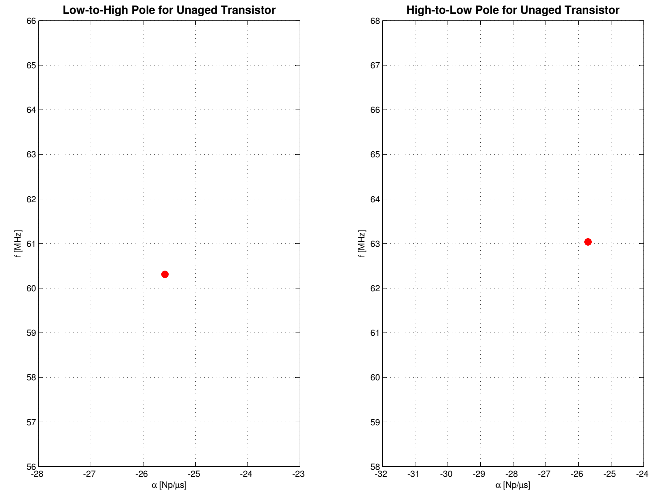

Fig. 7. MPM Poles of the ringing of an unaged transistor.

It has been shown that an FFT can be used to track changes in frequency due to transistor degradation [6]. While damping information can also be determined from an FFT, the MPM provides an advantage over the FFT by making the damping information easier to obtain accurately. From (1) through (4), changes in frequency will be caused by changes in capacitance while changes in damping will be caused by changes in resistance. Using an FFT to track device degradation, only events that alter device capacitance will be easily detected. With the MPM, events that alter either the resistance or capacitance can be detected with equal proficiency.

V. METHOD OF ARTIFICIALLY AGING TRANSISTORS

There are many different methods that can be used to artificially age transistors. In normal operation, transistors can be subjected to many stresses, including rapid thermal cycling, overvoltage (including ESD), and overcurrent. Each of these scenarios can be utilized and adapted to artificially simulate many hours of operation in a short amount of time.

Simulating an ESD event replicates a real-world occurrence that can degrade or even destroy a MOSFET. By tweaking the method of discharge, voltage, and number of discharge events, MOSFET transistors can be effectively degraded but not destroyed.

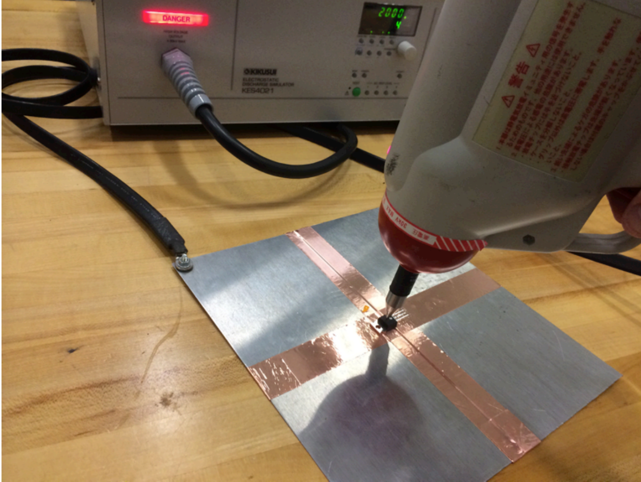

Fig. 8. Transistor aging platform.

The ESD aging setup used in this work is shown in Fig. 8. The ESD simulator was a Kikusui KES4021. The transistor to be aged was placed in the center of the ground plane with its tab on the ground plane pointed towards the ground strap of the ESD simulator. With the contact discharge tip placed at the center of the epoxy package, 4 pulses at 20 kV were generally found to provide enough degradation to be detectable without destroying the transistor. There is an inherent amount of inconsistency with the ESD event in this process. Slight misalignment of the discharge tip from the center of the package can cause the discharge to either be more or less destructive than desired.

VI. POLE SHIFTS DUE TO TRANSISTOR DEGRADATION

To evaluate possible pole shifts due to transistor degradation, each transistor was placed in the test bed and operated for 10 minutes before its pole location was determined five times. Five measurements were done so that a general location for the unaged pole location could be determined. Next, the unaged transistor was subjected to ESD as described in the previous section. If the transistor survived this process, it was placed back in the test bed and its pole location was again determined five times. The output voltage from an ESD degraded transistor is shown in Fig. 9.

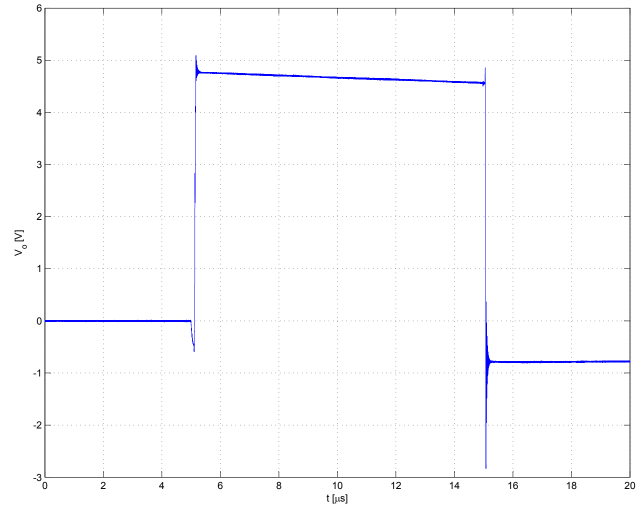

Fig. 9. V_O of an ESD degraded transistor.

A clear difference in the waveforms from Fig. 6 and Fig. 9 can be seen. A plot of both unaged and aged pole locations for the high-to-low transition of three transistors is shown in Fig. 10.

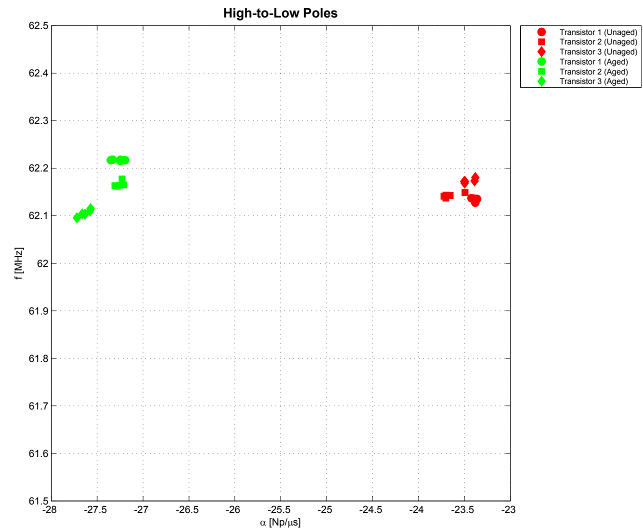

Fig. 10. MPM poles of three transistors before and after ESD degradation.

In this case, since the high-side transistor was subjected to degradation, only the high-to-low ringing was observed in order to track pole shifts. Doing so provides the ability to track changes in both the resistance and capacitance of the high-side transistor. In Fig. 10, each transistor's pole location clearly shifts left after it has been subjected to ESD. This shift indicates an increase in damping when the transistor has been aged.

By examining (4), an increase in damping corresponds to an increase in the series resistance of a transistor. Fig. 10 shows an increase in damping on the order of 15%. If

$$\alpha_{hl\,,\,\text{aged}} \approx 1.15 \cdot \alpha_{hl\,,\,\text{unaged}} \quad , \qquad (5)$$

then the approximate change in resistance can be found by substituting (4) into (5), which yields

$$R_{OSS\,,\,H\,,\,\text{aged}} \approx 1.15 \cdot R_{OSS\,,\,H\,,\,\text{unaged}} + .15 \cdot R_{OSS\,,\,L} \quad . \qquad (6)$$

This shows that the series resistance increased a little more than 15% as a result of the aging. From (3, no change in frequency indicates that there was very little, if any, change in the capacitance of these transistors after they were aged.

VII. Conclusion

As a transistor ages or becomes degraded, changes can occur that will affect the equivalent resistances and capacitances of the transistor. In this paper, the MPM is used to plot the poles associated with the ringing of unaged high-side transistors in a known test bed. The high-side transistors were then artificially aged by ESD and placed back in the same test bed. A shift in the MPM poles of the aged transistor relative to the unaged transistor was observed. When the transistors were aged in this manner, the ringing poles shifted to the left, indicating an increase in damping but no change in frequency. This increase corresponds to an increase in the high-side R_{OSS} and $R_{DS(ON)}$, and no change in the high-side C_{OSS}. While the ESD did not change C_{OSS} in this case, there are many other processes that can degrade the C_{OSS} of a MOSFET and potentially cause the ringing frequency to shift. If normal aging or device degradation cause changes in either of these parameters, these changes can be detected as a shift in MPM pole locations.

The measurement described in this paper can be performed on switching transistors while they are operating normally. This approach could ultimately be used to monitor the health of power inverters without disrupting the operation of the systems that employ them.

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