An Experimental Investigation of 4-Layer Printed Circuit Board Decoupling

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Abstract - This paper examines the measured power bus impedance of fully populated 4-layer printed circuit boards with internal power and ground planes. Three boards provided by two leading computer companies were evaluated. Each of the state-of-the-art high-speed boards used in this study employed surface-mount decoupling capacitors to reduce noise on the power bus. The boards were measured with and without some or all of their decoupling capacitance. The effectiveness of the decoupling capacitors as a function of location and frequency and the relationship between board impedance and power bus noise was explored. The behavior of 4-layer boards is shown to be quite different than that of boards without planes or boards with closely spaced planes.

INTRODUCTION

In a previous paper [1], the authors demonstrated that multilayer printed circuit boards with low-inductance power distribution planes require a different decoupling strategy than boards that use individual traces to distribute power to the active components. The closely spaced (usually 10 mils or less) power and ground planes in many multilayer boards have a relatively high mutual capacitance, which at high frequencies becomes the primary source of current for the active devices on the board. 4-layer boards, which are widely used throughout the electronics industry, typically have power and ground planes on the inner 2 layers. In order to preserve the structural integrity of these boards, the spacing between the inner 2 layers is usually about 40 mils. Should these boards be decoupled using the same strategy as other multilayer boards, or do they behave more like boards without a power plane? In order to address this question, three high-speed, 4-layer circuit boards were evaluated and the measured results were compared with existing models. The boards (two PC motherboards and a PC video board) were provided by two leading computer companies. All three boards were populated with surface mount components on both sides and employed internal power and ground planes spaced approximately 40 mils apart.

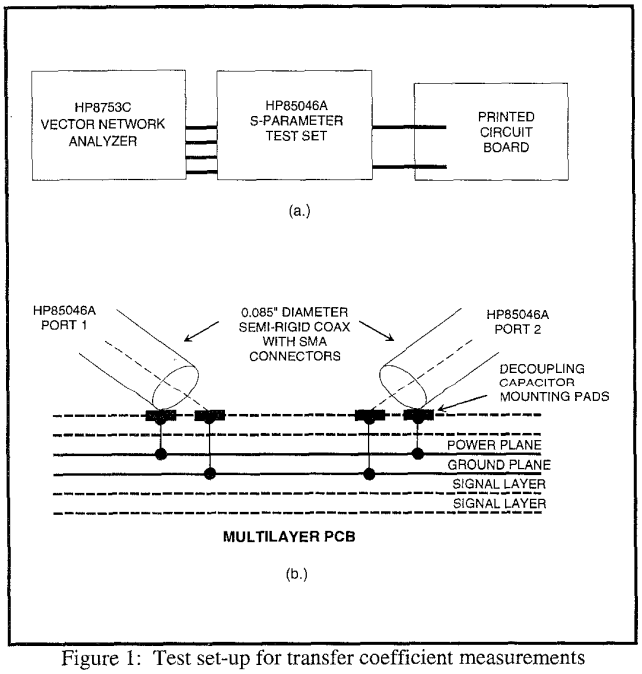

Figure 1: Test set-up for transfer coefficient measurements

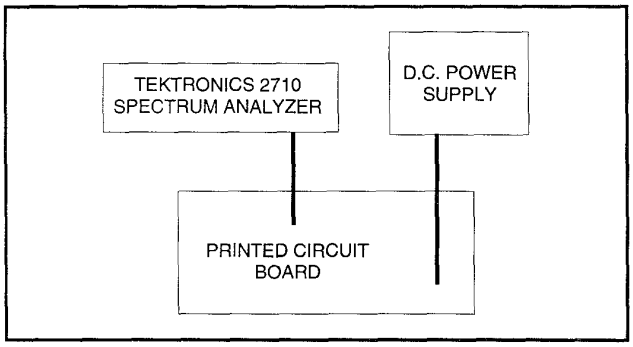

Figure 2: Test set-up for power bus noise measurements

EXPERIMENTAL PROCEDURE

Low inductance probes were attached to the power and ground planes at two locations on each board through existing decoupling capacitor bonding pads. An HP8753C network analyzer with an HP85046A S-parameter test set was connected to the probes as illustrated in Figure 1. A signal was injected at one location and the amplitude of the signal at the second location was measured. The ratio of the measured voltage to the injected voltage, S_{21}, was plotted as a function of frequency. S_{21} measurements provide an indication of how effectively a board's decoupling capacitance reduces the noise at one location on the board due to a source at another location.

In order to verify the correlation between S_{21} measurements and power bus noise, measurements of the power bus voltage were made on one of the boards using a spectrum analyzer. These measurements were

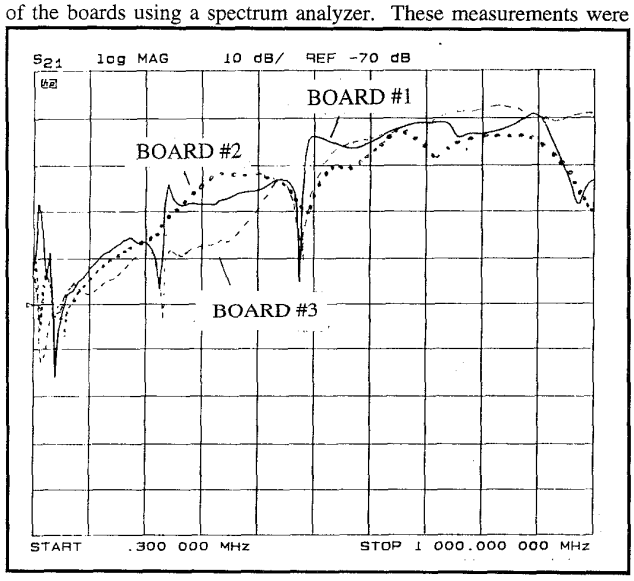

Figure 3: Transfer coefficient of three 4-layer boards

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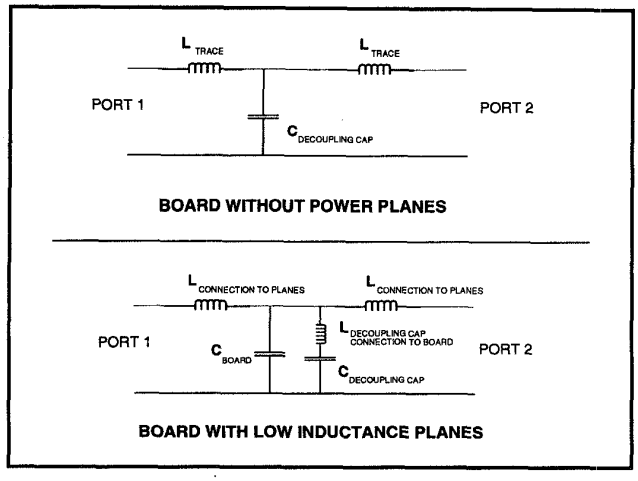

Figure 4: Lumped element decoupling models

made with D.C. power supplied to the board. This test configuration is illustrated in Figure 2.

MUTUAL INDUCTANCE

Figure 3 shows the measured transfer coefficient, S_{21}, for each of the three fully populated boards. At frequencies above 100 MHz, (i.e. beyond the self resonant frequencies of the board decoupling capacitors) the value of S_{21} increases on average, leveling out as the frequency approaches 1 GHz. This result was unexpected, since the transfer ratio of boards with low-inductance power planes and boards without power planes generally decreases at high frequencies. Figure 4 shows simple lumped element models of a board without power planes and a board with low-inductance power and ground planes. At high frequencies the

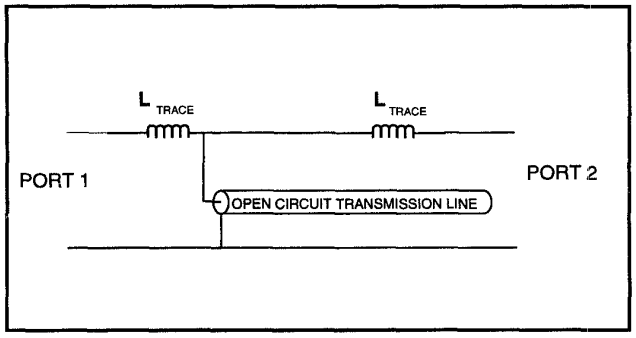

Figure 5: Transmission line decoupling model

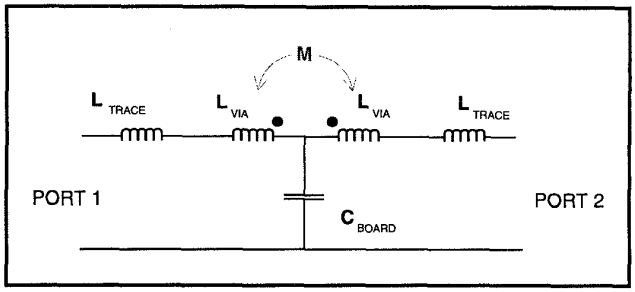

Figure 7: Model that accounts for the mutual inductance

inductance of the component leads dominates the frequency response and in both cases, S_{21} decreases with increasing frequency. At frequencies where a lumped element model is no longer valid due to the electrical size of the board, the lead inductance is still expected to cause the average value of S_{21} to decrease at high frequencies. This concept can be illustrated by the simple distributed circuit shown in Figure 5 where the open circuited transmission line represents the distributed impedance of the power distribution bus. Although there are spikes and nulls in the response of this circuit, eventually the lead inductance takes over reducing the coupling between Port 1 and Port 2.

So how can the measured behavior of the 4-layer boards be explained? Why should a board with a 40 mil power and ground layer spacing be

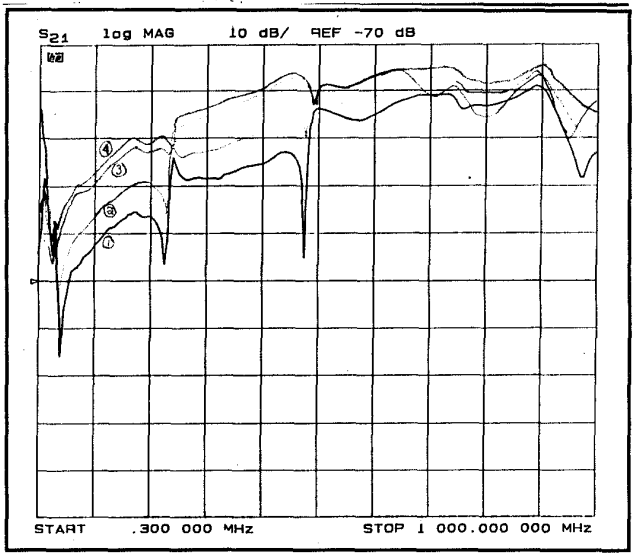

Figure 8: Measured transfer coefficient for Board #1

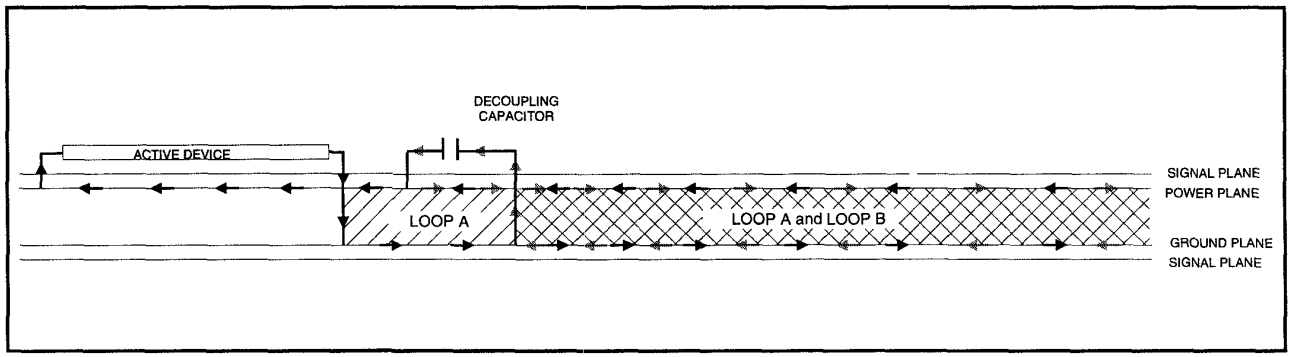

Figure 6: Illustration of flux linkage between planes

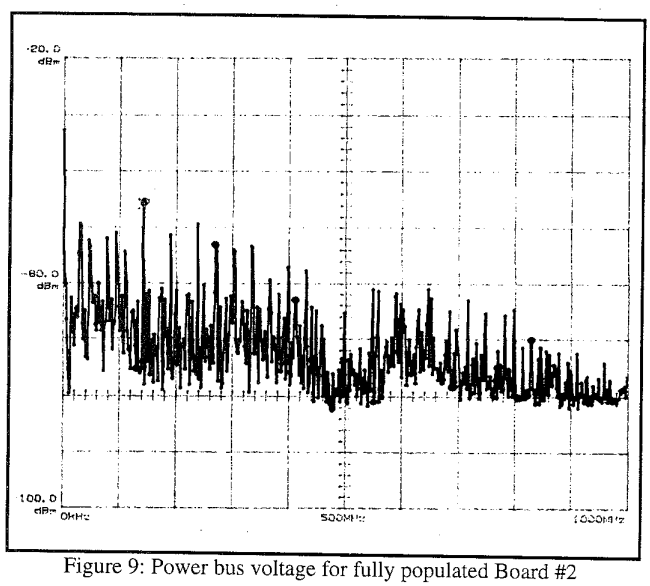

Figure 9: Power bus voltage for fully populated Board #2

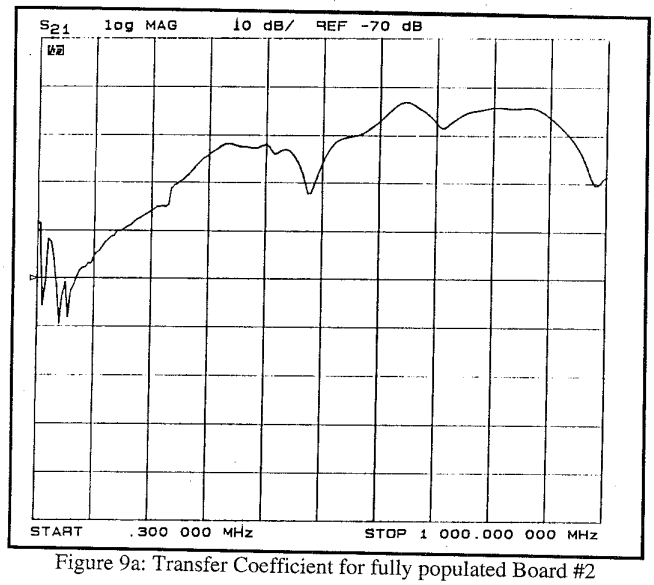

Figure 9a: Transfer Coefficient for fully populated Board #2

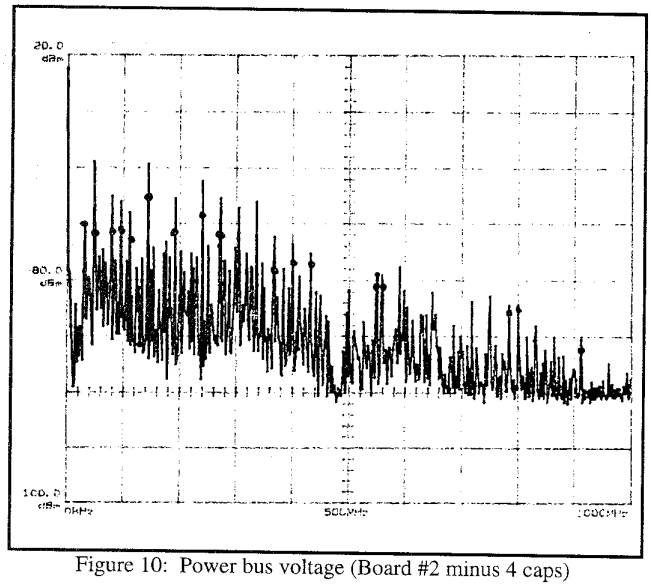

Figure 10: Power bus voltage (Board #2 minus 4 caps)

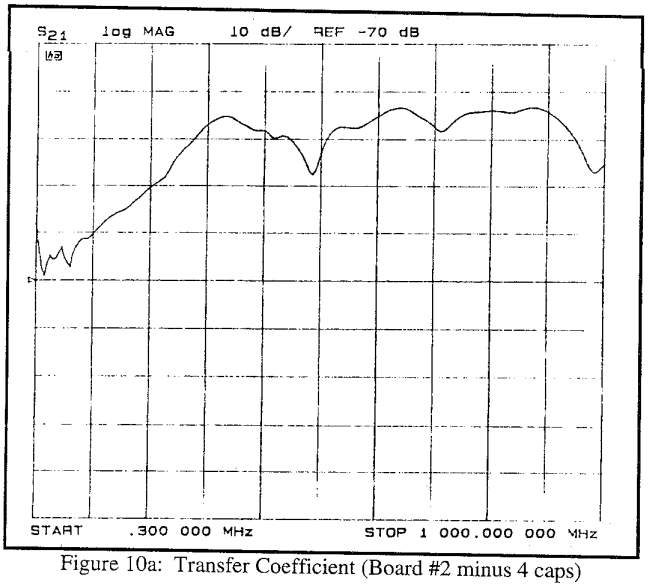

Figure 10a: Transfer Coefficient (Board #2 minus 4 caps)

so different from boards with a 10 mil spacing or boards without power planes? One explanation was first proposed in a 1994 Masters Thesis written by Mike Wilhelm at the University of Missouri-Rolla [2]. Mike was evaluating a scaled-up model of a multilayer printed circuit board made out of aluminum plates. He found that the measured results did not agree with the results predicted by radial transmission line models of the multilayer board.

In the scale model, all of the significant inductances were due to magnetic flux between the planes. He found that it was necessary to account for the *mutual inductance* between component current paths and decoupling capacitor current paths in order to obtain accurate results. For example, consider the component and decoupling capacitor mounted on the 4-layer board illustrated in Figure 6. Current drawn from the power plane by the active component can be supplied by the power/ground plane capacitance or it can come directly from the external decoupling capacitor. Current drawn from the power/ground plane capacitance flows in a loop (Loop A) indicated by the right diagonal lines. Note that this current loop shares a common loop area with a similar loop (Loop B), represented by left diagonal lines, linking the decoupling capacitor to the power/ground planes. The mutual inductance between Loop A and Loop B causes current to be drawn from the decoupling capacitor. Moving the decoupling capacitor closer to the active device increases the mutual inductance and increases the percentage of the current that is drawn from the decoupling capacitor.

Figure 7 shows a simple equivalent circuit that models this behavior. When the via inductance is large relative to the trace inductance, the transfer ratio of the two-port network increases at high frequencies and eventually levels off in much the same manner as the curves in Figure 3. Mutual inductance is not a factor in boards with closely spaced power and ground planes, because the magnetic flux between the planes is negligible compared to the flux coupling the traces used to attach component leads to the board. Unlike multilayer boards with closely spaced planes, the active components on boards with non-negligible mutual inductance draw most of their current from the nearest decoupling capacitors.

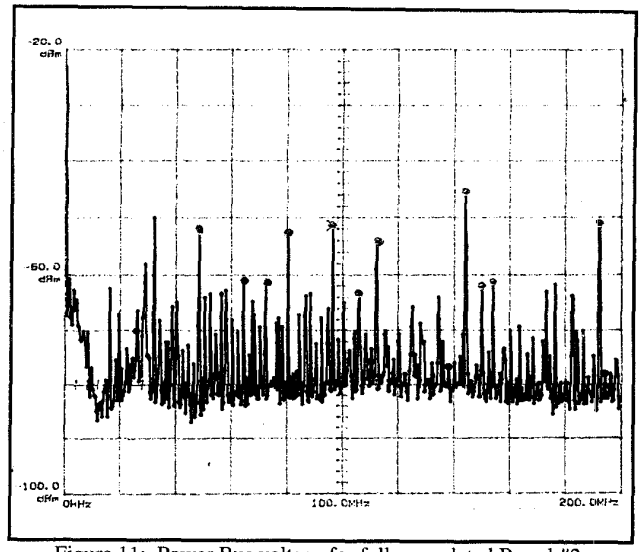

Figure 11: Power Bus voltage for fully populated Board #2

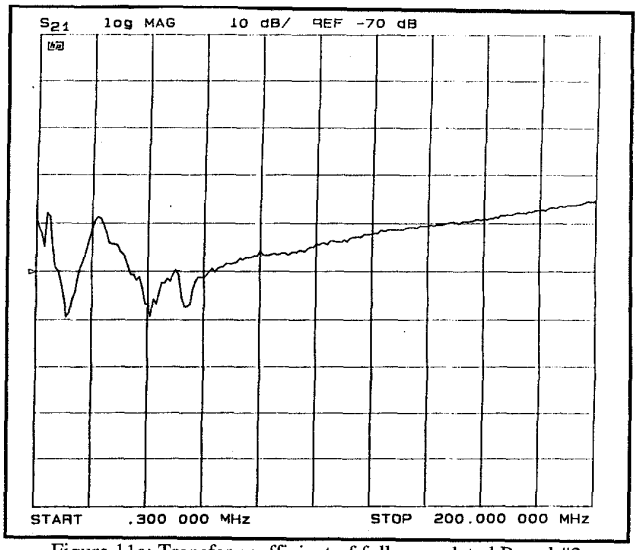

Figure 11a: Transfer coefficient of fully populated Board #2

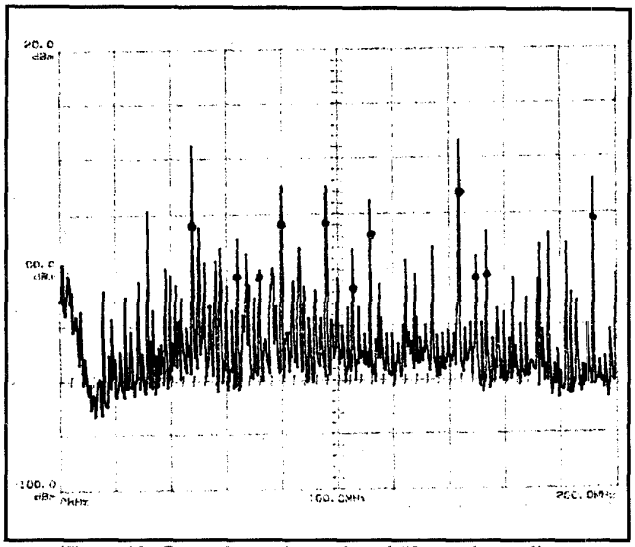

Figure 12: Power bus voltage (Board #2 - no decoupling)

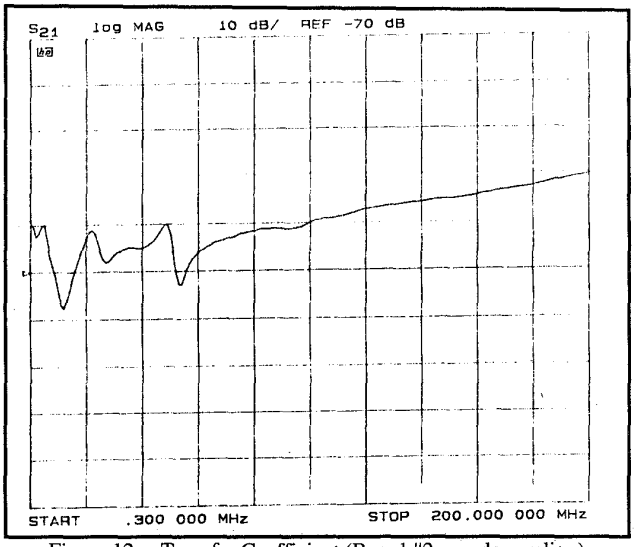

Figure 12a: Transfer Coefficient (Board #2 - no decoupling)

BOARD #1

The power layer in Board #1 contained both 3-volt and 5-volt planes. The probes were attached to the board at two locations relatively near to each other on the 5-volt plane. The lower curve in Figure 8 shows the measured transfer coefficient as a function of frequency for the fully populated board. Several 22 μF decoupling capacitors were then removed from the board and the board was re-measured. The 22 μF decoupling capacitors had no significant effect on the board response above approximately 2 MHz. Next, three high frequency decoupling capacitors (~10 nF) nearest the two probes were removed. The transfer coefficient, S_{21}, increased by 3-6 dB everywhere from 5 MHz to 1 GHz (Curve 2). Removing 5 more high frequency capacitors a little further from the probes increased the transfer ratio by another 5-6 dB between 5 MHz and 470 MHz and by a few dB up to 1 GHz (Curve 3). When the 12 remaining high frequency decoupling capacitors furthest from the probes were removed, the response was mostly unchanged increasing by 1-2 dB in some frequency bands (Curve 4).

BOARD #2

Board #2 was also a 4-layer PC motherboard with surface mount components. However it was designed and manufactured by a different company than Board #1. It employed different active components and a different overall decoupling strategy than Board #1. Probes were located at three positions on this board. Measurements of the power bus noise (active devices powered up) and S_{21} measurements were made. The most significant results are summarized below.

Figure 9 shows the voltage on the power bus measured at the first probe location while D.C. power was applied to the fully populated board. Figure 9a shows the corresponding transfer ratio measurement between the first and second probe locations without power applied. As individual high-frequency decoupling capacitors located near the first probe were removed, the measured noise voltage and the measured transfer coefficient increased slightly.

Figure 10 shows the voltage on the power bus measured at the first probe location after the 4 closest decoupling capacitors were removed. Figure 10a shows the measured transfer ratio between the first and

second probe locations. Note that both the noise voltage and the S_{21} measurement are increased by about 5 dB between approximately 100 and 500 MHz. Removing all of the remaining decoupling capacitors (14 of them) had little additional impact on either the noise spectrum or the transfer ratio.

Throughout all of the testing, it was observed that changes in the decoupling near a probe affected both the measured noise voltage at that probe and the measured transfer coefficient, S_{21}, similarly. Figures 11 and 11a show the noise voltage and the transfer coefficient of the fully populated board between 0.3 and 200 MHz. Figures 12 and 12a show the corresponding measurement for the board with all decoupling capacitors removed. The biggest change in the transfer ratio occurs around 45 MHz where there is a 10 dB increase. Note that the change in the measured power bus noise is also 10 dB at this frequency. Above approximately 60 MHz, both the power bus noise and the S_{21} measurement increase by about 5 dB.

OTHER RESULTS

Results of a few other measurements that were made as part of this study should be mentioned. Measurements of S_{21} were made on Board #3 both with and without D.C. power applied to the planes. D.C. blocks were inserted behind the probes in order to avoid damaging the network analyzer. Also the clock oscillator had to be removed from the board so that noise on the power bus wouldn't interfere with the measurement. Applying power to the active devices on Board #3 made no detectable difference in the measured value of S_{21}.

It should also be noted that several times during the testing, the positions of the source port and the measurement port were interchanged. In every case, the results were unchanged (i.e. $S_{21}=S_{12}$) satisfying reciprocity and indicating that there were no non-linearities affecting the measurement.

SUMMARY

The measured data presented above demonstrates that 4-layer boards with 40 mil spacing between the power and ground planes require a different decoupling model than boards with closely spaced power and ground planes. They are also unlike boards that do not have a power plane. The mutual inductance between active components and decoupling capacitors can force the active devices to draw most of their high frequency current from the nearest capacitor.

The data also demonstrated a good correlation between S_{21} measurements on unpowered boards and power bus noise on boards with the active devices powered up. This observation helps to verify the linear nature of the power bus impedance and justifies the common practice of modeling fully populated printed circuit boards with linear two-port networks.

ACKNOWLEDGMENT

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REFERENCES

[1] T. Hubing, J. Drewniak, T. Van Doren, and D. Hockanson, "Power Bus Decoupling on Multilayer Printed Circuit Boards," *IEEE Trans. on EMC*, vol. 37, no. 2, May 1995.

[2] M. Wilhelm, *Via Modeling and Lossy Media in the Power Bus Structure of Multilayer Printed Wiring Boards*, University of Missouri-Rolla Masters Thesis, 1994.