Quantifying SMT Decoupling Capacitor Placement in DC Power-Bus Design for Multilayer PCBs

Jun Fan, *Member, IEEE*, James L. Drewniak, *Senior Member, IEEE*, James L. Knighten, *Senior Member, IEEE*, Norman W. Smith, Antonio Orlandi, *Senior Member, IEEE*, Thomas P. Van Doren, *Senior Member, IEEE*, Todd H. Hubing, *Senior Member, IEEE*, and Richard E. DuBroff, *Senior Member, IEEE*

***Abstract*—Noise on a dc power bus that results from device switching, as well as other potential mechanisms, is a primary source of many signal integrity (SI) and electromagnetic interference (EMI) problems. Surface mount technology (SMT) decoupling capacitors are commonly used to mitigate this power-bus noise. A critical design issue associated with this common practice in high-speed digital designs is placement of the capacitors with respect to the integrated circuits (ICs). Local decoupling, namely, placing SMT capacitors in proximity to ICs, is investigated in this study. Multilayer PCB designs that employ entire layers or area fills for power and ground in a parallel plate structure are considered. The results demonstrate that local decoupling can provide high-frequency benefits for certain PCB geometries through mutual inductive coupling between closely spaced vias. The associated magnetic flux linkage is between the power and ground layers. Numerical modeling using an integral equation formulation with circuit extraction is used to quantify the local decoupling phenomenon. Local decoupling can effectively reduce high-frequency power-bus noise, though placing capacitors adjacent to ICs may limit routing flexibility, and tradeoffs need to be made based on design requirements. Design curves are generated as a function of power-bus layer thickness and SMT capacitor/IC spacing using the modeling approach to quantify the power-bus noise reduction for decoupling capacitors located adjacent to devices. Measurement data is provided to corroborate the modeling approach.**

***Index Terms*—DC power-bus design, decoupling capacitor location, high-speed digital design, local decoupling, mutual inductance, SMT decoupling capacitors.**

I. Introduction

CURRENT supply and return are commonly accomplished in high-speed digital designs with multilayer PCBs by a power-bus structure using two or more entire planes or large area fills as power and ground layers to achieve a very low impedance. The power-bus structure, however, is a good transmission-line, and noise generated by IC switching can be easily propagated throughout it, resulting in interference and radiation problems [1]–[4]. Surface mount technology (SMT) decoupling capacitors are commonly connected between the power and ground layers to mitigate the power-bus noise. From a frequency-domain perspective, the SMT capacitors may not always be effective at high frequencies [5]–[7]. The parasitic inductance associated with the interconnect (vias and traces) gradually dominates the SMT capacitance with increasing frequency, and the impedance at two terminals defined on the power/ground layers is solely determined by the power/ground layer itself. Consequently, it is typically proposed that decoupling capacitors are only effective below "their self resonant frequency," i.e., below the series resonance of the interconnect inductance and SMT capacitance value. The study presented herein shows that capacitors placed adjacent to IC devices can be effective even far beyond their series resonant frequency in certain circumstances. While practicing engineers have noted this in high-speed applications, no proven, and quantified design guidelines or curves have been established. This paper focuses on the impact of SMT decoupling capacitors on high-frequency power-bus noise in the frequency domain. It is well known in practice that noise on the dc power bus can lead to EMI and signal integrity problems.

Decoupling capacitor placement has been studied with both experimental [8]–[10] and modeling [11]–[13] approaches. Most schools of thought on dc power-bus design advocate some form of global bulk decoupling. A traditional view also advises the use of decoupling capacitors placed very close to individual integrated circuits [14]–[16]. The rationale for this approach may be rooted in early digital circuit designs where power supply and current return were achieved using traces, rather than entire planes. In this case, the locations of capacitors relative to the ICs determine the parasitic inductance associated with the traces, and thus determine the effective range of the capacitors. The closer a capacitor is placed adjacent to an IC, the smaller the parasitic inductance, and the higher the frequency at which the capacitor can supply charge, or equivalently decouple high-frequency noise. This idea is still used to advocate on-chip decoupling. Compared to the off-chip decoupling, the on-chip decoupling is more effective at higher frequencies due to the bond wire inductances [17]. Another study of SMT decoupling capacitors and printed circuit board power-bus design concluded that for printed circuit boards with entire power and ground planes, all decoupling capacitors are shared, or are global, in the frequency range over which they are effective; hence, the location of decoupling capacitor on the board is unimportant [8]. The effective frequency range of decoupling capacitors is limited by the interconnect inductance. In

Manuscript received November 22, 2000; revised August 7, 2001. This work was supported in part by NCR Corporation through the UMR EMC Consortium.

J. Fan was with the Electromagnetic Compatibility Laboratory, University of Missouri-Rolla, Rolla, MO USA. He is now with NCR Corporation, San Diego, CA 92127 USA.

J. L. Drewniak, T. P. Van Doren, T. H. Hubing, and R. E. DuBroff are with the Electromagnetic Compatibility Laboratory, University of Missouri-Rolla, Rolla, MO 65409 USA.

J. L. Knighten and N. W. Smith are with NCR Corporation, San Diego, CA 92127 USA.

A. Orlandi is with the University of L'Aquila, 67100 L'Aquila, Italy.

Publisher Item Identifier S 0018-9375(01)10020-7.

this case, the critical parasitic inductance is associated with the interconnects between the capacitors and power/ground layers, which are not a function of capacitor location relative to ICs. This study considered multilayer boards with closely spaced layers, and its conclusions had been extended beyond the region of validity of the study. Other experimental investigations have shown that the location of SMT decoupling capacitors relative to an IC can impact the capacitor effectiveness over frequency for certain PCB layer stackups [9], [18].

The effectiveness of SMT decoupling capacitors placed in proximity to an IC is treated herein. The phenomenon was investigated with a numerical electromagnetic modeling method supported by measurements. It can be accounted for by mutual inductive coupling between closely spaced vias of the IC and SMT decoupling capacitor [9]. This mutual inductance works as a current divider over a frequency range beyond the normal "series resonant frequency," and less noise current is injected onto the power bus, resulting in a lower power-bus noise voltage. The associated magnetic flux linkage is between the power and ground layers. Placing capacitors adjacent to switching sources and susceptible devices is denoted local decoupling herein, and global decoupling denotes placing capacitors away from those devices. Local decoupling capacitors were found to be still effective at high frequencies, when all other global capacitors were ineffective.

A circuit extraction approach based on a mixed-potential integral equation formulation, denoted CEMPIE, was used to study the local decoupling effect. CEMPIE is an PEEC-type modeling tool suitable and effective for dc power-bus modeling [19]–[21]. It can handle most commonly used power-bus structures, including an arbitray multilayer medium, arbitrarily shaped power planes, SMT decoupling capacitors, test fixtures, and so on. The formulation and circuit extraction approach of CEMPIE are overviewed in Section II, as well as comparisons between modeling and measurements. Then, the concept of mutual inductance and CEMPIE modeling are presented in Section III, and design curves for decoupling capacitor location are discussed in Section IV.

II. Modeling Approach

Full-wave electromagnetic modeling approaches such as MoM, FEM, and FDTD can be used for dc power-bus modeling [22], [23]. However, a circuit type of simulation is, more often, desirable for PCB-related signal integrity (SI) and electromagnetic interference (EMI) modeling [24]–[26], since it is very compatible with digital device and transmission line models. The CEMPIE approach is a dc power-bus modeling method with circuit extraction, and is an application of the partial element equivalent circuit (PEEC) approach for general multilayer dielectric media [27], [28]. Layered media Green's functions are used rather than the free-space Green's function. The CEMPIE approach is robust, with the accuracy for capturing the distributed behavior of the power/ground planes, while being compatible with SPICE. It is very suitable for dc power-bus modeling, since device, transmission line, and other models can be incorporated.

The CEMPIE formulation is based on a mixed-potential integral equation. A comprehensive treatment can be found in [19]. An overview is given here for convenience. A typical dc power-bus has two types of metallization surfaces—planar layers such as power and ground planes, and vertical via interconnects and connector surfaces, as shown in Fig. 1. The dielectric layers, as well as the ground plane, are assumed to have infinite horizontal dimensions, and Green's functions for the grounded dielectric slab are calculated. Similar to the formulation of a classical scattering problem with an incident electric field, surface currents $\vec{J}$ and charges q are induced on all the metallization surfaces. Boundary conditions must be satisfied on these metallization surfaces excluding the ground plane since it has already been accounted for in the Green's functions. Non-PEC (perfect electric conductor) boundary conditions can be used in order to introduce the conductor losses. An electric field integral equation results as [19], [21]

$$\hat{n}\times\left[j\omega\int_{S1+S2}\bar{\bar{G}}^{A}(\vec{r},\vec{r}')\cdot\vec{J}(\vec{r}')ds'+\nabla\phi(\vec{r})\right]=Z_{\rm s}\hat{n}\times\vec{J}(\vec{r}),\quad \vec{r}\in S1\cup S2 \tag{1}$$

where

- ϕ induced scalar electric potential;
- $S1$ horizontal planes of concern (power areas);
- $S2$ vertical surfaces of device vias and ports, as shown in Fig. 1;
- $Z_{\rm s}$ surface impedance of conductors.

Conductor losses are included and characterized by the right-hand side (RHS) in (1). At dc and low frequencies where the skin depth is greater than the conductor thickness, the surface resistance $R_{\rm s}$ is constant, and

$$R_{\rm s}=\frac{1}{\sigma\cdot h} \tag{2}$$

where σ is the conductivity of conductor structures, and h is the thickness of power planes or via walls. However, when the frequency reaches the point where skin depth is smaller than conductor thickness, the surface impedance increases with the square-root of frequency as [29]

$$Z_{\rm s,skin}=(1+j)\sqrt{\frac{\pi f\mu_0}{\sigma}}. \tag{3}$$

Representing the surface impedance as

$$Z_{\rm s}=R_{\rm s}+Z_{\rm s,skin} \tag{4}$$

enables the characterization of both low-frequency and high-frequency conductor-loss behaviors.

Equation (1) is then expanded using basis functions, and tested by testing functions that are the same as the basis functions. A matrix equation results as [19]

$$([\mathbf{R}]+j\omega[\mathbf{L}])[\mathbf{i}]-[\mathbf{\Lambda}][\boldsymbol{\phi}]=0 \tag{5}$$

where

- $[\mathbf{i}]$ unknown edge-current vector;
- $[\boldsymbol{\phi}]$ unknown vector of cell potentials;

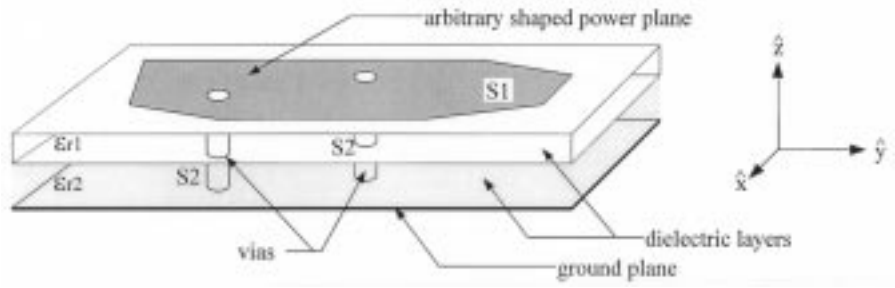

Fig. 1. A power-bus structure with vertical interconnects.

- $[\mathbf{\Lambda}]$ connectivity matrix that relates cell quantities to edge quantities;
- $[\mathbf{L}]$ *branch-wise inductance* matrix, due to its coefficient $j\omega$, and the relationship between current and voltage.

The elements of the $[\mathbf{L}]$ matrix are

$$L_{\alpha\gamma} \equiv \frac{1}{l_\alpha l_\gamma} \left\langle \vec{f}_\alpha, \quad \int_{S_\gamma} \bar{\bar{G}}^A(\vec{r},\vec{r}') \cdot \vec{f}_\gamma ds' \right\rangle \tag{6}$$

where $\vec{f}_\alpha$ and $\vec{f}_\gamma$ are the testing and basis functions, respectively; and, l_α and l_γ are the lengths of the edges where the testing and basis functions are anchored. The resistance matrix $[\mathbf{R}]$ has elements

$$R_{\alpha\gamma} = \frac{Z_s}{l_\alpha l_\gamma} \left\langle \vec{f}_\alpha, \vec{f}_\gamma \right\rangle. \tag{7}$$

The current continuity provides a relationship between charge and current as

$$-j\omega [\mathbf{Q}] = [\mathbf{I}] + [\mathbf{I}^e] \tag{8}$$

where nodal currents are defined as total currents flowing out of the corresponding mesh cells, and Q_n, I_n, and I_n^e are the charge, the nodal current, and the externally impressed nodal current associated with Cell n, respectively. The nodal currents I are related to the edge currents i by the connectivity matrix as

$$[\mathbf{I}] = [\mathbf{\Lambda}^{\mathrm{T}}][\mathbf{i}]. \tag{9}$$

The unknown cell potentials are related to cell charges as [19]

$$[\boldsymbol{\phi}] = [\mathbf{K}][\mathbf{Q}] \tag{10}$$

where

$$K_{pq} = \frac{1}{A_p A_q} \int_{S_p} \int_{S_q} G^\phi(\vec{r},\vec{r}') ds' ds \tag{11}$$

where S_p and S_q surface integration over Cells p and q, respectively; and A_p and A_q corresponding cell areas; G^ϕ Green's function for scalar potential. It is a function of material permittivities, which are complex numbers if dielectric losses are included. Then

$$[\mathbf{K}^{-1}] = [\mathbf{C}] - j[\mathbf{G_d}] \tag{12}$$

where the $[\mathbf{C}]$ and $[\mathbf{G_d}]$ matrices are both real. Due to the relationship between potential and charge, $[\mathbf{C}]$ is denoted the *cell-wise capacitance* matrix, and $\omega[\mathbf{G_d}]$ is the *cell-wise conductance* matrix that results from the dielectric losses. Using

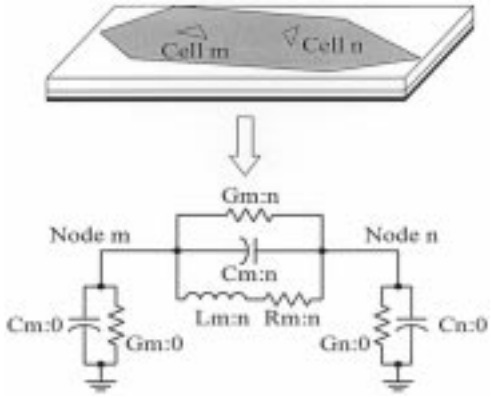

Fig. 2. The equivalent circuit model between any arbitrary pair of two nodes m and n.

(5), (8)–(10) and (12), a discretized form of the mixed-potential integral equation results as

$$\begin{bmatrix} \omega\mathbf{G_d} + j\omega\mathbf{C} & \mathbf{\Lambda}^{\mathrm{T}} \\ -\mathbf{\Lambda} & \mathbf{R} + j\omega\mathbf{L} \end{bmatrix} \begin{bmatrix} \boldsymbol{\phi} \\ \mathbf{i} \end{bmatrix} = \begin{bmatrix} -\mathbf{I}^e \\ 0 \end{bmatrix}. \tag{13}$$

A relationship between the node (cell) potentials and only the impressed nodal currents can be derived from (13) as

$$[\mathbf{Y}][\boldsymbol{\phi}] = [-\mathbf{I}^e], \tag{14}$$

where the $[\mathbf{Y}]$ matrix is denoted the *nodal admittance matrix* of the system, and

$$[\mathbf{Y}] = \left[\mathbf{\Lambda}^{\mathrm{T}}(\mathbf{R} + j\omega\mathbf{L})^{-1}\mathbf{\Lambda}\right] + \omega[\mathbf{G_d}] + j\omega[\mathbf{C}]. \tag{15}$$

The CEMPIE formulation differs from a classical MoM approach by not directly solving the matrix equation. Rather, it extracts an equivalent circuit model from the admittance matrix, by enforcing Kirchoff's Current Law (KCL) at every cell (node) [21]. The extracted circuit model is an $\{L, C, R, G\}$ network where R and G are used to include conductor and dielectric losses, respectively, and thus, are frequency-dependent. Fig. 2 shows the extracted circuit between any two arbitray circuit nodes that correspond to two mesh cells. This extracted circuit is SPICE compatible, and simulations are performed in a SPICE environment.

One of the advantages of the CEMPIE approach is its interface with SPICE. The power-bus structure, including the power and ground planes as well as vias and connectors, can be modeled using the first principles formulation (formulation based on Maxwell's equations), and an equivalent circuit extracted. The

digital circuits and components can be incorporated into the extracted circuit as lumped elements, or SPICE models. Circuit nets can be included with transmission-line models. SPICE is a mature circuit simulation tool with many well-developed IC, source, load, and transmission line models, and the power-bus can be modeled in an integrated fashion with the rest of the circuit design.

The extracted circuit element values are related to the Green's functions, which are frequency-dependent. In order to keep most of the circuit elements frequency-independent (some elements related to losses are frequency-dependent due to the loss characterization), a quasistatic approximation is applied to the Green's functions. The frequency independence of most of the circuit elements enables the frequency-domain modeling using CEMPIE to be much faster than a traditional MoM approach. Further, the extracted circuit can be used for many different "what-if" simulations. However, this quasistatic approximation can impose a stricter meshing requirement, requiring a finer mesh [21].

The frequency-dependent resistances that are used to account for the skin-effect losses in the extracted circuit lengthen the frequency-domain simulations. It is demonstrated by comparison with measurements, that, for power/ground layers with a separation of 10 mils or greater, the dielectric losses are dominant, and the skin-effect losses are negligible. Consequently, skin-effect losses are not included in the CEMPIE modeling for all the modeling examples presented below.

Previous measurements have already demonstrated that the CEMPIE approach is very effective for typical dc power-bus modeling [19], including a test board with numerous decoupling capacitors uniformly distributed over the PCB [20]. In this decoupling capacitor placement study, the SMT decoupling capacitor location relative to an IC is particularly important. To demonstrate the capability of the CEMPIE approach for handling this issue as well, two test geometries were modeled, and compared with measured results. Although Z_{21} between two terminals defined on the power/ground layers is the critical parameter that relates the output noise voltage with an input noise current, the input impedance looking into one port is more meaningful and exacting for modeling/measurement comparisons. Both transmitted and evanescent waves in the vicinity of the feed must be modeled correctly to achieve a correct input impedance result, while, for Z_{21}, the evanescent waves may not be as important. The input impedance looking into the test port was then investigated for two similar test boards with the geometry shown in Fig. 3. Both were two-layer PCBs with top and bottom layers representing power and ground planes, respectively. The dielectric material was FR-4 with a dielectric constant of $\epsilon_r = 4.7$, and loss tangent of $\tan\delta = 0.02$. One SMT decoupling capacitor was added to each board with one end directly soldered to the power plane, and the other end connected to the ground plane through a via. The locations of the capacitors were different for the two test boards. The spacing between the input port and the capacitor via for one board was 5 mm, while it was 50 mm for the other board. The power plane, the SMA test port via, and the capacitor via were modeled with the first principles formulation for each board, and SMT capacitors were incorporated into the CEMPIE extracted circuit using lumped series $\{L, C, R\}$ elements whose values were measured using an HP4291A Impedance Analyzer with an SMT test fixture. The values of the $\{L, C, R\}$ elements for the capacitor on board 1 were 1.57 nH, 8.14 nF, and 666 mΩ, respectively, and the corresponding values for the capacitor on board 2 were 1.57 nH, 8.62 nF, and 441 mΩ. Both boards were modeled from 1 MHz to 2 GHz. Comparisons between the modeling and measurements are shown in Figs. 4 and 5. The input impedance was measured with the HP4291A Impedance Analyzer (1 MHz–1.8 GHz). The CEMPIE modeled results agree favorably with the measurements for both cases over the entire frequency range from 1 MHz to 1.8 GHz.

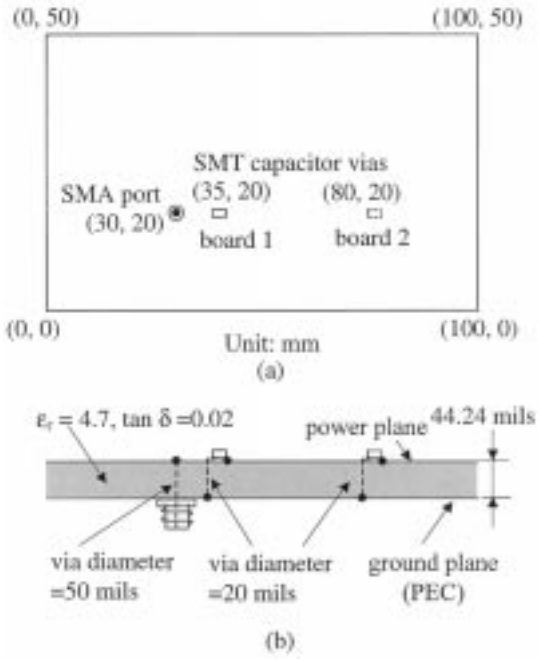

Fig. 3. DC power-bus test geometries with an SMT decoupling capacitor located either closely or remotely from the input port.

III. Physics of Global Versus Local Decoupling

A global decoupling capacitor is located remotely from an IC, and effectively reduces power-bus noise in a certain frequency band. An equivalent circuit model for the global decoupling is shown in Fig. 6, where an IC source is modeled as an ideal current source, L_1 and $L_{\rm d}$ are the interconnect inductances associated with the IC and a global decoupling capacitor, respectively, $C_{\rm d}$ is the capacitance of the global decoupling capacitor, and all other power-bus structures are characterized as a $[Z']$ network that will in general be distributed. The noise voltage at the output Port 2 due to the IC source at the input Port 1 is affected by the ratio of $j\omega L_{\rm d} + (1/j\omega C_{\rm d})$ to Z'_{11}. At the frequencies where $j\omega L_{\rm d} + (1/j\omega C_{\rm d}) \gg Z'_{11}$, the noise current generated by the IC is inadequately bypassed by the global decoupling capacitor, in other words, the global decoupling capacitor is ineffective. Since $L_{\rm d}$ and $C_{\rm d}$ are in series, the series resonant frequency provides a rough estimate of the effective frequency range for the global decoupling capacitor. The inductance $L_{\rm d}$ dominates the total series impedance and makes it increase at a

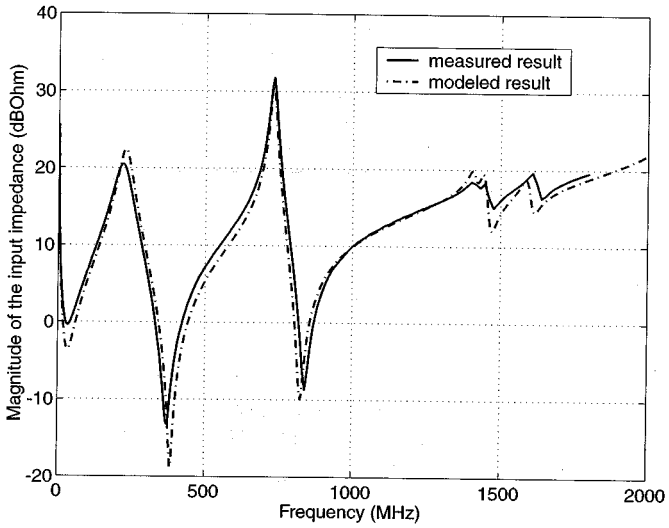

Fig. 4. Comparison between the modeled and measured results for the dc power-bus geometry shown in Fig. 3 with a closely spaced capacitor.

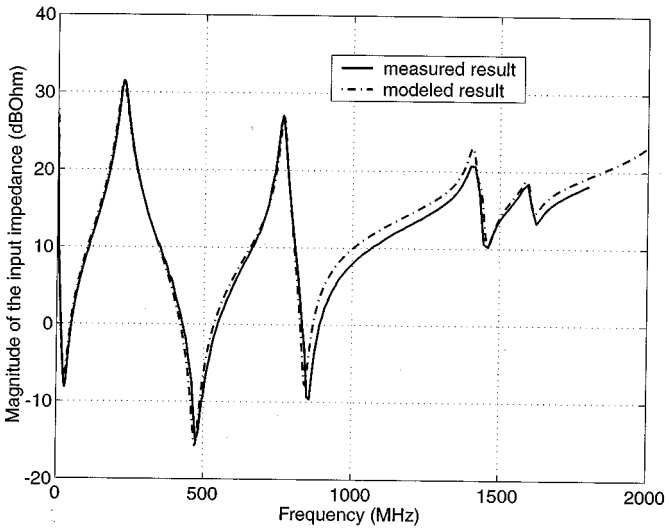

Fig. 5. Comparison between the modeled and measured results for the dc power-bus geometry shown in Fig. 3 with a remotely spaced capacitor.

rate of 20 dB/dec, when the frequency is beyond the series resonant frequency. A local decoupling capacitor closely spaced to an IC, on the other hand, can be tightly coupled to the power or ground pin of the IC as a result of mutual inductance between the vias of the IC and decoupling capacitor [9], [18]. The flux linkage between the two vias enables the local decoupling capacitor to be effective far beyond its series resonant frequency. This mutual inductance results from magnetic flux linkage between the power and ground planes due to currents on the vias sharing a common area, as shown in Fig. 7. When there is a current draw from the active device, the decoupling capacitor can provide charge, acting as a local source. These currents, flowing through the vias between the power and ground layers, generate magnetic flux between the layers. There is a common area of magnetic flux linkage from the vias to the edge of the board. This mutual flux determines the mutual inductance between the two vias, and the effectiveness of a decoupling capacitor closely

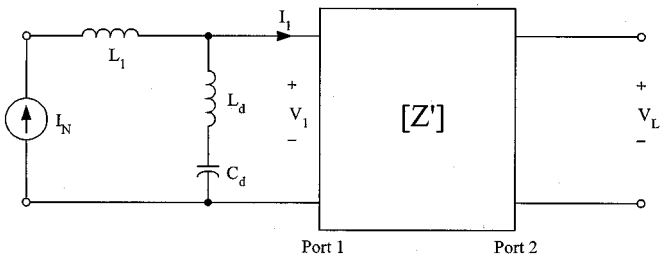

Fig. 6. Hybrid lumped/distributed model for a power-bus structure with a global decoupling capacitor.

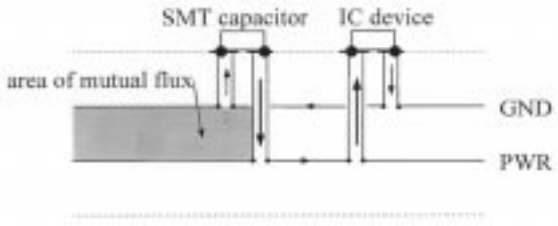

Fig. 7. Vias associated with a decoupling capacitor near an IC produce a region of shared magnetic flux and a mutual inductance.

spaced to an IC. Since the flux linkage is due to the via portions between the power and ground planes, the vias across the power/ground layer should be placed in proximity to obtain sufficient coupling. In the case illustrated in Fig. 7, these vias extend to the power plane. The mutual inductance is a function of the IC/decoupling capacitor spacing, spacing of the power and ground layers in the layer stackup, and the proximity of the IC/decoupling capacitor pair to the PCB edge.

The CEMPIE approach was used to study the local decoupling effect, since all vertical vias, as well as planar structures, can be included in the first principles formulation. The modeling approach provides a straight-forward means of performing various what-if scenarios. Modeling results can be generated, and, thus, design guidelines can be developed for similar applications. A 6×9-inch two-layer PCB power-bus structure was modeled using the CEMPIE approach. Power and ground were modeled as two solid planes. The dielectric layer had a dielectric constant of $\epsilon_r = 4.7$, and loss tangent of $\tan\delta = 0.02$. As shown in Fig. 8, 39 SMT decoupling capacitors were uniformly distributed over the board on a 1-inch-grid for global decoupling. Adjacent to the input port either one or four local decoupling capacitors were placed. All SMT decoupling capacitors were modeled with individual values of 0.01 μF, and the parasitic inductance and resistance values for the capacitor package used in the modeling were 820 pH and 120 mΩ, respectively. One end of each capacitor was modeled as a direct connection to the ground plane. The other end was modeled as a via connected to the power plane. The SMT capacitors were modeled as lumped elements, and the via interconnects were modeled in the first principles formulation. The input port was located on the board with a spacing from the left and bottom edges equal to 2 inches, as shown in Fig. 8. This port location was chosen to avoid symmetry planes and certain board resonant locations, so that all modes of the parallel planes were excited. All capacitor vias, as well as the input port, had diameters of 30 mils. Five ideal open-circuited probes were set as output ports,

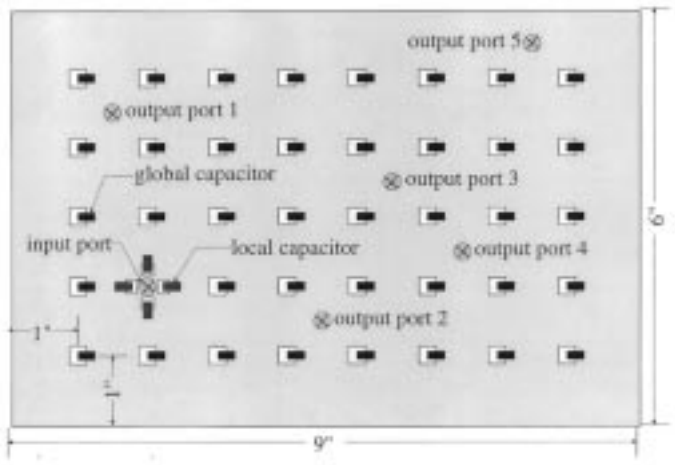

Fig. 8. Modeling structure for the local decoupling study.

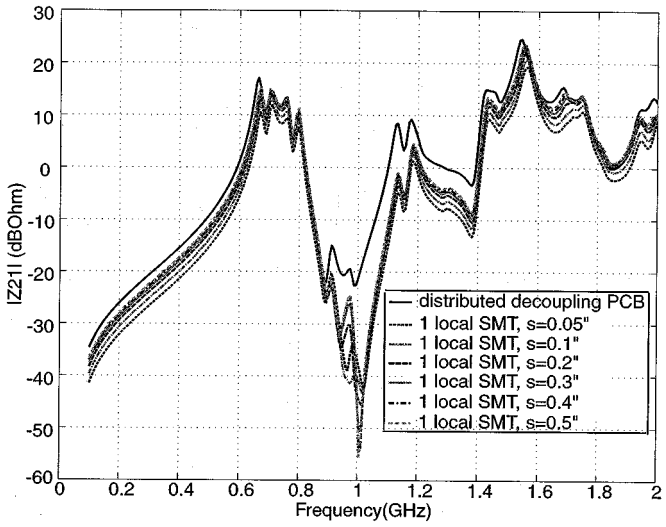

Fig. 9. Modeled results for a 44-mil-thick PCB with one local decoupling capacitor.

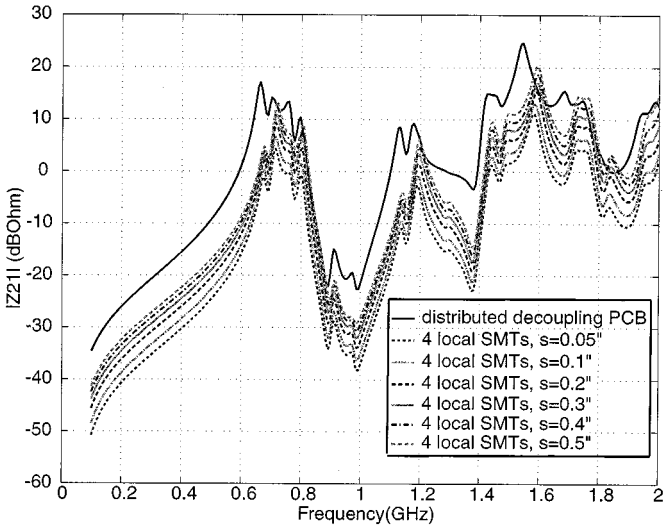

Fig. 10. Modeled results for a 44-mil-thick PCB with four local decoupling capacitors.

and an average response calculated to avoid nongeneral cases. The placement of these output probes was selected such that the peak and null locations of the low-order board resonances (within the frequency band of interest) could be avoided, and major board areas were roughly represented. For the four local decoupling capacitor case, all four capacitors were located on a circle centered at the input port. This case with four symmetrically located decoupling capacitors was studied as an approximate upper bound of the noise mitigation that could be expected with local decoupling. The spacing between the local capacitors and the input port, as well as the board thickness, varied, and the effect of the local decoupling compared with the case without local decoupling was quantified. The global decoupling capacitors were always included throughout the entire study.

The $|Z_{21}|$ between input and output ports was calculated from the modeling. A larger Z_{21} magnitude indicates more noise is transferred from the effective current source at Port 1 to the output at Port 2. Fig. 9 shows the modeled $|Z_{21}|$ results for the PCB structure shown in Fig. 8 between the input port and output port 1. The thickness of the board was 44 mils, and one local decoupling capacitor was present. The local decoupling is compared in Fig. 9 with the case of only uniformly distributed global decoupling. The cases with four local decoupling capacitors (also between the input port and output port 1) are shown in Fig. 10. The parameter s in both figures denotes the spacing between the input port and the local decoupling capacitor vias. These two figures indicate that the local decoupling did exhibit lower magnitudes than the case without local decoupling, and the decrease in magnitude was approximately frequency-independent over the entire frequency range from 100 MHz to 2 GHz. The $|Z_{21}|$ also decreased with decreased spacing between the local decoupling capacitor(s) and the input port. Further, the number of the local decoupling capacitors greatly impacted the local effect, due to the mutual inductive coupling between multiple vias being much stronger than the coupling between two vias.

As discussed previously, the local decoupling effect results from the mutual inductance between two closely spaced vias. A hybrid lumped/distributed model for the PCB structure shown in Fig. 8 can be constructed as shown in Fig. 11(a). In the model, L_1 is the self inductance of the via associated with the input port, and L_2 is the portion of the self inductance of the via between the planes associated with the local decoupling capacitor adjacent to the input port, L_3 is the remaining inductance of the interconnect to the capacitor package and its parasitics, M is the mutual inductance between the two vias associated with the flux linkage between the planes, and $C_{\rm d}$ is the value of the local decoupling capacitor. The $[Z']$ network embodies the remaining PCB behavior, lumped and distributed, including the 39 global decoupling capacitors. Only one local decoupling capacitor is assumed for the present discussion. At the high frequencies of interest, the impedance of the SMT capacitor is dominated by the interconnect inductance rather than capacitance, and the $1/\omega C_{\rm d}$ impedance is negligible relative to the inductive impedance. The mutual inductance can be transformed to a T-network, and the equivalent circuit shown in Fig. 11(b) results. The input port is connected to an ideal current source I_N

(the injected noise current), and the output port is an open-circuited pair of terminals with a voltage V_L. The Z_{21} between the input and output ports is expressed with I_N and V_L as

$$Z_{21} = \frac{V_L}{I_N}. \tag{16}$$

If the current flowing into Port 1 of the $[Z']$ network is designated as I_1 as shown in Fig. 11(b), the voltages V_1 and V_L can be obtained from the definition of Z-parameters as

$$V_1 = Z'_{11} I_1 \tag{17}$$

$$V_L = Z'_{21} I_1 \tag{18}$$

where Z'_{11} and Z'_{21} are the parameters of the two-port $[Z']$ network. Further, I_1 is related to I_N as

$$I_1 + \frac{V_1 + j\omega M I_1}{j\omega(L_2 + L_3 - M)} = I_N. \tag{19}$$

Substituting (17) into (19) gives

$$I_1 = \frac{j\omega(L_2 + L_3 - M)}{j\omega(L_2 + L_3) + Z'_{11}} I_N. \tag{20}$$

Then, using (16), (18), and (20), the Z_{21} of the total PCB structure that relates V_L to I_N is

$$Z_{21} = \frac{j\omega(L_2 + L_3 - M)}{j\omega(L_2 + L_3) + Z'_{11}} Z'_{21}. \tag{21}$$

In (21), Z'_{11} is the distributed self impedance of the $[Z']$ network for the power-bus structure, when the output port is open. If Z'_{11} is smaller than $\omega(L_2 + L_3)$, the $|Z_{21}|$ change (in dB) due to the mutual inductance is approximately frequency independent as is the case illustrated in Figs. 9 and 10. In general, at high frequencies, the magnitude of the impedance of a power-bus is lower than that of an SMT capacitor interconnect $\omega(L_2 + L_3)$. Then, the mutual inductance is working as a current divider at these high frequencies. For a noise current generated at the input port, only a portion of it can be transfered to the output port due to the mutual inductance, thus resulting in a smaller noise voltage at the output port. The change of the $|Z_{21}|$ (in dB) is determined by the value of this mutual inductance, rather than frequency. For a fixed board thickness, the closer the local capacitor is placed, the larger the mutual inductance, and the lower the Z_{21} magnitude.

If the closely spaced vias for the IC/capacitor pair have the same diameters, then

$$M \approx kL_2 \tag{22}$$

where k is the coupling coefficient. Using (22) in (21), and assuming $|Z'_{11}| \ll \omega(L_2 + L_3)$, then

$$Z_{21} \approx \frac{L_2(1-k) + L_3}{L_2 + L_3} Z'_{21}. \tag{23}$$

L_3 is the portion of the SMT inductance due to the via and interconnect above the power/ground layer that connects to the capacitor package, and can be significant for a PCB with many layers or interior power/ground layers. When L_3 is considerably greater than L_2, the noise mitigation benefits of local decoupling is negligible. In other words, minimum interconnect inductance above the power/ground plane pair (eliminating traces between the via and bonding pads, small package parasitics, etc.) is still required to achieve the potential local decoupling benefits. Equation (23) also indicates that a thinner power/ground plane pair will have less significant local decoupling effects because of a smaller L_2 value. The focus in this paper is the case where L_2 is dominant.

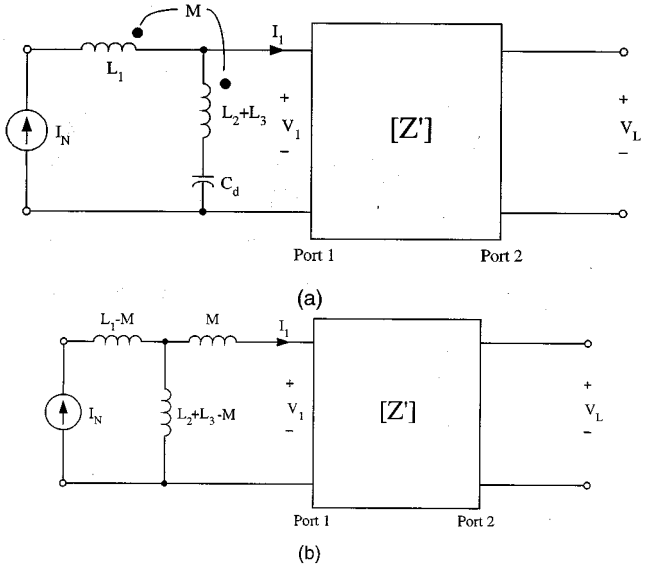

Fig. 11. (a) Hybrid lumped/distributed model for the power-bus structure shown in Fig. 8. (b) Equivalent circuit at high frequencies.

Equation (23) is based on the assumption that $|Z'_{11}|$ is smaller than $\omega(L_2 + L_3)$. To check this assumption, the test geometry shown in Fig. 8 without the local decoupling capacitors and the input port was modeled using the CEMPIE approach. L_1 and L_2 for the vias with a radius of 15 mils are approximately 1.35 nH for a 44-mil layer thickness, based on our experimental experience. L_3 was 0.82 nH in the modeling discussed previously. Then, $|Z'_{11}|$, the magnitude of the input impedance looking into the center of the local capacitor/input port pair when no vertical vias associated with the pair were present, was calculated, and is compared with $\omega(L_2 + L_3)$ in Fig. 12. At most frequencies of interest, $|Z'_{11}|$ is significantly less than $\omega(L_2 + L_3)$ except at some resonant peaks. The $|Z'_{11}|$ peaks render errors when using (23) at the corresponding frequencies. However, since an overall performance of local decoupling in a broad frequency band is of interest, rather than that at some specific frequencies, (23) is still valid for estimating the average $|Z_{21}|$ change. The imperfect frequency independence of the $|Z_{21}|$ change shown in Figs. 9 and 10 can be attributed to the frequency-dependent behavior of $|Z'_{11}|$, possibly as well as small frequency dependence of k.

IV. Design Curves

The $|Z_{21}|$ decrease (in dB) due to local decoupling is approximately frequency-independent in the frequency range of interest from 100 MHz to 2 GHz. Therefore, an average magnitude difference with regard to a baseline case, without local decoupling, over all the frequency points can be used to quantify the local decoupling effect. This average was also taken over

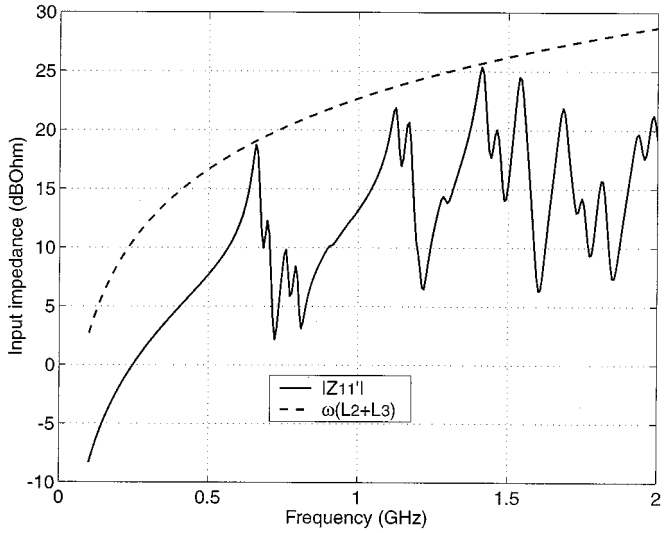

Fig. 12. Comparison of $|Z'_{11}|$ and $\omega(L_2 + L_3)$.

the five output ports shown in Fig. 8. Equation (23) indicates that changes in $|Z_{21}|$ due to local decoupling are relatively independent of the output port location. This conclusion has been corroborated with modeling results. The simple averaging technique used here relates a value of noise voltage decrease on the power/ground plane pair for a given noise current to the SMT decoupling capacitor location. It thus provides a feasible way of quantifying the noise mitigation effects of local decoupling based on geometrical parameters. Several cases with different spacing between the input port and local decoupling capacitors, as well as different layer spacings between the power and ground planes, were considered with the CEMPIE modeling. The average $|Z_{21}|$ difference (in dB) was calculated, and design curves based on these results were generated. These curves can be used to quatify the noise mitigation effects of local decoupling for a given power-bus geometry, and to weigh compromises between the benefits from local decoupling and the consequent impact on routing flexibility near IC chips.

Both self and mutual inductances are functions of via radius and board size, however, the variation of the inductance values is negligible when the ratio of the board size to the via radius is sufficiently large [30]. This is the case for the geometries modeled herein for the purpose of developing design curves, as well as most practical PCB designs. The inductance value varies with respect to via location on the PCB as well. However this change is insignificant in most of the board region except for the small areas in proximity to board edges [31]. Further, the ratio of the inductances, rather than the inductance values, determines the $|Z_{21}|$ decrease as seen in (23), which renders the inductance value change less significant. A via inductance extraction procedure was used to verify this. The self and mutual inductances associated with vias between power and ground planes was calculated with this procedure [30], [32]. Thus, the $|Z_{21}|$ decrease in dB can also be estimated using (21) by calculating L_2 and M directly, with the Z'_{11} assumed to be zero. Different input port/local decoupling pair locations were studied using this via inductance extraction procedure, and all calculated $|Z_{21}|$ decrease values were within 1 dB of the rigorous modeling presented in this paper. Therefore, the results obtained from the board geometry of Fig. 8 should provide a good estimate of the local decoupling effect for general DC power-bus designs. The limiting factor in determining the $|Z_{21}|$ reduction resulting from the mutual inductance between IC and SMT decoupling capacitor vias is L_3, the portion of the package and interconnect inductance excluding the via between the power and ground layers. The value of L_3 was set to a small number (820 pH, a typical value of package parasitic inductance) in this paper, since the objective was to quantify the maximum benefit that can be achieved by employing decoupling capacitors in proximity to ICs. In practice, a larger L_3 is often the case since it also includes the portion of the vias above the power/ground plane pair and any other interconnect parasitics (such as a trace length) to the SMT capacitor package. The benefits of local decoupling due to mutual inductance from magnetic flux linkage of vias between the planes is compromised by these parasitic effects. The derived curves are then approximate upper bounds that can be used for decoupling design, and assessing the potential benefits of a capacitor located close to an IC.

The average $|Z_{21}|$ decrease due to local decoupling versus the spacing between the local decoupling and the input port is shown in Fig. 13 for five different power/ground layer thicknesses. Three curves with the layer spacing of 30, 44, and 60 mils were calculated from the test geometry shown in Fig. 8. The modeled board material was FR-4 with a dielectric constant of $\epsilon_r = 4.7$, and loss tangent of $\tan\delta = 0.02$. However, a smaller PCB with dimensions of 4×7 inches, shown in Fig. 14, was also modeled to generate the other two $|Z_{21}|$-decrease curves with layer spacings of 10 and 20 mils, due to the increased computational burdon imposed by the thinner layers. A denser mesh is needed for a thinner layer, as required by the quasistatic approximation of the Green's functions applied in the CEMPIE formulation [21]. The board material for the two PCBs was identical. Although five curves were generated from two different test geometrices, they are plotted on a single graph, to facilitate direct comparison. As discussed previously, if $|Z'_{11}|$ is less than $\omega(L_2 + L_3)$, the $|Z_{21}|$ difference (in dB) is approximately only a function of L_2, L_3, and M, which does not change significantly with different board sizes. This will be demonstrated.

For all five cases, both one and four local decoupling capacitor(s) on the board were considered. The four local capacitors were symmetrically located on a circle centered at the input port. In practical designs, it may not be possible to place capacitors around an IC pin. Therefore, the modeled results, again, give an approximate upper bound on the benefit that can be achieved with local decoupling capacitors. The numerical value of each data point is an average of the $|Z_{21}|$ decrease over the entire frequency band from 100 MHz to 2 GHz, and over the five output ports as well. From Fig. 13, it is clear that the noise mitigation effect of local decoupling is greater in a thicker power layer, and that multiple local capacitors greatly enhance the decoupling effect. In the design phase, when the minimal spacing between a local SMT decoupling capacitor and an IC chip is determined after careful evaluation of other important issues such as routing flexibility, PCB manufacturing, component assembly, etc., the reduction of power-bus noise with the local decoupling can be

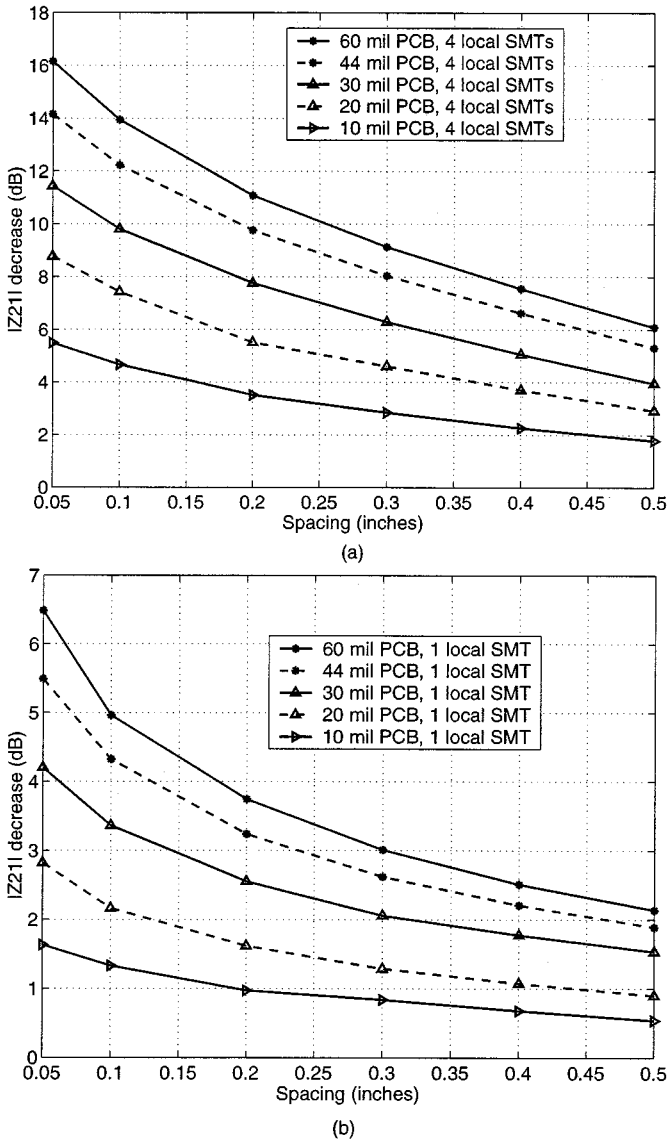

Fig. 13. Decrease in $|Z_{21}|$ versus spacing between the local decoupling and the input port. (a) Four local SMT decoupling capacitors. (b) One local SMT decoupling capacitor.

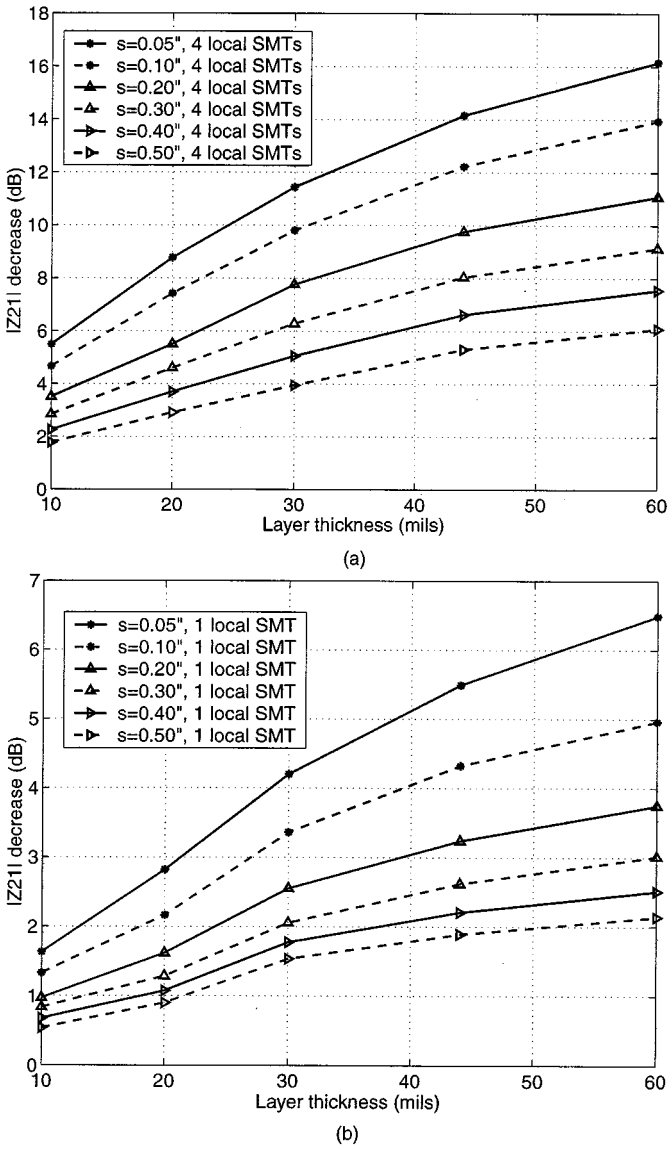

Fig. 15. Decrease in $|Z_{21}|$ versus power/ground layer thickness. (a) Four local SMT decoupling capacitors. (b) One local SMT decoupling capacitor.

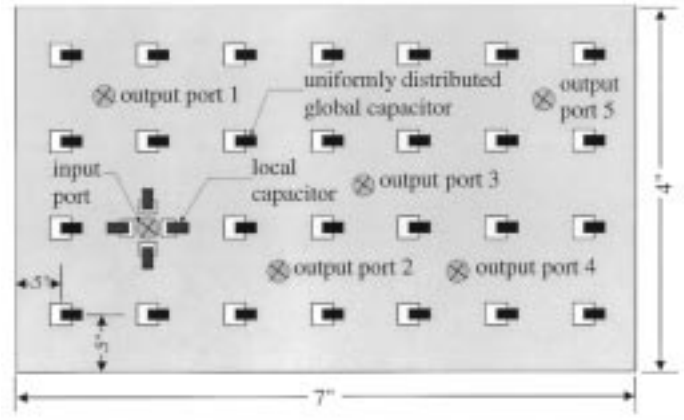

Fig. 14. A smaller PCB for the local decoupling study with 10- and 20-mil layer thickness.

estimated using the curves shown in Fig. 13, provided that the layer spacing has already been determined. If several dB of reduction is achievable, locating the decoupling capacitor(s) in proximity to an IC is beneficial. Otherwise locating the decoupling capacitor(s) where minimal inductance interconnects to the power/ground layers can be achieved is sufficient.

Fig. 15 shows the $|Z_{21}|$ decrease due to local decoupling versus layer thickness. The data replotted in this format is particularly useful for interpolating the board thickness. It is worth noting again, that the noise mitigation benefits of a local SMT decoupling capacitor extend over a very wide frequency range, well beyond the series resonant frequency limiting the effectiveness of a globally placed decoupling capacitor. The minimum spacing between decoupling capacitor(s) and an IC is limited by the issues of trace routing, component assembly, etc. In practical designs, the number of PCB layers and layer stackup that dictates power/ground pair spacing is related to other considerations as well. The results in this paper impact PCB designs with layer stackups that dictate a power/ground layer separation in excess of 30 mils. In particular, these boards will be predom-

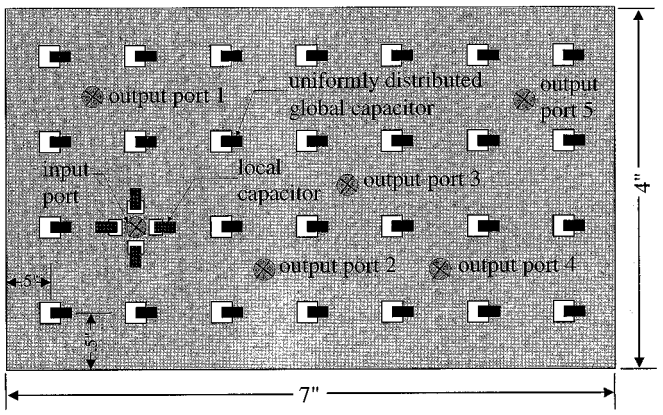

Fig. 16. The effect of PCB board size on local decoupling.

inantly 4-layer boards with a power/ground core, and 6-layer boards with four layers for routing impedance controlled signal lines. In both cases, the separation of the power and ground layers will be 30–40 mils for a standard 60–65 mil board thickness. In these cases, power-bus noise mitigation benefits from local decoupling capacitors can be achieved. However, from both an SI and EMI perspective, the thinnest power/ground layer achievable is best. In particular, power and ground layer separations of 4 mils and less are superior for power-bus noise mitigation, and impact both SI and EMI [33]–[35]. As new technologies and manufacturing techniques advance, submil separation will be achievable in practical designs. The impedance looking into the planes is then reduced, and, for a given current draw, the noise voltage resulting on the planes is directly proportional to the thickness. For multilayer PCBs with many layers, e.g., 10-layer boards, a thin power/ground layer pair can be implemented. In this case, there is little noise mitigation benefit from local decoupling. The generated design curves in Figs. 13 and 15 provide a means of estimating the local decoupling effect for a given layer spacing and proximity of the SMT capacitor to the IC, and thus helps to quatify tradeoffs between various design considerations.

Equation (21) indicates that the $|Z_{21}|$ decrease (in dB) due to local decoupling is only a function of inductances associated with the local decoupling capacitor and its adjacent IC device, if the board-related parameter $|Z'_{11}|$ is much less than $\omega(L_2 + L_3)$. This implies that PCB size should not significantly impact the local decoupling effect. In order to demonstrate this, two $|Z_{21}|$-decrease curves for the same layer thickness of 30 mils, where all PCB features were rigorously modeled using the CEMPIE formulation, were generated from the two different PCB geometries shown in Figs. 8 and 14. These curves for the $|Z_{21}|$ decrease for the two different size boards are shown in Fig. 16. It is clear that the effect of board size is relatively insignificant. The difference between the results from the two boards of differing dimensions is less than 0.35 dB. Since a smaller PCB tends to have a larger input impedance, namely a larger $|Z'_{11}|$, the Z_{21} decrease in dB is then a little bit smaller according to (21), as demonstrated in Fig. 16. As discussed before, the board size may change the inductance values by a small amount as well. This change also contributes to the small difference between the smaller and larger PCBs. With the PCB size large enough, both Z'_{11} and the inductance-value change is too small to affect the Z_{21} results.

V. Conclusion

The location of an SMT decoupling capacitor relative to an IC can impact the noise performance of the DC power-bus for certain PCB stackup configurations. Local decoupling can effectively reduce high-frequency power-bus noise for thick power/ground layer separations, which can not be mitigated by adding global decoupling capacitors. The noise mitigation benefits of local decoupling were quantified with a numerical modeling approach. The phenomenon was physically explained by mutual inductive coupling between closely spaced vias as a result of magnetic flux linkage between power and ground layers. The benefits from local decoupling were quantified as a function of capacitor/IC spacing, and power/ground layer thickness. The results presented are intended to impact PCB designs where the layer spacing of the power/ground plane pair is in excess of 30 mils, in particular 4-layer PCBs with a core, and 6-layer PCBs with four impedance controlled signal layers. For boards with more layers, achieving the lowest power-bus impedance seen looking into the planes by minimizing the separation of power and ground layers is best.

Placing decoupling capacitors adjacent to ICs may be beneficial in reducing high-frequency power-bus noise; however, it also imposes some difficulties for signal routing near the ICs, especially for some BGA packaging techniques where the balls are uniformly distributed over the package footprint, and no room beneath the ICs is available. Tradeoffs need to be evaluated carefully. For a thick power layer typically 30 mils or greater, the noise mitigation benefits of local decoupling are more significant, but may come at the expense of routing flexibility. Design curves presented in this work can be used to facilitate making these types of tradeoffs. However, for a thin power layer typically 10 mils or less, the noise mitigation effects of local decoupling are minimal, and the SMT decoupling capacitors can be placed anywhere on the PCB where space is available and minimum self inductance associated with the interconnects can be achieved.

References

[1] J. G. Yook, V. Chandramouli, L. P. B. Katehi, K. A. Sakallah, T. R. Arabi, and T. A. Schreyer, "Computation of switching noise in printed circuit boards," *IEEE Trans. Comp., Packag., Manufact. Technol. A*, vol. 20, no. 1, pp. 64–75, Mar. 1997.

[2] S. Radu and D. M. Hockanson, "An investigation of PCB radiated emissions from simultaneous switching noise," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, vol. 2, 1999, pp. 893–898.

[3] A. Vaidyanath, B. Thoroddsen, J. L. Prince, and A. C. Cangellaris, "Simultaneous switching noise: Influence of plane–plane and plane–signal trace coupling," *IEEE Trans. Comp., Packag., Manufact. Technol. B*, vol. 18, pp. 496–502, Aug. 1995.

[4] I. Novak, "Reducing simultaneous switching noise and EMI on ground/power planes by dissipative edge termination," *IEEE Trans. Adv. Packag.*, vol. 22, pp. 274–283, 1999.

[5] B. Archambeault, P. Wetmore, X. Yuan, and R. Mathews, "Modeling the effectiveness of decoupling capacitors for multilayer PCB's," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, vol. 1, 1998, pp. 522–526.

[6] F. Y. Yuan, "Analysis of power/ground noises and decoupling capacitors in printed circuit board systems," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, 1997, pp. 425–430.

[7] C. B. O'Sullivan, L. D. Smith, and D. W. Forehand, "Developing a decoupling methodology with SPICE for multilayer printed circuit boards," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, vol. 2, 1998, pp. 652–655.
[8] T. H. Hubing, J. L. Drewniak, T. P. Van Doren, and D. M. Hockanson, "Power bus decoupling on multilayer printed circuit boards," *IEEE Trans. Electromagn. Compat.*, vol. 37, pp. 155–166, May 1995.
[9] T. H. Hubing, T. P. Van Doren, F. Sha, J. L. Drewniak, and M. J. Wilhem, "An experimental investigation of 4-layer printed circuit board decoupling," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, 1995, pp. 308–312.
[10] J. Chen, M. Xu, T. H. Hubing, J. L. Drewniak, T. P. Van Doren, and R. E. DuBroff, "Experimental evaluation of power bus decoupling on a 4-layer printed circuit board," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, vol. 1, 2000, pp. 335–338.
[11] Y. Chen, Z. Chen, and J. Fang, "Optimum placement of decoupling capacitors on packages and printed circuit boards under the guidance of electromagnetic field simulation," in *Proc. Electron. Comp. Technol. Conf.*, 1996, pp. 756–760.
[12] B. Archambeault, "Analyzing power/ground plane decoupling performance using the partial element equivalent circuit (PEEC) simulation technique," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, vol. 2, 2000, pp. 779–784.
[13] N. Na, J. Choi, S. Chun, M. Swaminathan, and J. Srinivasan, "Modeling and transient simulation of planes in electronic packages," *IEEE Trans. Advanced Packag.*, vol. 23, pp. 340–352, Aug. 2000.
[14] C. Paul, *Introduction to Electromagnetic Compatibility*. New York: Wiley, 1992.
[15] H. W. Johnson and M. Graham, *High-Speed Digital Design: A Handbook of Black Magic*. Englewood Cliffs, NJ: Prentice-Hall, 1993.
[16] H. W. Ott, *Noise Reduction Techniques in Electronic Systems*. New York: Wiley, 1976.
[17] M. Ingels and M. S. J. Steyaert, "Design strategies and decoupling techniques for reducing the effects of electrical interference in mixed-mode IC's," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1136–1141, July 1997.
[18] J. Fan, J. L. Knighten, A. Orlandi, N. W. Smith, and J. L. Drewniak, "Quantifying decoupling capacitor location," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, vol. 2, 2000, pp. 761–766.
[19] J. Fan, H. Shi, A. Orlandi, J. L. Knighten, and J. L. Drewniak, "Modeling DC power-bus structures with vertical discontinuities using a circuit extraction approach based on a mixed-potential integral equation formulation," *IEEE Trans. Advanced Packag.*, vol. 24, pp. 143–157, May 2001.
[20] J. Fan, J. L. Drewniak, H. Shi, and J. L. Knighten, "DC power-bus modeling and design with a mixed-potential integral equation formulation and circuit extraction," IEEE Trans. Electromagn. Compat., to be published.
[21] H. Shi, "Study of printed circuit board power-bus design with a circuit extraction technique based on a quasi-static MPIE/MOM formulation," Ph.D., Dept. Elect. Comput. Eng., Univ. Missouri-Rolla, 1997.
[22] X. D. Cai, G. L. Costache, R. Laroussi, and R. Crawhall, "Numerical extraction of partial inductance of package reference (power/ground) planes," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, 1995, pp. 12–15.
[23] X. Ye, J. Fan, M. Koledintseva, and J. L. Drewniak, "DC power bus design with FDTD modeling including a dispersive media," in *Proc. 9th Top. Meet. Elect. Perform. Electron. Packag.*, 2000, pp. 55–58.
[24] F. Y. Yuan, "Electromagnetic modeling and signal integrity simulation of power/ground networks in high speed digital packages and printed circuit boards," in *Proc. Design Automat. Conf.*, 1998, pp. 421–426.
[25] A. E. Ruehli and A. C. Cangellaris, "Application of the partial element equivalent circuit (PEEC) method to realistic printed circuit board problem," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, vol. 1, 1998, pp. 182–187.
[26] B. Archambeault, "Using the partial element equivalent circuit (PEEC) simulation technique to properly analyze power/ground plane EMI decoupling performance," in *Proc. 16th Ann. Rev. Progress Appl. Computat. Electromagn.*, vol. 1, 2000, pp. 423–430.
[27] H. Heeb and A. E. Ruehli, "Three-dimensional interconnect analysis using partial element equivalent circuits," *IEEE Trans. Circuits Syst. I*, vol. 39, Nov. 1992.
[28] A. E. Ruehli and A. C. Cangellaris, "Overview of the partial element equivalent circuit (PEEC) electromagnetic modeling approach," *Appl. Computat. Electromagn. Soc. J.*, vol. 14, no. Suppl. 1, pp. 17–27, Mar. 1999.
[29] D. M. Pozar, *Microwave Engineering*, Second ed. New York: Wiley, 1998.
[30] J. Fan, "Modeling and design of DC power buses in high-speed digital circuit designs," Ph.D. dissertation, Dept. Elect. Comput. Eng., Univ. Missouri-Rolla, 2000.
[31] M. Xu, Y. Ji, T. H. Hubing, T. P. Van Doren, and J. L. Drewniak, "Development of a closed-form expression for the input impedance of power-ground plane structures," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, vol. 1, 2000, pp. 77–82.
[32] J. Fan, J. L. Drewniak, J. L. Knighten, N. W. Smith, and A. Orlandi, "Calculation of self and mutual inductances associated with vias in a DC power bus structure from a circuit extraction approach based on a mixed-potential integral equation formulation," in *Proc. 14th Int. Zurich Symp. Tech. Exhibition Electromagn. Compat.*, 2001, pp. 521–526.
[33] X. Ye, M. Y. Koledintseva, M. Li, and J. L. Drewniak, "DC power-bus design using FDTD modeling with dispersive media and surface mount technology components," *IEEE Trans. Electromagn. Compat.*, vol. 43, pp. 579–587, Nov. 2001.
[34] X. Ye, D. M. Hockanson, M. Li, W. Cui, Y. Ren, J. L. Drewniak, and R. E. DuBroff, "EMI mitigation with multi-layer power bus stacks and via stitching of reference planes," *IEEE Trans. Electromagn. Compat.*, vol. 43, pp. 538–548, Nov. 2001.
[35] W. Cui, X. Ye, B. Archambeault, D. White, M. Li, and J. L. Drewniak, "EMI resulting from signal via transitions through the DC power bus," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, vol. 2, 2000, pp. 821–826.

Jun Fan (S'97–M'00) received the B.S. and M.S. degrees in electrical engineering from Tsinghua University, Beijing, China, in 1994 and 1997, respectively. He received the Ph.D. degree in electrical engineering from the University of Missouri, Rolla, in 2000.

He is currently with NCR Corporation, San Diego, CA, where he works as a Senior Hardware Engineer. His research interests include signal integrity and EMI designs in high-speed digital systems, dc power bus modeling, PCB noise reduction, and differential signaling.

Dr. Fan received the Conference Best Paper Award from the Applied Computational Electromagnetics Society in 2000. He serves as Secretary of TC-9 Computational Electromagnetics Committee of the IEEE EMC Society.

James L. Drewniak (S'85–M'90–SM'01) received the B.S. (highest honors), M.S., and Ph.D. degrees in electrical engineering, all from the University of Illinois, Urbana-Champaign, in 1985, 1987, and 1991, respectively.

In 1991, he joined the Electrical Engineering Department at the University of Missouri, Rolla, where he is a Professor and is affiliated with the Electromagnetic Compatibility Laboratory. His research interests include the the development and application of numerical methods for investigating electromagnetic compatibility problems, packaging effects, and antenna analysis, as well as experimental studies in electromagnetic compatibility and antennas.

He is an Associate Editor of the IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY.

James L. Knighten (S'62–M'77–SM'97) received the B.S. and M.S. degrees in electrical engineering from Louisiana State University, Baton Rouge, in 1965 and 1968, respectively. He received the Ph.D. degree in electrical engineering from Iowa State University, Ames, in 1976.

He is currently with NCR Corporation, San Diego, CA, and serves as a Technical Consultant. Since 1996, he has worked in the field of electromagnetic research interests including the EMI and signal integrity issues related to design of digital computing systems that employ high-speed signaling. Prior to joining NCR, he was with Maxwell Technologies, Inc. and, earlier, with IRT Corporation, San Diego, CA, where he held management positions and was engaged in the study and mitigation design of the lightning, and high-powered microwaves on electronic systems. He has presented numerous technical papers on topics involving various aspects of electromagnetics and taught short courses on electromagnetic pulse effects and electronics survivability both in the USA and in Europe.

Norman W. Smith received the B.S. degree in electrical engineering from Auburn University, Auburn, AL, in 1985 and the M.S. degree in computer engineering from National Technological University in 1998.

He is currently with NCR Corporation, San Diego, CA, and serves on the technical staff as a Consulting Engineer. In his eleven years with NCR, he has worked on board-level design for networking products. He is responsible for signal integrity at the board and ASIC levels. His research interests include signal integrity and EMI related to high speed networks. Prior to joining NCR, he worked with Digital Technology, Dayton, OH, for five years where he developed emulators for digital avionics busses. He has coauthored twelve IEEE EMC papers.

Antonio Orlandi (M'90–SM'97) was born in Milan, Italy, in 1963. He received the Laurea degree in electrical engineering from the University of Rome, La Sapienza, Italy, in 1988.

He was with the Department of Electrical Engineering, University of Rome, La Sapienza, from 1988 to 1990. In 1990, he was appointed Assistant Professor, and in 1998, appointed Associate Professor with the Department of Electrical Engineering of the University of L'Aquila, L'Aquila, Italy. He has published papers in the field of electromagnetic compatibility in lightning protection systems and power drive systems. Current research interests are in the field of numerical methods to approach signal integrity issues in high-speed digital systems.

Dr. Orlandi received the IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY Best Paper Award in 1997. He is a member of the Education and TC-9 Computational Electromagnetics Committees of the IEEE EMC Society, the Editorial Boards of the Applied Computational Electromagnetic Society (ACES) Journal, and Chairman of the EMC INNOVATION Technical Committee of the International Zurich Symposium and Technical Exhibition on EMC.

Thomas P. Van Doren (S'60–M'69–SM'96) received the B.S., M.S., and Ph.D. degrees from the University of Missouri, Rolla (UMR), in 1962, 1963, and 1969, respectively.

From 1963 to 1965, he served as an Officer in the U.S. Army Security Agency. From 1965 to 1967, he was a Microwave Engineer with Collins Radio Company, Dallas, TX. Since 1967, he has been a member of the electrical engineering faculty at UMR, where he is currently a Professor. His research interests concern developing circuit layout grounding, and shielding techniques to improve electromagnetic compatibility. He has taught short courses on electromagnetic compatibility to more than 10 000 engineers and technicians representing 200 corporations.

Dr. Van Doren received the IEEE EMC Society Richard R. Stoddard Award for contributions to electromagnetic compatibility research and education in 1995. He is a Registered Professional Engineer in the state of Missouri and a member of Eta Kappa Nu, Tau Beta Pi, and Phi Kappa Phi.

Todd H. Hubing (S'82–M'82–SM'93) received the B.S.E.E. degree from the Massachusetts Institute of Technology, Cambridge, in 1980, the M.S.E.E. degree from Purdue University, West Lafayette, IN, in 1982, and the Ph.D. degree in electrical engineering from North Carolina State University, Raleigh, in 1988.

He is currently a Professor of electrical engineering with the University of Missouri, Rolla (UMR), where he is also a member of the principal faculty in the Electromagnetic Compatibility Laboratory. Prior to joining the UMR in 1989, he was an Electromagnetic Compatibility Engineer with IBM, Research Triangle Park, NC. Since joining the UMR, the focus of his research has been measuring and modeling sources of electromagnetic interference. He has authored or presented more than 70 technical papers, presentations, and reports on electromagnetic modeling and electromagnetic compatibility related subjects.

Dr. Hubing writes the satirical "Chapter Chatter" column for the IEEE *EMC Society Newsletter*. He is on the Board of Directors for the IEEE EMC Society.

Richard E. DuBroff (S'74–M'77–SM'84) received the B.S.E.E. degree from Rensselaer Polytechnic Institute, Troy, NY, in 1970, and the M.S. and Ph.D. degrees in electrical engineering from the University of Illinois, Urbana-Champaign, in 1972 and 1976, respectively.

From 1976 to 1978, he held a Postdoctoral position with the Ionosphere Radio Laboratory, University of Illinois, Urbana-Champaign, and worked on backscatter inversion of ionospheric electron density profiles. From 1978 to 1984, he was a Research Engineer with the Geophysics Branch of Phillips Petroleum, Bartlesville, OK. Since 1984, he has been affiliated with the University of Missouri, Rolla, where he is currently a Profesor with the Department of Electrical and Computer Engineering.