Short Papers

Power Bus Isolation Using Power Islands in Printed Circuit Boards

Juan Chen, Todd H. Hubing, Thomas P. Van Doren, and Richard E. DuBroff

***Abstract*—Power islands are often employed in printed circuit board (PCB) designs to alleviate the problem of power bus noise coupling between circuits. Good isolation can be obtained over a wide frequency band due to the large series impedance provided by the gap between the power islands. However, power bus resonances may degrade the isolation at high frequencies. The amount of isolation also depends on the type of connection between power islands and the components on the board. This paper experimentally investigates the effectiveness of several power island structures up to 3.0 GHz.**

***Index Terms*—Board resonance, coupling, power bus isolation, power island.**

I. Introduction

Power bus noise caused by the switching of integrated circuits (ICs) can cause signal integrity problems and be a significant source of electromagnetic interference (EMI). It is often desirable to isolate relatively noisy regions of a printed circuit board (PCB) power bus from quiet areas by dividing the power bus into separate regions using a gap in the power plane [1], [2]. These regions of the power bus are sometimes referred to as power islands. Power island structures are used to prevent power bus noise from propagating between all devices on the same power bus. For example, the power supplies for digital and analog devices may be isolated, and noisy devices such as microprocessors may be isolated from other susceptible components.

Theoretically, splitting the power plane of a PCB prevents current and voltage spikes from spreading to the entire power distribution bus. Without any direct connection between the power islands, the primary noise coupling mechanism is capacitive coupling across the gap. This coupling capacitance is generally very low compared to the inter-plane capacitance and provides a large series impedance between islands.

The effect of power island structures on power bus isolation was experimentally investigated in [3]. A numerical model for segmented power bus structures was presented in [4] and [5]. This paper further investigates power island structures and draws general conclusions regarding their effectiveness in different situations. Populated and unpopulated production boards are measured and compared. Also the power island isolation for a prototype three-layer board with a symmetric stack-up is investigated.

II. Two-Layer Test Board Measurements

Two simple test boards with the layout shown in Fig. 1 were built to evaluate the effectiveness of various isolation strategies. Both boards were 6 inches long and 4 inches wide and consisted of two copper planes separated by FR-4 material. The board thickness was 63 mils for Board 1 and 95 mils for Board 2. A gap was cut in the middle of the power plane forming two isolated power islands. Two 85-mil diameter semi-rigid coaxial probes were attached to the center of the power islands. The voltage transfer coefficient, S_{21}, between these two ports was measured using an HP8753D network analyzer. The magnitude of S_{21} is the ratio of transmitted signal at Port 2 to the incident signal at Port 1 and provides a good indication of the isolation between the two ports [6]. Lower levels of $|S_{21}|$ imply better isolation.

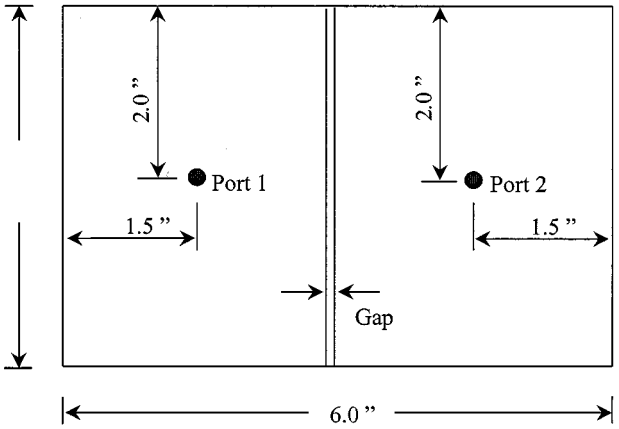

Fig. 1. Layout of boards 1 and 2.

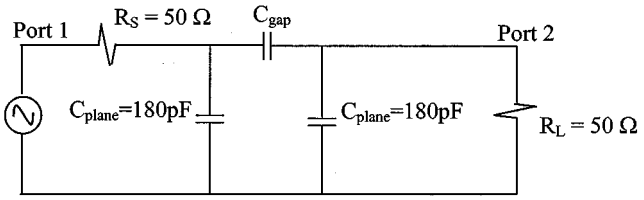

Fig. 2. A lumped-element circuit model of the test configuration.

Fig. 2 shows a lumped-element circuit model for the test configuration. The power island structure is modeled as a π-network comprised of two shunt capacitors representing the interplane capacitances of the two islands and one series capacitor representing the coplanar gap capacitance [3]. The source and load impedances defined by the network analyzer are 50 Ω. The gap capacitance is generally on the order of several picofarads and is much lower than the interplane capacitance.

Fig. 3 shows calculated values of $|S_{21}|$ for the model in Fig. 2. There is little coupling at very low frequencies due to the isolation provided by $C_{\rm gap}$. There is also little coupling at very high frequencies due to the low impedance of $C_{\rm plane}$. For the values of R and C in Fig. 2, the coupling peaks at 30 MHz. The coupling is greater for larger values of $C_{\rm gap}$.

Fig. 4 plots the measured $|S_{21}|$ as a function of frequency for the test board in Fig. 1 with different gap widths. The measured results correlate to the model results in Fig. 3 very well except at the higher frequencies where the coupling is weak and the planes are no longer electrically small.

The isolation between islands is a function of the gap width. Wider gaps provide better isolation due to smaller gap capacitance. The uppermost curve in Fig. 4 corresponds to a 16-mil gap. Each time the gap width is doubled additional isolation is achieved. This effect

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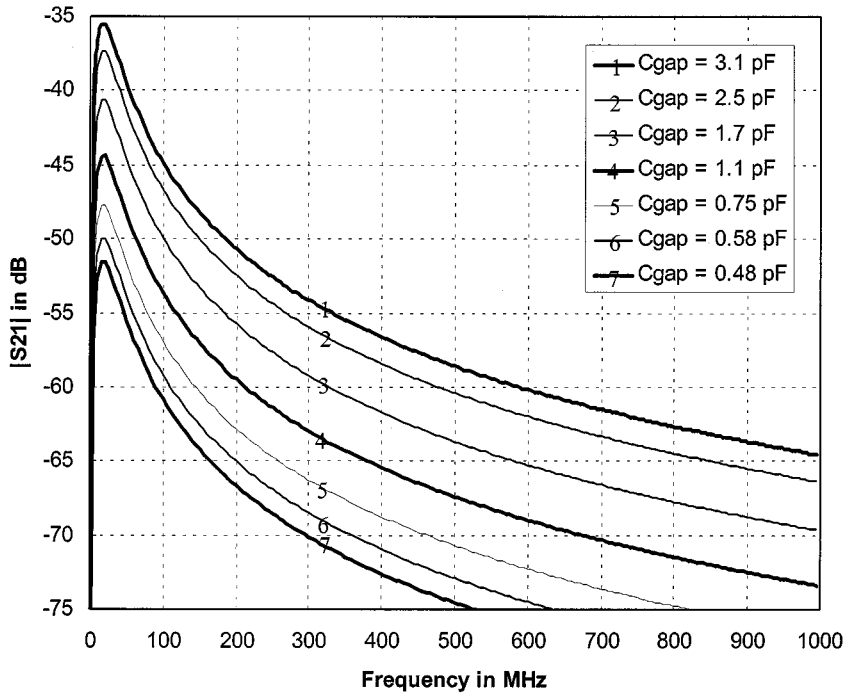

Fig. 3. Calculated $|S_{21}|$ for board 1 based on circuit model in Fig. 2.

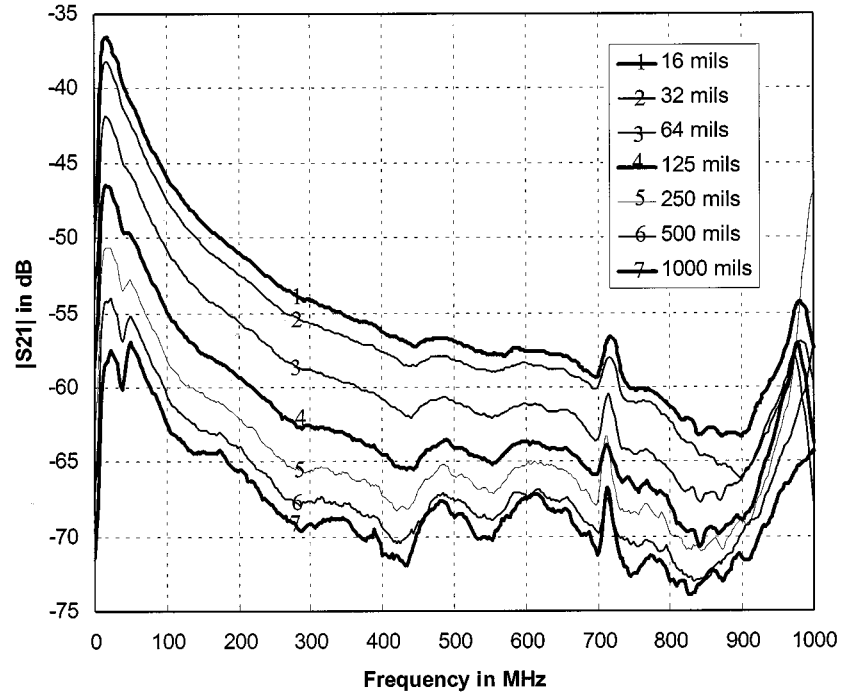

Fig. 4. Measured $|S_{21}|$ for board 1 with different gap widths.

is most significant when the gap width is close to the plane spacing (i.e., 63 mils).

As the circuit model in Fig. 2 suggests, isolation is also a function of the interplane capacitance and hence a function of the spacing between the power and return planes. Thinner boards achieve better isolation for a fixed gap width. Larger values of interplane capacitance divert more source current causing less current to reach the other island. Fig. 5 compares the measured $|S_{21}|$ for Boards 1 (63 mils thick) and 2 (95 mils thick) with the same 32-mil gap width. The $|S_{21}|$ level of Board 1 is 4–9 dB lower than that of Board 2 at frequencies below 900 MHz.

At frequencies away from board resonances, the coupling between the two islands is weak because the gap capacitance is very low compared to the interplane capacitance. However, at frequencies where the power bus structure is resonant, it is possible to get relatively good coupling between planes and the isolation may be significantly degraded. Fig. 6 shows the effect of board resonance on power island isolation up

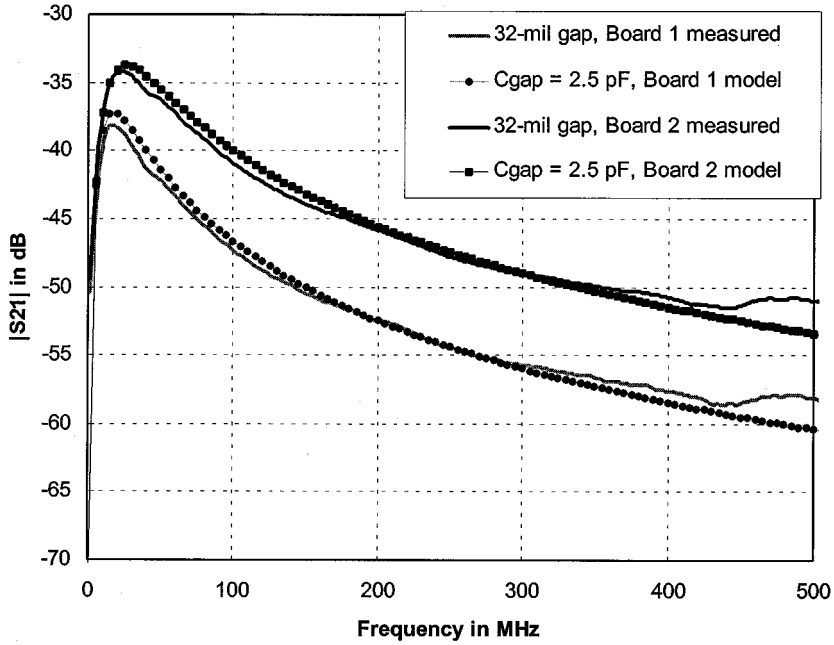

Fig. 5. Measured and calculated $|S_{21}|$ for boards with different plane spacing.

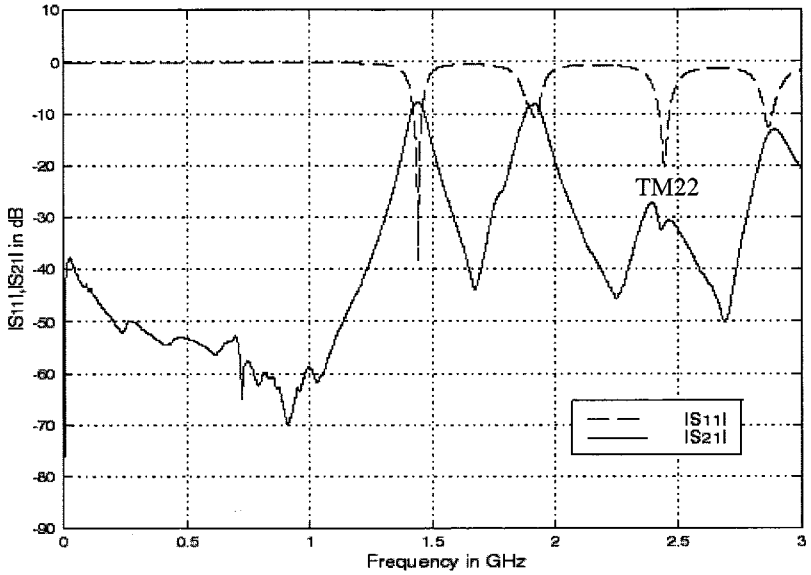

Fig. 6. Measured $|S_{11}|$ and $|S_{22}|$ for board 1.

to 3.0 GHz. At certain board resonant frequencies, the $|S_{11}|$ response dips, indicating higher board impedance. At these frequencies, more power is injected into the board and more power is coupled from one power island to the other, thus the $|S_{21}|$ response peaks. In this example, the two identical islands resonate at the same frequencies, so the resonance effect is significant. Better isolation can be obtained using asymmetric power island structures [3].

In some applications, it is desirable to implement a power island structure that has good high frequency isolation while maintaining DC continuity. Power islands can be connected using conductive bridges or ferrite beads for this purpose. Experiments were performed using Board 1 to show the effect of these connections.

Fig. 7 compares the isolation of a gapped plane to the results obtained from a solid plane, a gapped plane with a copper bridge, and a gapped plane with a ferrite bead connecting the islands. In these measurements, a 100-nF surface mount capacitor was connected near the driving port to simulate a low-impedance source that was more representative of real printed circuit board configurations. A strip of copper tape was used as the conductive bridge. A surface mount BLM21B471SD ferrite bead was used as the ferrite bead bridge. The bead's resistance was measured using an impedance analyzer and found to be 470 Ω at 100 MHz.

Compared to the continuous power plane, the power island structure exhibited much better isolation over nearly the entire frequency range, except at board resonant frequencies as expected. The gapped plane with a copper bridge provided no additional isolation below 100 MHz. The resonance at 500 MHz was shifted to 300 MHz causing $|S_{21}|$ to decrease by about 20 dB from 500 to 900 MHz. The gapped plane

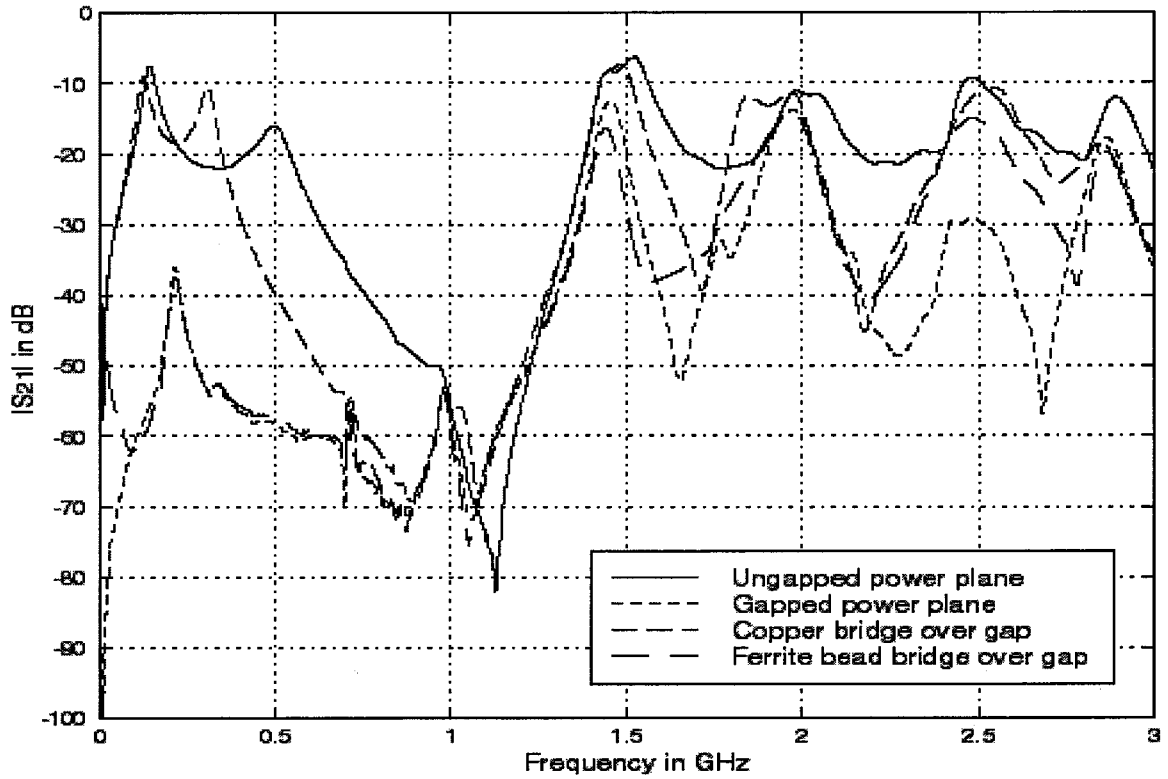

Fig. 7. Effect of connections bridging the power islands.

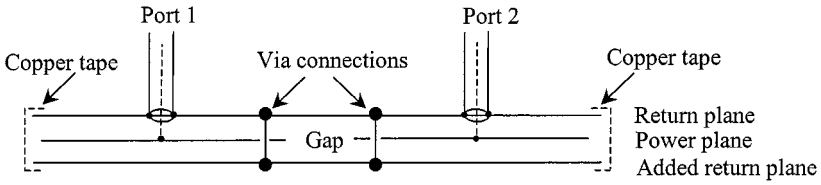

Fig. 8. Three-layer board stack-up.

with a ferrite bead connection demonstrated almost the same degree of isolation as the totally gapped structure above 150MHz.

A three-layer board with a symmetric stack-up was also investigated in this study. This board simulates a power island structure in boards with a power plane sandwiched between two power-return planes. As shown in Fig. 8, a one-layer board with the same thickness as Board 1 was added to the original two-layer board to form a three-layer stack-up. The top and bottom planes were both return planes and the middle plane represented the segmented power plane. The two return planes were connected by sealing all edges with copper tape or by making eight via connections near the gap location.

Fig. 9 compares the isolation for the original two-layer board and the symmetric three-layer board. The three-layer configuration studied here improved the isolation below 200 MHz, but exhibited little if any improvement above 200 MHz. From 250 MHz to 1.5 GHz, the isolation was even worse. In the 3-layer configuration, current on one side of the gap can couple to the additional plane and couple back to the power plane on the opposite side of the gap. This coupling path is indicated by the impedances Z_3 and Z_4 in Fig. 10. Also, three-layer configurations introduce new board resonances below the first resonance of the original two-layer structure.

III. Four-Layer Production Board Measurements

Measurements were made on a populated personal computer (PC) motherboard and an unpopulated version of this board. The dimensions, the location of the power islands, and the location of ports used in the experiments are illustrated in Fig. 11. The boards were 4-layer boards with power and return planes on Layers 3 and 2, respectively. The power plane was divided into two power islands, designated Region 1 and Region 2 in the figure.

$|S_{21}|$ measurements were performed on the fully populated PC motherboard. Because the power and return planes were buried between the two component layers and were not readily accessible, measurements were made between locations on the same island and on different islands with approximately equal distances between ports to compare the level of isolation. To obtain the measurement results shown in Fig. 12, the two ports were located at L1, L2 for the solid curve and L1, L3 for the dashed curve, respectively. It is apparent that the isolation between ports on different islands is much better than the isolation between ports on the same island. The dashed curve is 20–30 dB lower than the solid curve over most of the frequency range.

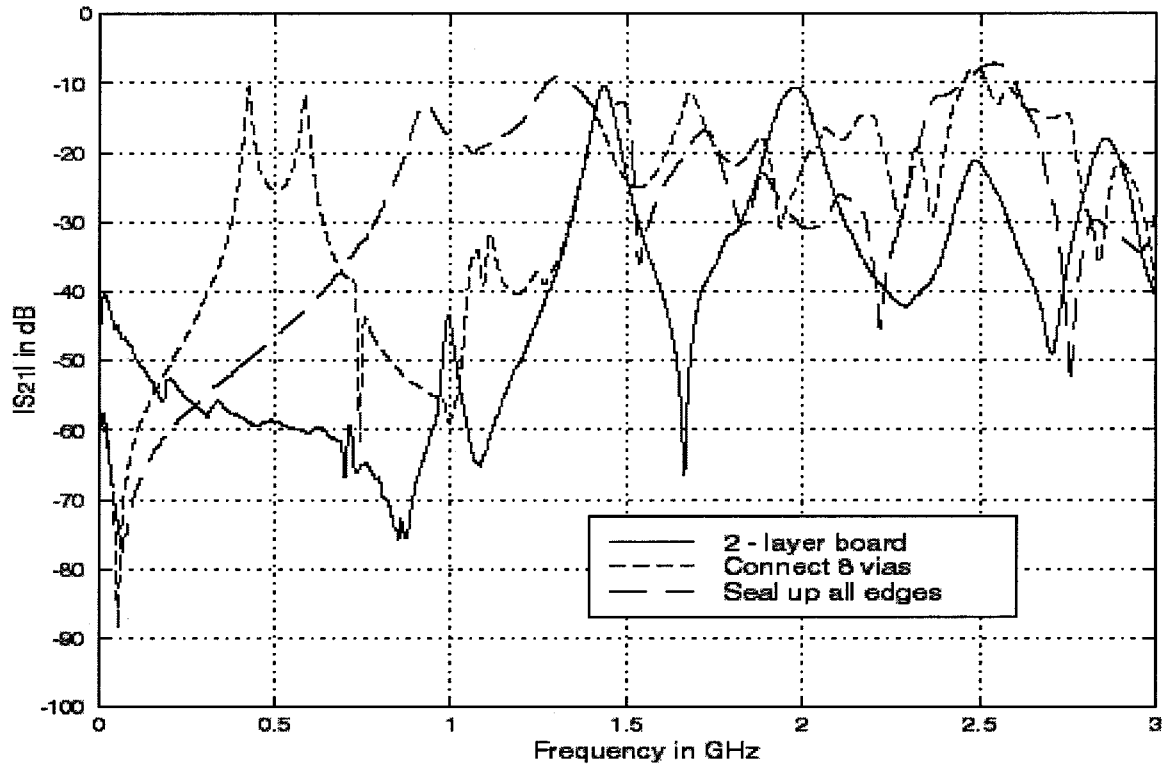

Fig. 9. $|S_{21}|$ for two-layer and three-layer boards.

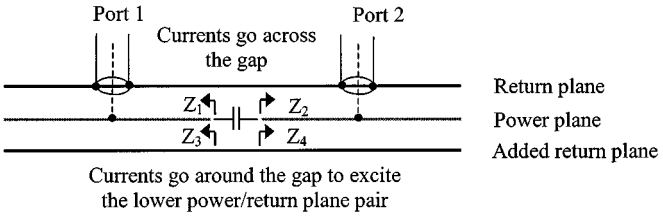

Fig. 10. Current path in the three-layer board.

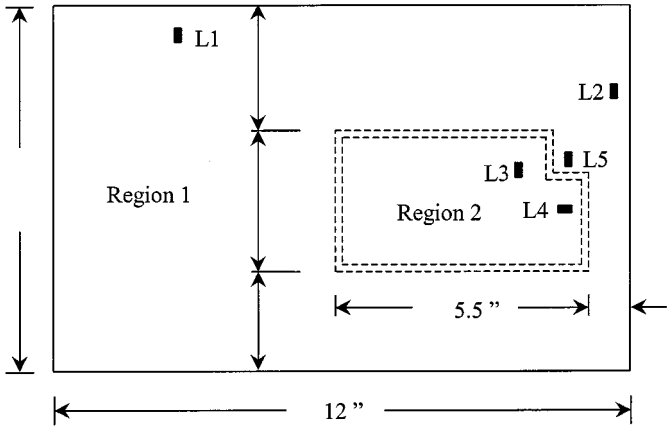

Fig. 11. Layout of the PC motherboards.

Similarly, Fig. 13 shows the measured coupling between two ports in close proximity on same island and on different islands. The ports were located at L3, L4 for the solid curve and L3, L5 for the dashed curve, respectively. Again the isolation between ports on different islands is better than that between ports on the same island. The dashed curve is 10–20 dB lower than the solid curve over nearly the entire 0–3 GHz frequency range.

The measurements above were repeated at several additional near and distant port locations with similar results. It is clear that the power island on this populated PC motherboard improves the isolation between devices on the island and devices on the rest of the board. The amount of additional isolation provided by the island is related to the distance between the ports. Comparing the two figures above, the overall $|S_{21}|$ levels in Fig. 13 are 15–30 dB higher than those in Fig. 12 above 1 GHz, indicating the isolation is better between distant ports than between ports in close proximity. The greater level of isolation between distant ports is not predicted by the model in Fig. 2, because modeling the power island as a lumped capacitance implies the position of the connection to the power island is unimportant. Nevertheless, greater isolation is observed even at frequencies where the planes are electrically small. A previous study of 4-layer boards [7] shows that the lumped-capacitance model for electrically small power bus structures is inadequate under certain conditions. In particular, when the spacing between power island and ground planes is greater than $\sim$30 mils, the mutual inductance between vias cannot be ignored [7], [8]. The mutual inductance between closely spaced ports encourages more current to flow into the receiving port than the model in Fig. 2 predicts. Therefore, isolation is degraded between ports in close proximity. Furthermore, the mutual inductance between the ports and the decoupling capacitors near them in populated boards, improves the isolation between distant ports. This is particularly evident at low frequencies where the board is electrically small, but the effect of the mutual inductance can be observed at frequencies well beyond the first board resonances [7], [8]. Therefore, the isolation between power islands on a populated four-layer board

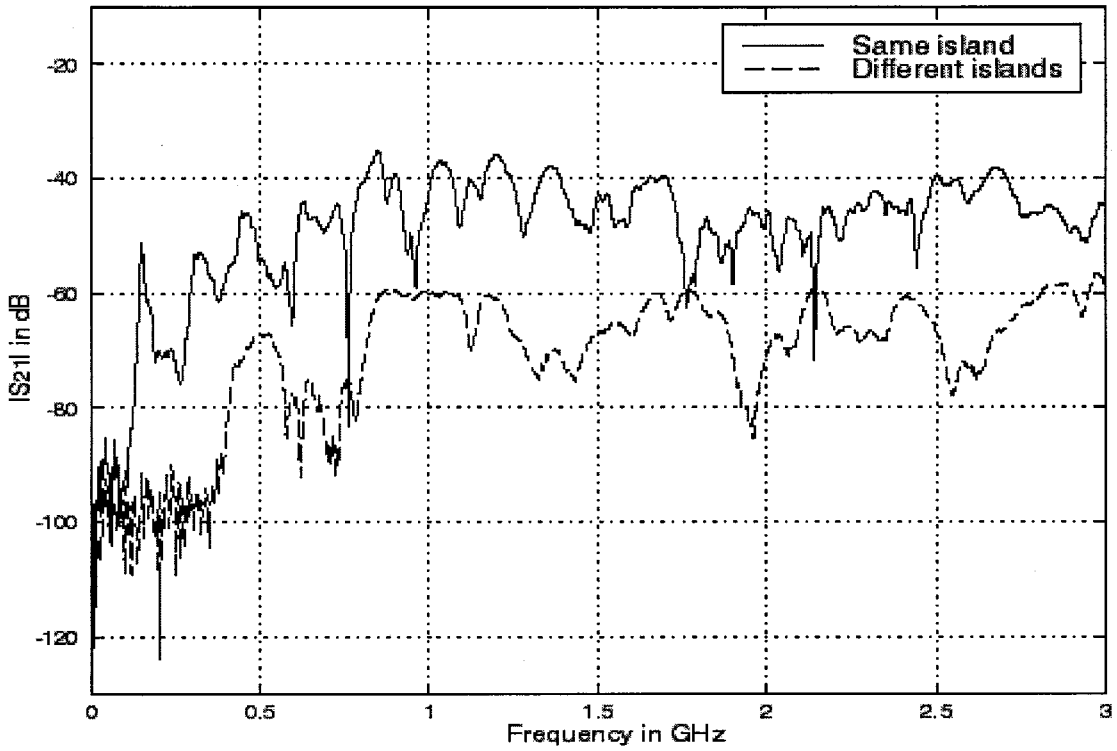

Fig. 12. Measured $|S_{21}|$ on same island and on different islands between distant ports.

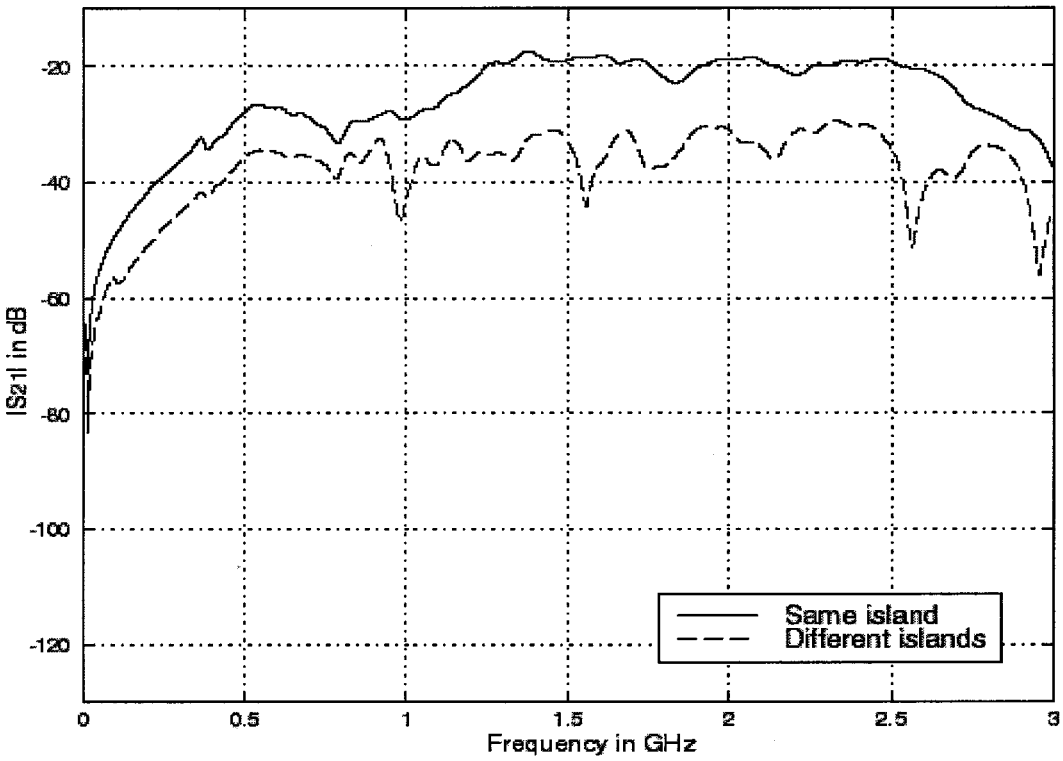

Fig. 13. Measured $|S_{21}|$ on the same island and on different islands between ports in close proximity.

is a function of the gap geometry, decoupling capacitor location, and the location of the active devices.

Fig. 14 compares the power island isolation between distant ports L1 and L3 for populated and unpopulated motherboards. The populated board exhibits better power island isolation over most of the 0–3-GHz frequency band. Fig. 15 compares the isolation between closely spaced ports L3, L5 on populated and unpopulated boards. Since these ports are much nearer to each other than they are to any

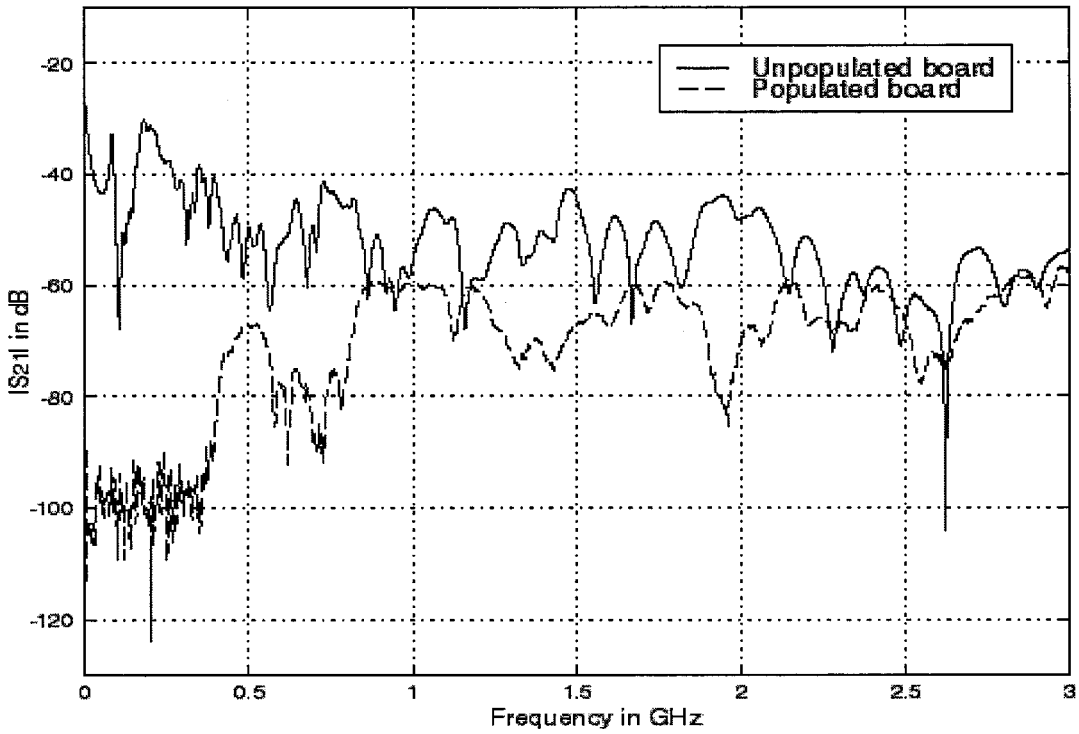

Fig. 14. Measured $|S_{21}|$ between distant ports on different islands.

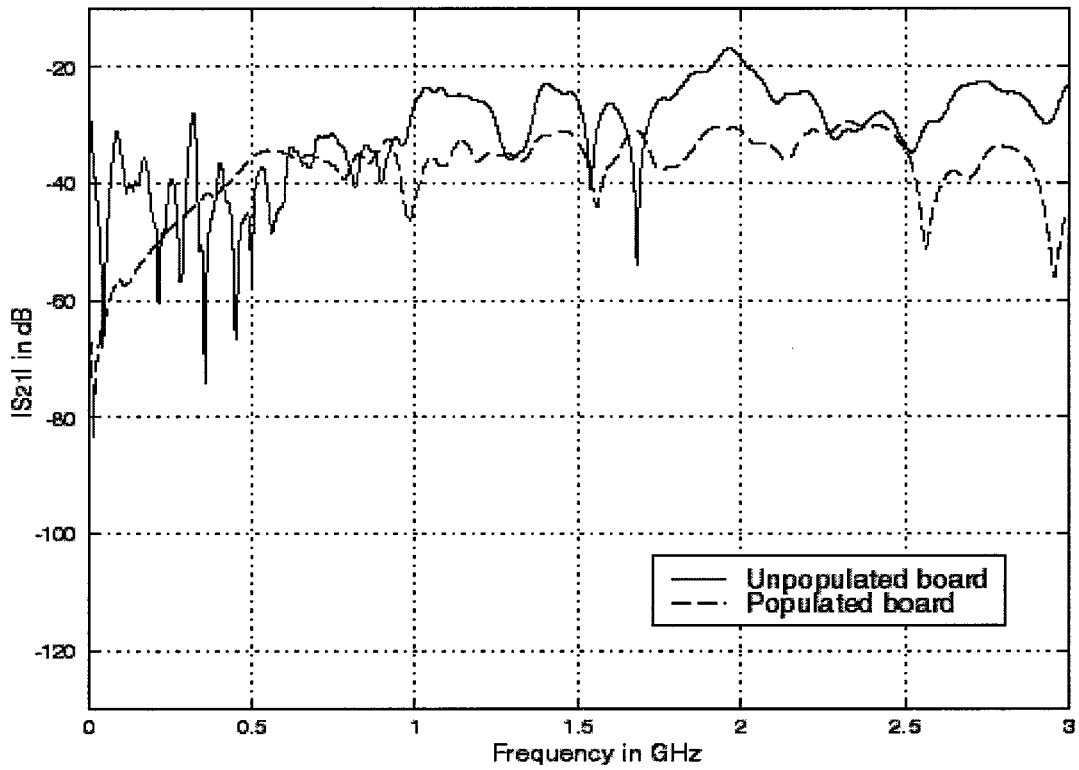

Fig. 15. Measured $|S21|$ between ports in close proximity on different islands.

decoupling capacitors, the decoupling on the populated board does not significantly improve the power bus isolation. However, resonances in the populated board are damped resulting in a modest improvement in the isolation.

IV. Summary

Power islands are sometimes used in printed circuit board designs to isolate devices that generate power bus noise from devices susceptible to power bus noise. The measurements performed for this study were

designed to evaluate the effectiveness of various power island structures.

Initial measurements were conducted on a bare 2-layer board at frequencies where both islands were electrically small. This structure can be readily modeled using a simple capacitor-divider circuit (Fig. 2). The measured results indicated that significant isolation (relative to a solid power bus) was achieved even with a relatively narrow gap (16 mils) between the planes. Wider gaps resulted in additional isolation, although the importance of the gap width diminished when the gap width was more than twice the plane separation. Connecting the power islands with a narrow copper bridge nearly eliminated the isolation provided by the gap structure at most frequencies. The small amount of inductance due to the bridge was not enough to impede current flow significantly. However, connecting the power islands with a ferrite bead (chosen to have a high impedance at the frequencies of interest) was nearly as effective as the original gapped structure.

At frequencies where each power island was no longer electrically small, additional factors come into play. The amount of coupling across the gap is a function of the electric field strength at the gap and this is a function of the source and load positions on the power islands. At frequencies where both power islands are resonant, the isolation provided by the gapped structure may be minimal. For this reason power islands should not have exactly the same size and shape.

Measurements of a production PC motherboard with a power island also indicate that power islands can be used effectively to isolate power bus noise in one area of the board from devices in another area. In the boards evaluated, the amount of additional isolation (relative to a solid plane) was generally several dB or more depending on the location of the source and receiver.

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Electromagnetic Interference Mitigation by Using a Spread-Spectrum Approach

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***Abstract*—We investigate a new technique, referred to as spread-spectrum clock generation (SSCG), for reducing the level of radiated emission from devices with digital clock signals. To calculate the radiated emissions from such devices, we model the radiating geometry and compute the radiated field at a multitude of frequencies by using NEC-4, which is an electromagnetic field solver based on the method of moments (MoM). We consider a variety of modulating profiles for the spread spectrum clock and demonstrate that by using a frequency deviation of only 1%, we can achieve from 10 to 30 dB reduction in the radiated emission levels.**

***Index Terms*—Electromagnetic interference, metallic shield, modeling, spread-spectrum clock.**

I. INTRODUCTION

A novel technique involving the frequency modulation of the clock and referred to as the spread-spectrum clock generation (SSCG) method [1], [3] has recently been proposed [3]–[5] for reducing the radiated emissions from digital electronic devices. This new technique, which is analogous to the spread-spectrum technique widely used in communications [2], effectively spreads the energy of discrete frequency harmonics over a wider range of frequencies. In this paper, we investigate the SSCG technique in some detail and show that the amplitude of the harmonics of the clock signal can be reduced by about 6–18 dB, depending on the clock frequency and frequency deviation of the modulation. Then, we investigate the level of EMC interference signals radiated by a digital device by multiplying the frequency response of the device with the spectrum of its clock. The frequency response is obtained by computing the radiated field of the device with NEC by using a time-harmonic excitation of constant phase and magnitude for various frequencies across the band of interest. The spectrum of the digital clock is computed via the FFT of the time waveform of the clock.

II. SPREAD SPECTRUM CLOCK

Modulation of the clock frequency creates side-bands, spreading the emission spectrum in the process. Lin [6] has shown that the frequency modulation is particularly effective for switching power circuits in reducing the level of the fundamental frequency, especially if the switching frequency is less than 150 kHz and the modulating frequency is chosen to be somewhat greater than 200 Hz.

Consider a clock signal represented by $f(t)$, shown in Fig. 1. The pulse shape shown in this figure is exaggerated to convey the idea that the pulse width of the clock signal varies over the period T of the modulating waveform.

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