An Experimental Procedure for Characterizing Interconnects to the DC Power Bus on a Multilayer Printed Circuit Board

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***Abstract*— The effectiveness of dc power-bus decoupling is impacted by the inductance associated with interconnect vias in printed circuit boards (PCB's). Adequate characterization of these interconnects is necessary to facilitate modeling and simulation, and to assess the effectiveness of added decoupling. In this study, a measurement procedure is presented for determining the series inductance and resistance of an interconnect with a network analyzer. The validity and limitations of the procedure are discussed. Experimental results of interconnect parameters on an 8 × 10 in ten-layer test-board corroborate those measured with a precision impedance analyzer. The measured interconnect values are used to simulate several cases of power-bus decoupling which show good agreement with two-port swept frequency measurements.**

***Index Terms*— Decoupling, interconnect model, multilayer PCB, power bus modeling**

I. Introduction

THE rapidly increasing speed of digital devices raises concerns for signal integrity (SI), as well as electromagnetic interference (EMI) problems that result from simultaneous device switching. Adding decoupling capacitors between the power and ground planes on a multilayer printed circuit board is a common strategy for mitigating the simultaneous switching, or delta-I noise [1]–[3]. As compared to single- or doubled-sided boards, a multilayer printed circuit board (PCB) can accommodate a low-impedance power-bus structure as a result of one or multiple sets of planes dedicated to both V_{cc} and GND. Critical power-bus issues include the total capacitance, individual capacitor values, and locations of the decoupling capacitors. Models to aid the designer in developing and evaluating a power-bus design must include the parameters of the external decoupling interconnects. A simple procedure is presented herein for measuring surface mount technology (SMT) interconnect parasitics on PCB's that use entire planes for V_{cc} and GND. This study employs a test-board with high-capacitance low-inductance power planes with a 10 mil layer spacing.

SMT decoupling capacitors have greatly reduced the interconnect inductance to PCB power planes as compared to leaded components. However, the inductance associated with vias is still typically on the order of a few nanohenries for a 10 mil layer spacing. The effectiveness of decoupling with an SMT decoupling capacitor is limited by the inductance associated with the traces/vias of the interconnect for frequencies greater than a few megahertz [4]. Adequate characterization of the series inductance and resistance of interconnect traces/vias is essential for developing both lumped-element and distributed power-bus models, although a lumped-element power-bus model valid below the distributed resonances of the PCB board is treated herein in particular [5], [6]. The interconnect inductance can be measured with an impedance analyzer, such as the HP 4291A (1 MHz–1.8 GHz), with high accuracy. The HP 4291A impedance analyzer is a recently introduced instrument that has better accuracy for measuring large and small impedances than a conventional network analyzer employing square-law detectors [7]. However, this specialized precision instrument may not be available in many laboratories. This study introduces a two-port procedure for characterizing decoupling interconnects on a multilayer PCB power-bus having entire V_{cc}-GND planes using a network analyzer. The interplane capacitance is first determined with an LCR meter. A metal strip is then applied to short the interconnect of concern, whose inductance is determined from the resonance frequency of $|S_{21}|$, and resistance from the input impedance (real part) at Port 1. Interconnect parameters measured on the ten-layer test-board using the proposed two-port procedure are compared with more accurate results obtained from an impedance analyzer. Experimental results are presented to demonstrate the approach, and the limitations of the procedure are discussed.

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II. A Lumped Element Model of the DC Power-Bus

A. Test Board Geometry

A ten-layer 8 × 10 in test-board with 10 mil layer-spacing was employed for the measurements. The board had a total of 63 pairs of bonding pads for connecting SMT decoupling capacitors between the power and ground planes. The top layer of the configuration is shown in Fig. 1. The 63 pairs of bonding pads can be divided into nine identical pattern groups placed at several locations on the board and are labeled 1–9 accordingly. Each group contains seven different interconnect patterns numbered P1–P7 from the top down as shown in

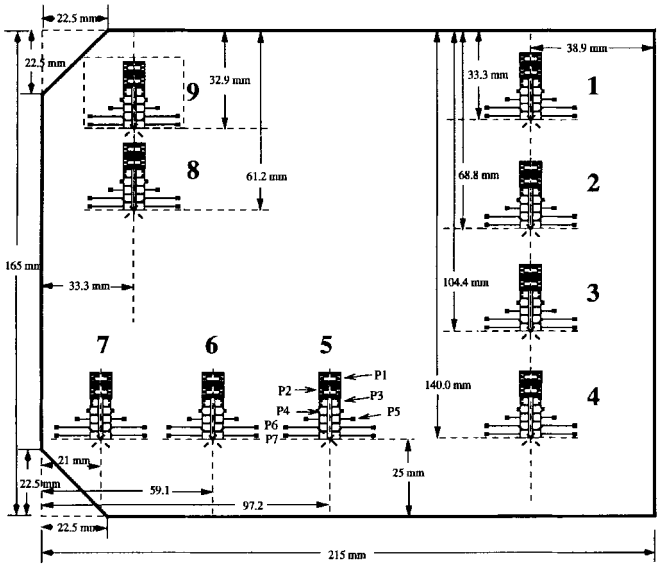

Fig. 1. Layout of the top level of the ten-layer test-board.

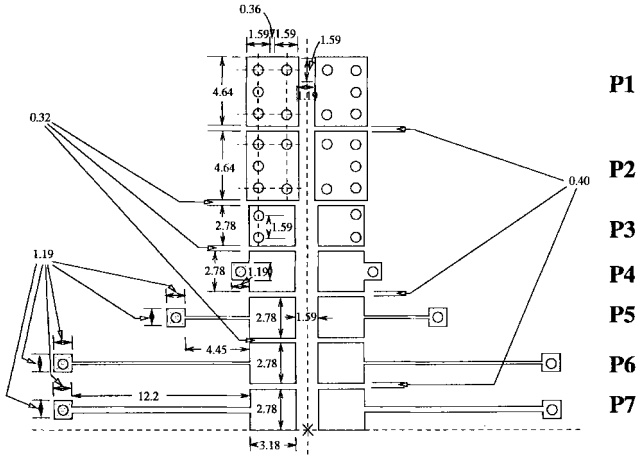

Fig. 2. A typical test pattern on the ten-layer test-board.

Fig. 2. Every pair of bounding pads are identified by the group index and the pattern labels, e.g., 6P3 is the pair of bonding pads in Group 6 and the third pattern in that group. A cross-sectional view of the test board layer stack-up is shown in Fig. 3. Two pairs of bonding pads were employed as Ports 1 and 2 in a typical S-parameter measurement. The 0.085 in semi-rigid coaxial-cable probes were attached in a manner that minimized the probe inductance, though this had little effect on the interconnect inductance measurement in practice. Any other pair of bonding pads can be investigated by mounting a decoupling capacitor on them or shorting them with a wide copper strip. In measurements with both the vector network analyzer and the impedance analyzer, calibrations were made at the connectors of the semi-rigid cable test probes, then port-extension values were set to extend the reference planes to the tips of the probes.

B. The Lumped Element Model for the Power-Bus with Interconnects

A lumped element model of the power-bus with multiple decoupling branches has been previously introduced by [8].

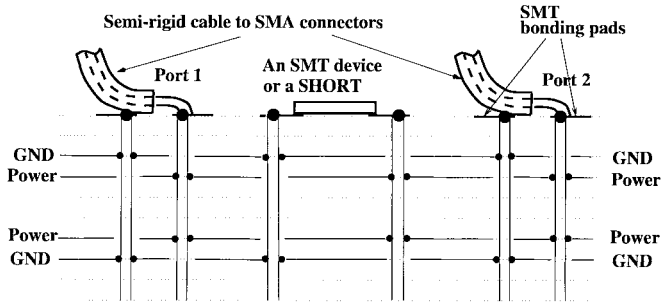

Fig. 3. The cross section of the test-board. Dotted lines represent signal planes, and the layer spacing is 10 mils.

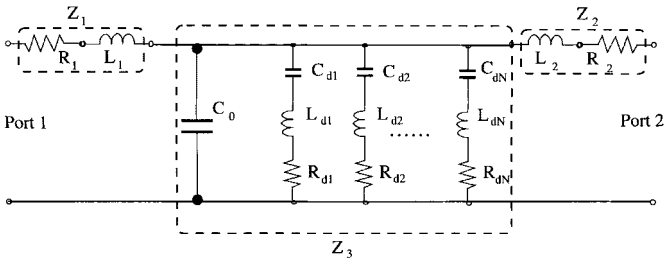

Fig. 4. The lumped element model for the PCB and test configuration.

The interplane capacitance is simply modeled by a lumped capacitor C_0. For the ith ($1 \leq i \leq N$, and $N = 63$ for the test-board) interconnect branch, the series inductance is $L_{\rm di}$ and the resistance is $R_{\rm di}$. The overall model is shown in Fig. 4 if every branch has a decoupling capacitor mounted, where $R_{1,2}$, $L_{1,2}$ are the resistances and inductances associated with probes at Ports 1 and 2, respectively, in an S_{21} measurement. In the frequency range where the interconnect inductance is measured, and the lumped element model applies, the location of a decoupling capacitor interconnect does not impact the measurement. For example, the S_{21} data shown in Fig. 5 for configuration P7 shorted and no external decoupling capacitors applied, at locations 2P7, 8P7, and 6P7 are nearly identical. In the case when the ith branch is shorted across the SMT bonding pads and no SMT decoupling capacitors are mounted, only one series branch of $R_{\rm di}$ and $L_{\rm di}$ is necessary in this model.

C. Measurement Approach

There are several factors upon which the proposed interconnect characterization procedure are based. It is intuitive to model the sets of power-ground planes by an interplane capacitance C_0. A naive calculation, with $\epsilon_r = 4.2$ and considering the two parallel plate capacitors connected in parallel for the test board considered, yields $C_0 \sim 15.1 \times 10^{-9}$ F. In general, the C_0 value of a PCB power-bus with entire planes may range from 200 pF to 0.02 μF, for typical high-speed designs, and depends on the power plane separation and total area. The range of interconnect inductance in practical designs can be estimated with a crude wire-loop model to be around $L \sim$ 0.5–15 nH [9], [10]. The proposed lumped element model is limited to frequencies such that

$$f_0 = \frac{1}{2\pi\sqrt{L_{\rm di}C_0}} \ll f_{\rm c}, \tag{1}$$

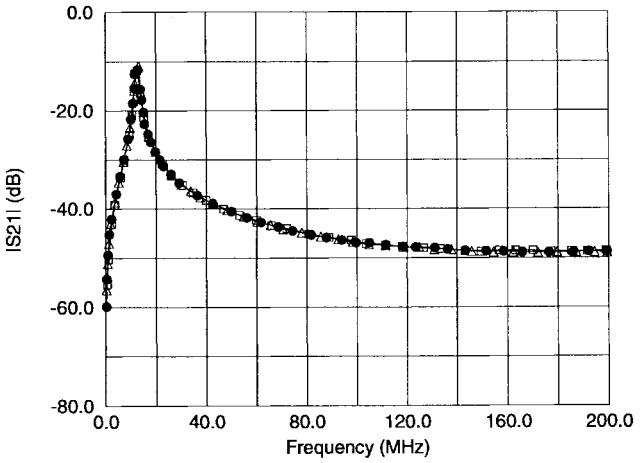

Fig. 5. Measured $|S_{21}|$ response between 9P1 and 1P1 when one of the following locations is shorted—2P7 (square), 8P7 (solid circle), and 6P7 (triangle).

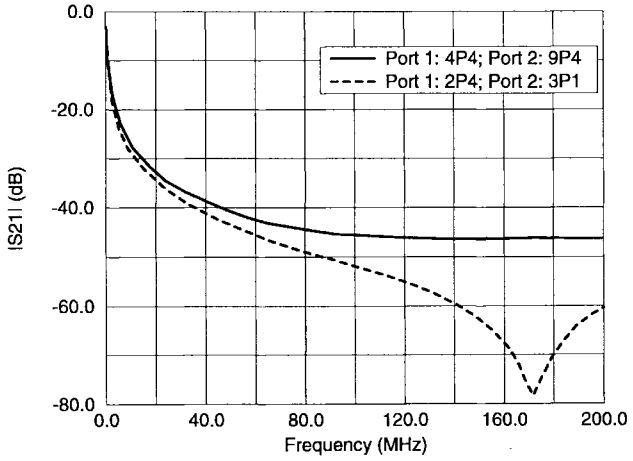

Fig. 6. Measured $|S_{21}|_{\mathrm{dB}}$ for closely-spaced probes (dashed line) and distant probes (solid line).

where f_{c} is the critical frequency, beyond which the power-bus exhibits a distributed behavior and a simple lumped element model for the planes fails. Such a condition is usually satisfied for typical designs. It should be noted that the lumped model serves merely as a vehicle to extract interconnect parameters, rather than a comprehensive model to describe the power bus response in a wide frequency range.

In the S-parameter measurements, the input impedance (Z_{in}) seen at either Ports 1 or 2 is usually much smaller than the probe characteristic impedance ($Z_0 = 50\ \Omega$) over the frequency range of interest. Since $S_{11} = (Z_{\mathrm{in}} - Z_0)/(Z_{\mathrm{in}} + Z_0)$, then $|S_{11}| \sim 1$. An inductance measurement using S_{11} requires well-characterized and precise test fixtures for locating reference plane and accurate phase information, which is difficult or expensive to achieve. In fact, only the resonant frequency manifested by a peak in $|S_{21}|$ is important in determining interconnect inductance. Consequently, $|S_{21}|$ is chosen as the primary measurable quantity. Experiments show that the S_{21} responses are consistent with a single lumped capacitance model for the V_{cc}-GND power-bus structure when the two port locations are widely spread ($\geq$0.6 L, where L is the longer side of the test-board). Anomalies are observed when the two probe locations are separated by less than 0.25 L, where the $|S_{21}|$ for the measured test board exhibits a distributed resonance (a "null") near 180 MHz. This resonance cannot be accounted for by a lumped element model, but is predicted with a full-wave analysis [6]. Increasing the probe separation, e.g., putting the two ports near the opposite ends of the board, increases the first distributed resonance to approximately 250 MHz. For the test-board, the upper frequency for the model to be valid is 200 MHz. The probe positions do not significantly impact the measured interconnect inductance values, since the resonance frequencies from which the L_{di} are determined are well below the distributed board resonance frequencies even for closely spaced probes. Fig. 6 shows the typical $|S_{21}|_{\mathrm{dB}}$ response for a bare board with two different probe spacings. Even though the first distributed "null" can vary with the probe-to-probe distance, the condition in (1) still holds.

The transfer impedance Z_{21} between two ports is a more direct indicator of the effect of a noise source on other devices through the common dc power-bus, which is related to the S-parameters by

$$Z_{21} = \left.\frac{V_2}{I_1}\right|_{I_2=0} = Z_0 \frac{2S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}}. \quad (2)$$

For most measurements involving interconnects on the power-bus, $|S_{21}|, |S_{12}| \ll 1$. Also $S_{11}, S_{22} \sim -1$. Then

$$|Z_{21}| \approx \frac{|S_{21}|}{2} Z_0. \quad (3)$$

Hence, another reason for choosing S_{21} over S_{11} is that $|S_{21}|$ is a scaled version of $|Z_{21}|$. In other words, $|S_{21}|$ is a good indicator (measurable with a network analyzer) of a noise voltage at the victim location (V_2) caused by a sudden draw of current at the source location (I_1) through the dc power-bus.

III. Experimental Characterization of Decoupling Interconnects

The interplane capacitance C_0, the branch inductance L_{di}, and the branch series resistance R_{di} (for $i = 1$ to N) must be determined in order to experimentally characterize decoupling interconnects. Further, the effect of the inductances and resistances associated with the two probes must be assessed.

A. Determination of C_0

Several possible schemes for measuring C_0 have been considered, including curve fitting S_{21} measurements (with a network analyzer), or one-port impedance measurements (with an impedance analyzer), and measurement with an LCR meter. For the test-board, the three different methods yielded $C_0 \sim$ (14.9, 14.1, 15.2) $\times\ 10^{-9}$ F, respectively. A naive parallel plate capacitor calculation and $\epsilon_r = 4.2$ yields $C_0 \sim 15.1 \times 10^{-9}$ F. For a routine power-bus characterization, a direct measurement of C_0 with a low frequency LCR meter (e.g., HP 4263B) is adequate.

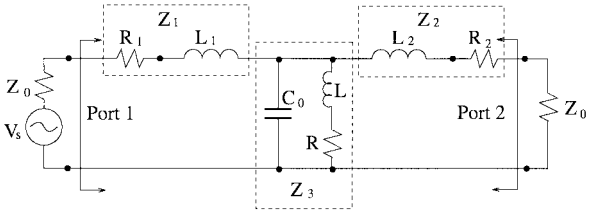

Fig. 7. A lumped element model for the PCB when one interconnect is shorted by a wide copper strip.

B. Determining the Series Inductance and Resistance of an Interconnect Branch

The series inductance and resistance of an interconnect can be determined from S_{21} and S_{11} measurements, respectively. In a sequence of measurements, the locations of the two probes were fixed such that the inter-probe distance was larger than 0.6 L, although this was not absolutely necessary for characterizing typical decoupling interconnects. A wide copper strip was used to short across the decoupling capacitor bonding pads for the ith interconnect and all others remained open-circuited. Because the contact areas with the bonding pads were large, and the shorting-strip was wide, the additional resistance and inductance of the strip were negligible. For simplicity in the following development, the branch inductance $L_{\rm di}$ and series resistance $R_{\rm di}$ will be designated L and R, respectively. The circuit model in Fig. 4 for this particular arrangement can be simplified as shown in Fig. 7. The impedance at the generator terminals is

$$\begin{aligned} Z_{\rm in}(s) &= R_1 + sL_1 + \frac{1}{sC_0 + \dfrac{1}{R+sL} + \dfrac{1}{Z_0 + R_2 + sL_2}} \\ &\approx R_1 + sL_1 + \frac{R+sL}{1+sC_0(R+sL)} \end{aligned}$$

where the approximations

$$R_1 \sim R_2, \quad |sL_2| = \omega L_2 \sim \omega L_1 \ll Z_0 \tag{4}$$

are used since $Z_0 = 50\ \Omega$, $R_{1,2} < 1\ \Omega$, $L_{1,2} \sim$ (1–15) nH, and the frequency range for the lumped element circuit model for the test-board is $\omega \leq 2\pi\times$ 200 MHz $\sim 1.3 \times 10^9\ {\rm s}^{-1}$. The applicable range of the lumped element model is approximately $D < \lambda/4$ (D is the representative board dimension) below which the distributed effects begin to manifest themselves [11]. For typical values of C_0 and interconnect inductances, the approximations are valid for most PCB's used in practice. The poles of $Z_{\rm in}(s)$ can be found as

$$s_0 = -\frac{R}{2L} \pm j\,\frac{\sqrt{1-1/(4Q^2)}}{\sqrt{C_0 L}}$$

where

$$Q \equiv \frac{\sqrt{L/C_0}}{R}. \tag{5}$$

For typical PCB board

$$Q \geq 10$$

consequently

$$s_0 \approx -\frac{R}{2L} \pm j\,\frac{1}{\sqrt{C_0 L}}.$$

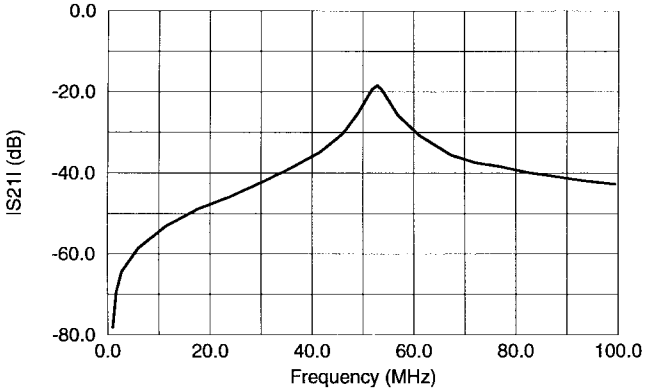

Fig. 8. A typical $|S_{21}|_{\rm dB}$ response obtained by an HP8753C network analyzer. Port 1 is at 8P1, Port 2 is at 2P1, and a SHORT is applied at 6P2.

The resonance frequency is then

$$\omega_0 = \frac{1}{\sqrt{C_0 L}}. \tag{6}$$

Thus, the peak in the $|Z_{\rm in}|$ response corresponds to

$$f_{\rm peak} = \frac{1}{2\pi\sqrt{LC_0}} \tag{7}$$

(to within 0.5% [12]), and the inductance of the interconnect is

$$L = \frac{1}{(2\pi f_{\rm peak})^2 C_0}. \tag{8}$$

The transfer impedance Z_{21} for this particular arrangement is simply [13]

$$Z_{21} = \frac{1}{j\omega C_0 + \dfrac{1}{R + j\omega L}} \tag{9}$$

which has the same pole location as $Z_{\rm in}$, implying that there is also a peak at ω_0 in the $|Z_{21}|$ response. Consequently, there is a peak at ω_0 in S_{21} as well, by virtue of (3). A typical $|S_{21}|_{\rm dB}$ measurement with probes located at 8P4 and 2P4, and 6P2 shorted is shown in Fig. 8. The probe inductances $\{L_1, L_2\}$ as well as probe resistances $\{R_1, R_2\}$ virtually always satisfy all the conditions of (4) (which will be later justified by measured results in Section IV), and have no effect on the peak frequency. Hence, even though the measurement is unfixtured, the interconnect inductance L can still be well determined.

At this point, the board capacitance C_0, and interconnect inductance have been determined from measurements. The series resistance of the decoupling capacitor interconnect can be calculated from the input impedance measured at Port 1 at the resonance frequency when the decoupling capacitor bonding pads are shorted together with a wide copper strip. A typical S_{11} measurement is shown in Fig. 9. The input impedance is related to the probe and interconnect parameters at the resonance frequency by

$$\begin{aligned} Z_{\rm in}(\omega) &\equiv R_{\rm in}(\omega) + X_{\rm in}(\omega) \\ &= R_1 + j\omega L_1 + [j\omega C_0 + (R + j\omega L)^{-1} + Z_0^{-1}]^{-1} \\ &= R_1 + j\omega L_1 \\ &\quad + \frac{1}{j\omega C_0 + (R - j\omega L)(R^2 + \omega^2 L^2)^{-1} + Z_0^{-1}} \end{aligned} \tag{10}$$

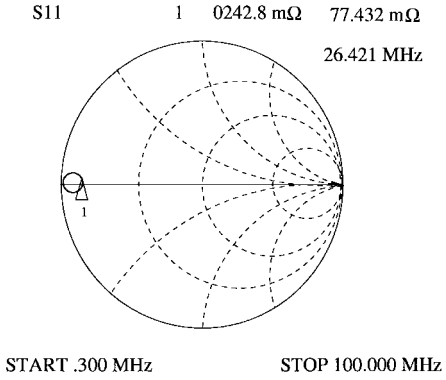

Fig. 9. A typical S_{11} Smith Chart display with an HP8753C network analyzer. Port 1 is at 8P4, Port 2 is at 2P4, and the SHORT is at 6P2.

where R_2, $|\omega_0 L_2| \ll Z_0$ are assumed. The real part of the $Z_{\text{in}}(\omega)$ is

$$R_{\text{in}}(\omega) = R_1 + [Z_0^{-1} + (R^2 + \omega^2 L^2)^{-1} R]/ \{[Z_0^{-1} + (R^2 + \omega^2 L^2)^{-1} R]^2 + \omega^2 [C_0 - (R^2 + \omega^2 L^2)^{-1} L]^2\}. \quad (11)$$

At the resonance frequency, using $\omega = \omega_0 = 1/\sqrt{LC_0}$, (11) yields

$$R_{\text{in}}(\omega_0) = R_1 + Z_0 \frac{L(C_0 R^2 + L + C_0 R Z_0)}{C_0 R^2 L + (L + C_0 R Z_0)^2} = R_1 + Z_0 \frac{1 + (R/R_v)^2 + Z_0 R/R_v^2}{(R/R_v)^2 + (1 + Z_0 R/R_v^2)^2} \quad (12)$$

where $R_v = \sqrt{L/C_0}$. The second term in R, R_v, and Z_0 can be compared to R_1 by defining the function

$$f(R, R_v) = Z_0 \frac{1 + (R/R_v)^2 + Z_0 R/R_v^2}{(R/R_v)^2 + (1 + Z_0 R/R_v^2)^2}. \quad (13)$$

It will be demonstrated below by plotting $f(R, R_v)$ graphically that for practical values of R and R_v

$$R_1 \ll f(R, R_v). \quad (14)$$

The domain of $f(R, R_v)$, for typical values of R, L, and C_0, is 0.001 $\Omega \le R \le 1\ \Omega$ and 0.01 $\Omega \le R_v \le 10\ \Omega$. A contour plot of the function $f(R, R_v)$ is shown in Fig. 10 over this domain, and $f(R, R_v)$ values are marked on several equal-value contours in the R–R_v plane. The two dashed lines in Fig. 10 correspond to two conditions that are typically satisfied

$$R_v > 10R, \quad R_v < \sqrt{RZ_0}. \quad (15)$$

The dark solid line marks a realistic limit $R > 5$ mΩ. The triangular region enclosed by these three constraints correspond to an $f(R, R_v)$ value greater than 500 mΩ. In practice, R_1, which is the probe resistance associated with the connector to the power planes is expected to be slightly greater than those of an interconnect (Table I) and still much less than 500 mΩ, which leads to $R_1 \ll f(R, R_v)$. Thus, the interconnect resistance can be determined by solving the

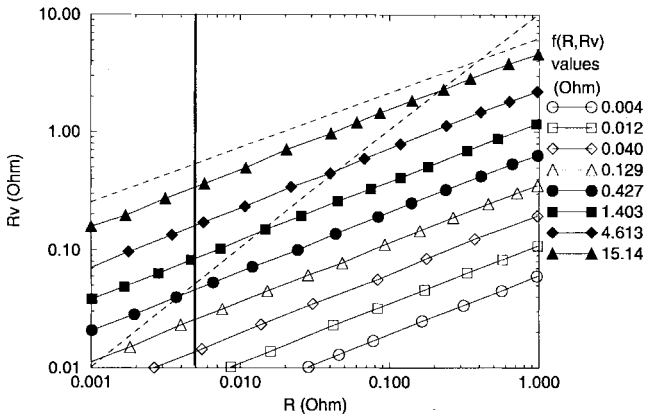

Fig. 10. A contour plot of $f(R, R_v)$.

TABLE I
INDUCTANCES AND RESISTANCES ASSOCIATED WITH TRACES/VIAS FOR THE BONDING PADS DETERMINED WITH THE IMPEDANCE ANALYZER (1) AND THE NETWORK ANALYZER (2)

	$L^{(1)}$(nH)	$R^{(1)}$(mΩ)	$L^{(2)}$(nH)	$R^{(2)}$(mΩ)
P2	0.64	12.8	0.61	11.9
P3	1.44	18.5	1.33	15.5
P4	2.15	22.6	2.05	19.9
P5	7.13	51.7	6.79	48.2
P6	15.6	88.4	14.5	82.3
P7	10.4	55.3	10.1	54.4

quadratic equation

$$R_{\text{in}}(\omega_0) = f(R, R_v) = Z_0 \frac{1 + (R/R_v)^2 + Z_0 R/R_v^2}{(R/R_v)^2 + (1 + Z_0 R/R_v^2)^2} \quad (16)$$

where both C_0 and L have been previously obtained.

C. Characterizing a PCB Power-Bus with an Impedance Analyzer

A multilayer PCB dc power-bus can also be characterized by precision one-port measurements with an HP4291A impedance analyzer. For a bare board, the impedance seen at any interconnect (where the probe is mounted) is

$$Z_{\text{in}} = R_{\text{p}} + j\omega L_{\text{p}} + \frac{1}{j\omega C_0}. \quad (17)$$

Here, $\{R_{\text{p}}, L_{\text{p}}\}$ are the resistance and inductance associated with the probe and interconnect. A typical input impedance measurement for a bare board is shown in Fig. 11. The impedance analyzer provides a curve fitting option for determining a lumped element model from the measured response. Making Z_{in} measurements at eight (or any other number that is perceived as a good for statistical sampling) different port locations, the average measured interplane capacitance is $C_0 = 14.1 \times 10^{-3}$ μF. There is a 0.1×10^{-3} μF variation from location to location in the measurement results, which is attributed to the small differences in the probe connections. To a good approximation, C_0 can be considered to be independent of location. Once C_0 is found, the inductance and resistance $\{R_{\text{p}}, L_{\text{p}}\}$ of a specific decoupling capacitor interconnect can be determined by shorting the bonding pads of the interconnect of concern with a copper strip. A typical measurement for this

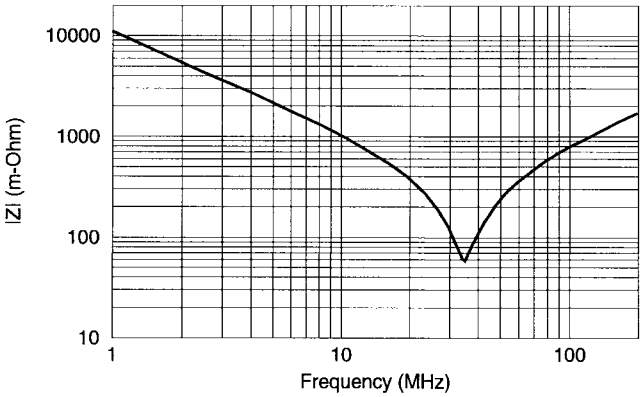

Fig. 11. A typical measurement of $|Z_{\rm in}|$ for a bare board with an HP4291A impedance analyzer.

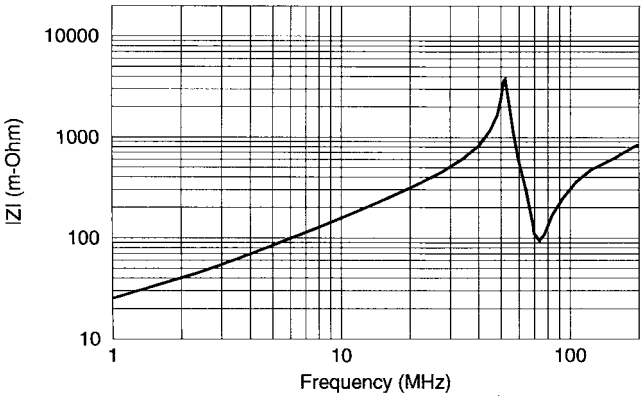

Fig. 12. A typical measurement of $|Z_{\rm in}|$ with an HP4291A impedance analyzer when one decoupling capacitor interconnect is shorted.

configuration is shown in Fig. 12. The input impedance seen at the probe terminals is

$$\begin{aligned} Z_{\rm in} &= R_{\rm p} + j\omega L_{\rm p} + \frac{1}{j\omega C_0} \Big/\Big/ (R + j\omega L) \\ &= [(L_{\rm p} L C_0)(j\omega)^3 + (L R_{\rm p} C_0 + L_{\rm p} R C_0)(j\omega)^2 \\ &\quad + (L_{\rm p} + L + R_{\rm p} R C_0)(j\omega) + (R_{\rm p} + R)]/ \\ &\quad [1 + (j\omega) R C_0 + (j\omega)^2 C_0 L]. \end{aligned} \tag{18}$$

The denominator is a quadratic polynomial with a natural resonance frequency

$$f_{\rm n} = \frac{1}{2\pi\sqrt{C_0 L}} \tag{19}$$

and quality factor

$$Q = \frac{\sqrt{L/C_0}}{R}. \tag{20}$$

When $Q > 10$, the peak in the $|Z|$ response is $f_{\rm peak} \approx f_{\rm n}$ to within 0.3% [12], and the interconnect inductance is

$$L = \frac{1}{(2\pi f_{\rm peak})^2 C_0}. \tag{21}$$

Also

$$|Z|_{\max} = \sqrt{\left(R_{\rm p} + \frac{L}{RC_0}\right)^2 + \left(\frac{L_{\rm p}}{\sqrt{LC_0}} - \sqrt{\frac{L}{C_0}}\right)^2} \tag{22}$$

and the interconnect resistance can be solved for as

$$R = \frac{L}{C_0\left[\sqrt{|Z|^2_{\max} - \left(L_{\rm p}/\sqrt{LC_0} - \sqrt{L/C_0}\right)^2} - R_{\rm p}\right]}. \tag{23}$$

Thus, characterizing the interconnect with an impedance analyzer is a straight-forward process.

IV. Experimental and Simulation Results

The results from four measurements using different probe locations using the HP4291A impedance analyzer were repeatable to within 1% for C_0, 2% for all L values, and 5% for all R values. In using the HP8753C network analyzer, the results were repeatable to within 4% for all L values and 6% for all R values. The measured values of Ls and Rs for the different interconnect configurations using both methods are given in Table I. Bonding pads P1 and P2 have identical configurations, so only data for P2 are listed. The discrepancies between the measured values using the two methods were less than 7% for L values, and 2–15% for R values. The experimental results demonstrate that characterizing a dc power bus (entire planes) of a multilayer PCB with a network analyzer can yield results for the interconnect inductance and resistance, very close to those measured with a precision impedance analyzer. The conditions in (4) evaluated for the measured values of interconnect inductance and resistance are tabulated in Table II. For all cases, $Q > 10$. Hence, the approximations made in developing the measurement procedures are satisfied.

TABLE II
The Q Factor Calculated from the Measured (with HP4291A Impedance Analyzer) Interconnect $\{L, R\}$ Parameters. C_0 = 0.0141 μF

	L (nH)	R (mΩ)	Q
P2	0.64	12.8	16.5
P3	1.44	18.5	17.2
P4	2.15	22.6	17.2
P5	7.13	51.7	13.7
P6	15.6	88.4	11.8
P7	10.4	55.3	15.5

The experimentally determined lumped element parameters were used then to simulate the PCB response with multiple decoupling capacitors. The lossy X7R SMT decoupling capacitors employed were modeled as a series RC branch, and the internal resistance was determined by precision impedance measurements with the HP 4291 Impedance Analyzer and HP 16 192A SMT test fixture. Interconnect inductance and resistances were characterized as previously described. Three cases were studied with 8P4 as Port 1 and 2P4 as Port 2: 1) The bare-board. 2) A 0.1 μF SMT decoupling capacitor (40 mΩ internal resistance) connected at 6P4, and a 0.01 μF decoupling capacitor (110 mΩ internal resistance) connected at 5P4. 3) A 0.1 μF decoupling capacitor (40 mΩ internal resistance) mounted at 6P4, and four 0.01 μF decoupling capacitors (100 mΩ nominal internal resistance) mounted at 3P4, 4P4, 6P4, and 7P4, respectively (L = 2.17 nH for all). The simulated $|S_{21}|$ results, using the lumped element model and independently determined element parameters, are plotted together with the measured data in Fig. 13. In all three cases, the parallel (maximums in the $|S_{21}|$ response) and series

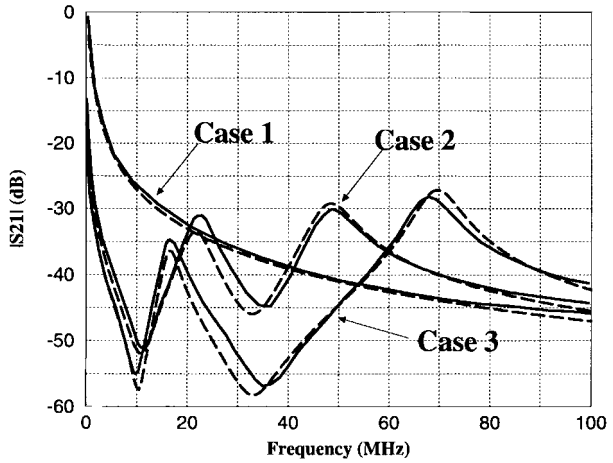

Fig. 13. Measured $|S_{21}|_{\mathrm{dB}}$ (dashed lines) for three different decoupling cases and simulated results (solid lines) with a lumped model.

(minimum in the $|S_{21}|$ response) resonance frequencies of the lumped element model agree with the measurement to within 3%. Overall, the agreement in the magnitude is satisfactory. These results further support the measurement procedure and the use of the lumped element model upon which it is based.

V. Conclusion

This study indicates that the interconnects for multilayer PCB dc power-buses employing entire planes can be accurately characterized by a precision impedance analyzer, or by a network analyzer. The values measured by the network analyzer are within 7% for inductance and 15% for resistance of measurements with a precision impedance analyzer. For both methods, the quality factor ($Q = \sqrt{L/C_0}/R$) of each interconnect needs to be greater than 10, which is generally the case.

Although the power-bus model employed in this study is only valid up to 200 MHz—below the distributed resonances of the test-board, the L and R parameters determined through the procedure presented can be used in more sophisticated power-bus models [6], [11] over a broader frequency range. The electrical length of the interconnects are typically small compared to a wavelength at the highest frequency of interest, and the behavior of an interconnect can be adequately modeled by a series inductance and resistance. Besides the test-board detailed above, the procedure detailed herein has been applied for characterizing several real-world power-bus designs including CPU daughter cards and computer mother-boards.

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Thomas P. Van Doren (M'85), for a photograph and biograpy, see p. 155 of the May 1997 issue of this Transactions.

Todd H. Hubing (S'82–M'82–SM'93), for a photograph and biograpy, see p. 155 of the May 1997 issue of this Transactions.