Reducing Power Bus Impedance at Resonance with Lossy Components

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ABSTRACT

Power bus structures in printed circuit boards with solid power and ground planes exhibit resonances. When the power bus is resonant, the power bus impedance can increase dramatically. This paper explores the effect of component equivalent series resistance (ESR) on power bus resonances. General guidelines for selecting an optimum ESR are provided and are supported by laboratory measurements and numerical simulations.

INTRODUCTION

At resonance, the power bus impedance of printed circuit boards with solid copper planes can be relatively high. To reduce the power bus impedance at resonance, the quality factor of the power bus must be reduced. This can be accomplished by adding loss to the system. Many loss mechanisms exist within a printed circuit board power bus, including radiation loss, dielectric loss, conduction loss and component loss. Typically, radiation loss and dielectric loss do not provide enough damping to completely eliminate resonances. Conduction loss can completely damp power bus resonances if the power planes are closely spaced [1], but manufacturing boards with closely spaced power planes can be expensive and is not always a good solution. If the power planes are widely spaced (e.g. >0.1 mm [1]), conduction loss will not be great enough to completely damp resonant peaks in the impedance. In a few cases, component losses have been shown to damp power bus resonances significantly.

A transmission line grid model was used to compute the input impedance of various power bus geometries. With this method, the power bus is modeled as a grid of small, lossy transmission line segments [2]. Each segment of the grid contains resistive elements, representing conductive and dielectric loss. Components connected to the power bus, like decoupling capacitors and integrated circuits, can be included in the model by adding the component's admittance to the appropriate grid point of the model. Conductive, dielectric and component loss can be modeled accurately with this technique. Radiation loss is not modeled, but this loss mechanism is typically insignificant compared to the other loss mechanisms in a printed circuit board [1], [3].

The input impedance of a typical power bus is shown in Fig. 1. The large peaks in the impedance correlate to resonant frequencies of the power bus. The quality factors of the resonant peaks can be calculated using:

$$Q = \frac{f_0}{BW} \tag{1}$$

where f_0 is the resonant frequency and BW is the 3-dB bandwidth of the resonant peak.

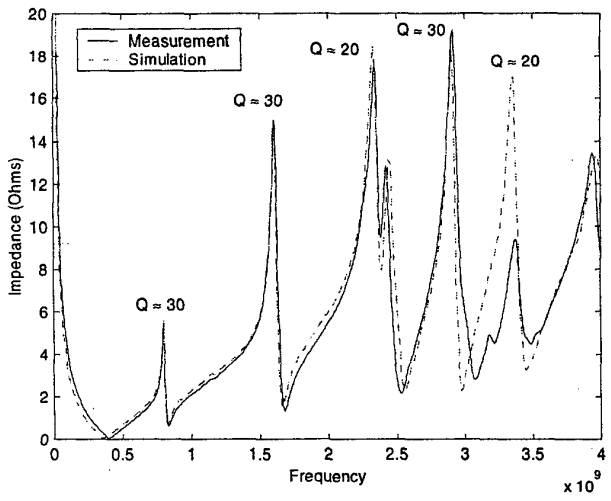

Fig. 1. The power bus impedance of an unpopulated test board.

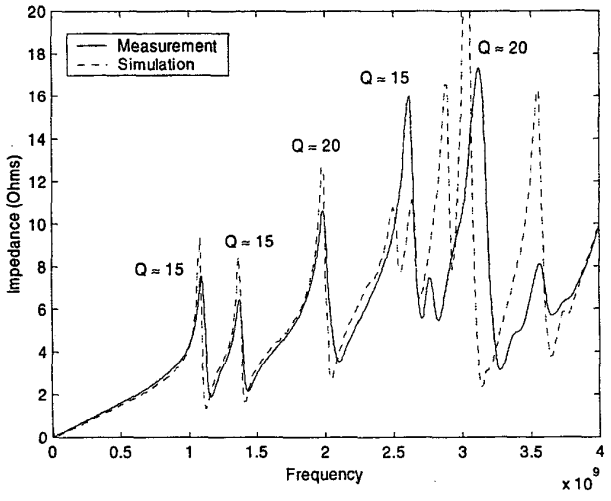

Fig. 2. The power bus impedance of the test board populated with decoupling capacitors.

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The test boards used for this study were 72 mm by 50 mm large, and the dielectric was 19.4 mils thick with an effective relative dielectric constant, ε_{reff}, equal to 6.78 and a loss tangent equal to 0.020. The measurement port was at (46,26) mm. Several test boards with identical layouts were constructed, each having a different number of components mounted on them. The fully populated test board had 8 octal clock drivers, with loaded outputs. There were 33 10-nF capacitors and one 22-μF capacitor to provide decoupling. The remaining test boards had identical layouts, but fewer mounted components. One test board had only decoupling capacitors mounted, another one had only integrated circuits mounted, and one was completely unpopulated. The power bus impedance of the test boards was measured in the laboratory with an HP8753D network analyzer.

The unpopulated test board was modeled using a transmission line grid. The simulation results are compared to the measured results in Fig. 1. The quality factors at the first few resonant frequencies are indicated in the figure. For this test board, conductive and dielectric losses do not lower the quality factor enough to significantly damp the power bus resonances.

A second test board, one with only decoupling capacitors mounted, was measured and modeled. Each of the 33 decoupling capacitors had a mounted equivalent series inductance (ESL) of 1.1 nH, and an equivalent series resistance (ESR) of 100 mΩ. The ESL and ESR of the mounted capacitors were determined from a power bus impedance measurement of an unpopulated board with one mounted capacitor [4]. The results are shown in Fig. 2. The decoupling capacitors tend to shift the resonant peaks of the power bus impedance, but the peak power bus impedance at resonance is not significantly reduced. As configured, the decoupling capacitors do not supply enough loss to significantly damp the power bus resonances.

The third test board, the board with only the integrated circuits mounted, was measured with the network analyzer. The results are shown in Fig. 3. The integrated circuits on this test board provide enough loss to significantly damp most of the resonant peaks. The quality factors of each resonant peak are indicated in the figure.

To reduce the impedance even further, new lossy components could be added or existing components could be modified. A procedure for adding new components to increase component loss has been investigated before [2]. This work will focus on modifying existing components on the board to enhance component loss, specifically, modifying the ESR of existing decoupling capacitors.

Optimizing Component Loss

Once approach that can be used to compute the optimum ESR each capacitor should have, is to calculate the equivalent average resistance between the power planes, needed to attain a particular quality factor. The quality factor of a cavity filled with a dielectric material is related to the loss tangent as [5], [6]:

$$Q = \frac{1}{\tan \delta} \tag{2}$$

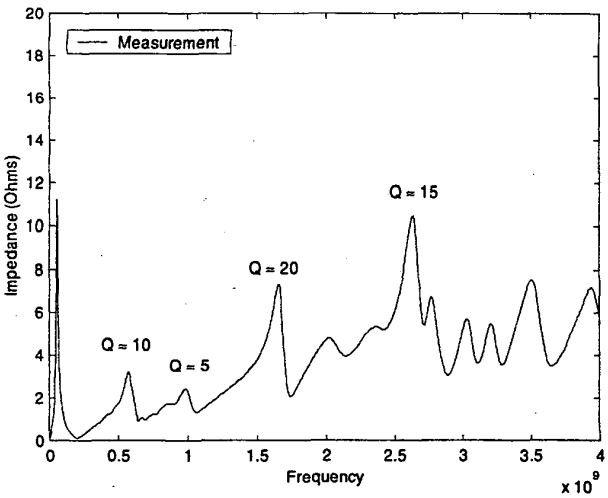

Fig. 3. The power bus impedance of the test board populated with integrated circuits only.

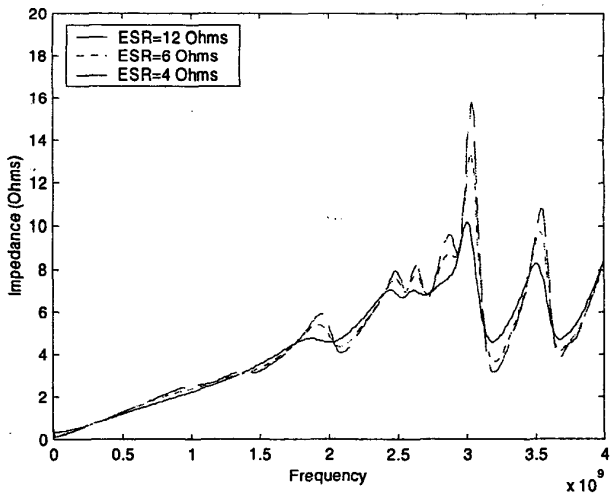

Fig. 4. The power bus impedance of the test board, populated with capacitors with an ESL = 1.1 nH.

and the loss tangent is related to the conductivity of the dielectric material as

$$\tan\delta = \frac{\sigma}{2\pi f \varepsilon_{reff} \varepsilon_0} \tag{3}$$

where σ is the conductivity of the dielectric material between the power planes, f is the frequency, ε_{reff} is the effective relative permittivity of the dielectric and ε_0 is the permittivity of free space. The resistance across a material with a cross-sectional area A, a depth h, and a conductivity σ, is given as:

$$R_{eqv} = \frac{h}{A\sigma}. \tag{4}$$

Substituting (4) into (2) and (3) yields the equivalent distributed resistance, R_{eqv}, that is needed to get a quality factor, Q, at a given frequency, f:

$$R_{eqv} = \frac{Qh}{2\pi f \varepsilon_r \varepsilon_0 A}. \tag{5}$$

If more than one lossy component is added to the power bus, then the value of the resistance in each component, R_N, should be equal to:

$$R_N = NR_{eqv} \tag{6}$$

where N is the number of equal-valued resistive components added to the power bus. As more resistive elements are added to the power bus, the optimum resistance of each component, R_N, increases.

For the test board, the equivalent distributed resistances required to obtain a quality factor of 1 at 1 GHz and 3 GHz are 0.36 Ω and 0.12 Ω respectively. According to (6), with 33 decoupling capacitors on the test board, the ESR of each decoupling capacitor on the test board should be 33 times R_{eqv} (12 Ω and 4 Ω at 1 GHz and 3 GHz, respectively). A numerical simulation of the test board with modified decoupling capacitors is shown in Fig. 4. As configured, the power bus is not damped enough to lower the resonant peaks. The reason the calculated value of R_N is not effective is that the ESL of the decoupling capacitors is too high. At 3 GHz, the magnitude of the inductive reactance, Z_L, is approximately 21 Ω. With this ESL, the reactive impedance of each decoupling capacitor is significantly larger than the optimum ESR and very little power can be dissipated in the components.

To determine the usefulness of (5) as a means of determining the optimum ESR, the ESL of the decoupling capacitors was changed from 1.1 nH to 0.1 nH. This way, the inductive impedance, Z_L, is lower than R_N up to several GHz. The results of this change are shown in Fig. 5. The solid curve in Fig. 5 shows the power bus impedance when the optimum value of ESR at 3 GHz (4 Ω) is used. As shown in Fig. 5, the power bus resonances can be significantly damped using the value for R_N calculated in (5) as long as the connection inductance impedance (Z_L) is less than R_N.

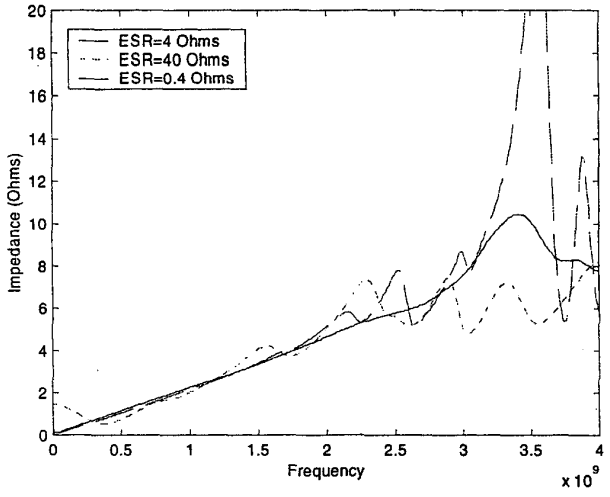

Fig. 5. The power bus impedance of the test board, populated with capacitors of different ESR and an ESL = 0.1 nH.

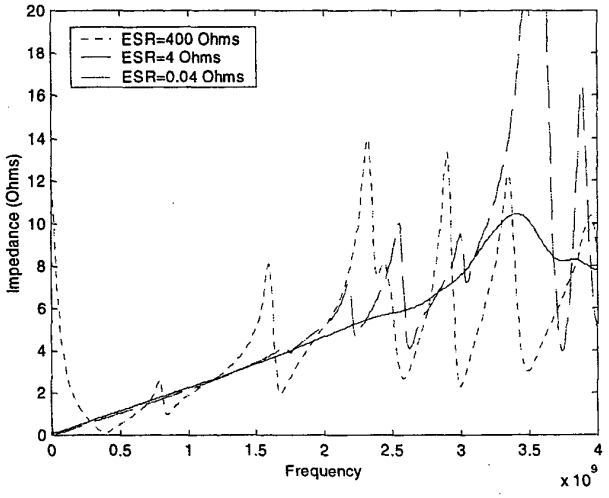

Fig. 6. The power bus impedance of the test board, populated with capacitors of different ESR and an ESL = 1.1 nH.

The other two curves in Fig. 5 show the power bus impedance when non-ideal values of the ESR are used. For values of ESR that are a factor of 10 higher than optimum, (5) suggests that the Q of the resonance will be about 10. We might also expect the same to be true for values of ESR that are a factor of 10 lower than optimum. Assuming 4 Ω $(Q \approx 1)$ is optimum for our test board, we would then expect boards with ESR = 40 Ω and ESR = 0.4 Ω to exhibit resonant peaks with Q's on the order of 10. This expectation is confirmed by the curves in Fig. 5. If the ESR is a factor of 100 higher or lower than the optimum value of ESR, then (5) suggests the Q should be much higher. In Fig. 6, the power bus impedance with ESR = 400 Ω and with ESR = 0.04 Ω is shown. The curves in Fig. 6 support this expectation.

For the boards used in this study, the ESL (1.1 nH) was too high for capacitors with a 4-Ω ESR to be effective. One solution would be to use a larger number of decoupling capacitors. However, the number of capacitors (33) was already high for a board this size. When $|Z_L| > R_N$, a maximum amount of power will be dissipated through the capacitor by setting the ESR equal to $|Z_L|$ [7]. In this situation, it is no longer possible to completely damp the resonances. The optimum value of ESR is determined by the connection inductance and is independent of the number of decoupling capacitors on the board.

For the test board in this study, at 3 GHz, $|Z_L|$ is approximately 20 Ω, so the best choice of ESR is 20 Ω. Simulations of the original test board are shown in Fig. 7 with an ESR of 20 Ω. With this ESR, the power bus impedance is lower than the power bus impedance of the original test board and the board with ESR equal to R_N.

CONCLUSIONS

Component losses have the potential to reduce power bus impedance. To optimize component loss, the equivalent series inductance of each component must be taken into consideration. For components uniformly distributed on a board's surface, the optimum value of ESR is R_N as determined by (5) and (6) provided the connection inductance impedance, $Z_L = j\omega(\text{ESL})$, is small relative to R_N.

If $|Z_L|$ is greater than or equal to R_N, then the maximum damping is achieved by setting the ESR equal to $|Z_L|$. However, if $|Z_L|$ is too large relative to R_N, the component losses will not damp power bus resonances significantly. The ESL may be lowered by changing the package size or by improving the connection between the component and the power bus. The value of R_N can be increased by adding more lossy components to the design.

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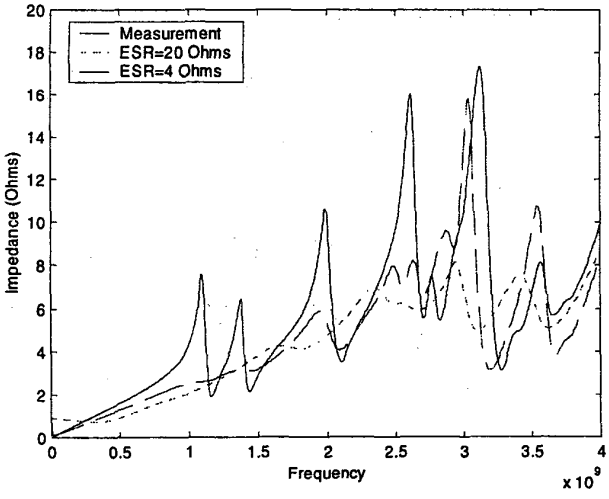

Fig. 7. The power bus impedance of the test board, populated with capacitors with an ESL = 1.1 nH.

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