Plate Orientation Effect on the Inductance of Multi-Layer Ceramic Capacitors

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***Abstract*—Various multi-layer ceramic capacitor (MLCC) geometries with horizontally and vertically oriented plates are modeled to determine the equivalent series inductance. It shows that the plate stack location and dimensions (independent of plate orientation) are the most significant factors affecting the inductance.**

Keywords-ESL, MLCC, electrode geometry

I. INTRODUCTION

In high-speed circuits, the value of the inductance associated with a connection to a MLCC (Multiple-Layer Ceramic Capacitor) is often more important than the nominal value of the capacitor. ESL (Equivalent or Effective Series Inductance) is a value often quoted in capacitor data sheets for the purpose of comparing different capacitor designs. However, the actual connection inductance for small SMT capacitors depends on several parameters that are not part of a typical ESL measurement. The actual high-speed performance of an SMT capacitor is generally unrelated to its nominal ESL. Capacitors that are designed to have the lowest ESL may not be the best capacitors to use in a particular application. In the research reported here, the effect of electrode (plate) orientation on the connection inductance of MLCC capacitors is investigated. It is shown that a single vertical plate has a higher inductance than a single horizontal plate when mounted over a board with a ground plane. However, as more vertically oriented plates are stacked side by side, the value of the self inductance decreases significantly, whereas the inductance of horizontal plates that are vertically stacked is relatively independent of the number of plates in the stack. For large stacks, the overall width of the stack is the most significant parameter affecting the connection inductance. When the width and height of the stacked plates is the same, the effective inductance with either plate orientation was the same. Thus capacitors with vertically oriented multiple plates do not inherently provide an advantage over capacitors with horizontally oriented multiple plates. The primary capacitor geometry parameters that affect the connection inductance are the plate stack width (which should be maximized) and the loop area associated with current flowing up into and back out of the capacitor plates (which should be minimized). The following sections report the results of modeling various multi-layer ceramic capacitor (MLCC) geometries with horizontally and vertically oriented plates. The purpose of these models is to determine the effect that plate orientation has on a capacitor's high-frequency inductance.

II. MODELING RESULTS

A. 2D Modeling of Horizontal and Vertical Plates

Two-dimensional models were used to isolate the contributions of the plates from the contributions of the end caps to the overall connection inductance. These models are illustrated in Fig. 1. The simulation of the self-inductance of a single plate over a ground plane was performed using a 0.4342 mm by 0.0342 mm plate located 0.0829 mm over a ground plane. The calculated inductance per unit length values were multiplied by a length of 0.94 mm (corresponding to a 0402 capacitor package) to give a value for the "partial" inductance associated with the plates.

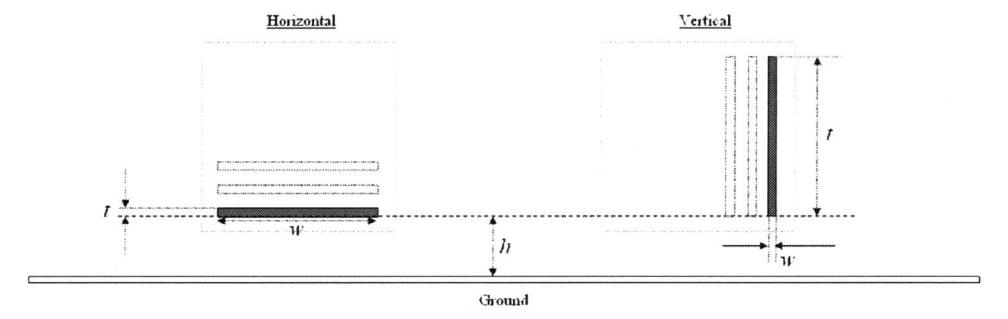

Fig. 1. Cross-section view of the two-dimensional plate geometry.

As the results in Table I indicate, the effective inductance of a vertically oriented single plate is significantly higher than that of a horizontally oriented plate. As the current spreads across the surface of the vertically oriented plate, the loop area formed between the plate current and the ground current increases. The horizontal plate provides the lowest inductance current path for a given height, h and plate surface area.

TABLE I

Comparison of the effect of the orientation of a single plate (l=0.94mm)

	Self Inductance (Plate)	Mutual Inductance (GND-to-Plate)	Loop Inductance (SI – MI)
Horizontal Plate	0.89976 nH	0.77172 nH	0.1280 nH
Vertical Plate	0.97186 nH	0.75017 nH	0.2217 nH

B. Modeling Stacked Plate Pairs as Blocks

Since this study is focused on the inductance characteristics of a decoupling capacitor, the models used for this analysis short the positive and negative electrodes together where the plates overlap. This allows the current to spread out over the plates in the same way that it would at high frequencies, while eliminating the capacitive reactance from the models. Plate pairs are represented as solid conducting "blocks" as illustrated in Fig. 2. The inductance values of the MLCCs are determined by the three primary dimensions of the structure, w, t, and l denoting the width, thickness, length of the stacked plate respectively.

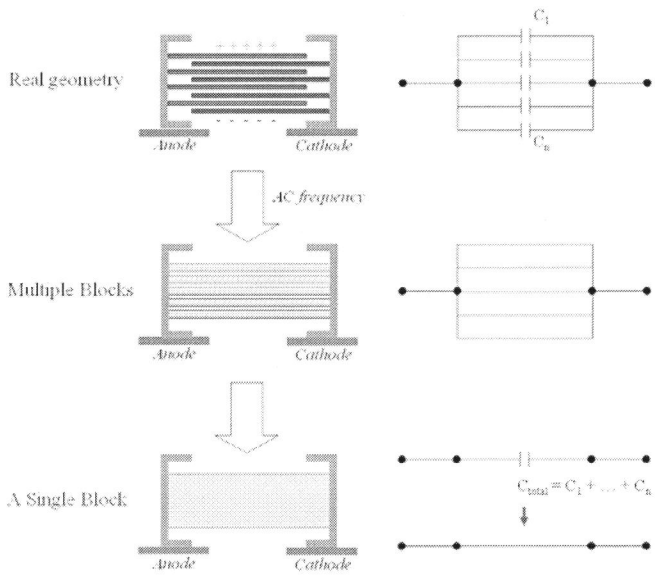

Fig. 2. Simplified inductance models for MLCCs.

C. Effect of the Dimensions of a Single Block on the Inductance

Although the inductance of a single plate is higher when the plate is oriented vertically, this inductance decreases as we add more plates in parallel. Single horizontal plates have lower inductance, but stacking more plates on top of the first one has little effect on the high-frequency inductance. To illustrate this, we use the model on the left side of Fig. 3. The parameters of a 2D single block were varied to determine the effect of the plate stack size and orientation on the capacitor inductance. A "block" in this model represents a pair of internal electrodes forming the capacitor structure for AC current flow. The ground conductor under the blocks was an ideal ground plane. For the research reported here, the stack size (t for the horizontal blocks and w for the vertical blocks) was increased from 1 to 11 block thicknesses. A single block thickness was 0.0342 mm. The height of the block above the plane was 0.0829 mm.

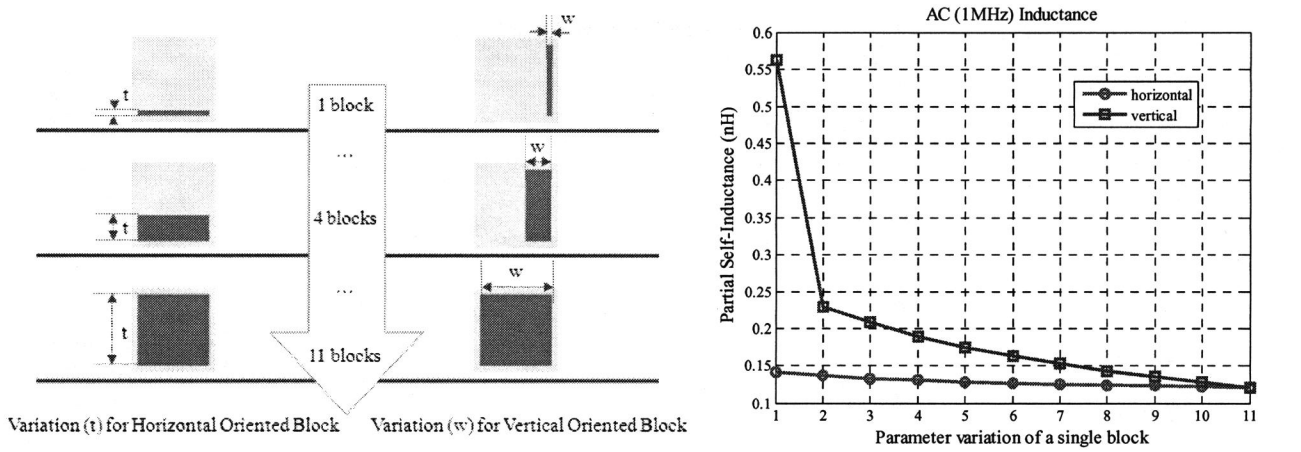

Fig. 3. Left: Parameter variation of a single block. Right: Inductance as the stack size increases.

As can be seen in Fig. 3, the self-inductance of the vertically oriented block is much higher than that of the horizontally oriented block. As the number of blocks increases, the inductance of the vertically oriented blocks decreases significantly. However, the inductance of the horizontal blocks shows little change as the number of blocks increases.

D. 3D Modeling for Analyzing Effective Inductance

Fig. 4 illustrates a 3D model for a MLCC. It is not possible to quantify a meaningful inductance for this structure without specifying a test fixture that completes the current loop. Therefore, a 3D structure for extracting effective inductance was used in this study. The structure consisted of a two-layer printed circuit board with an input port and a capacitor mounting port as illustrated in the right side of Fig. 4.

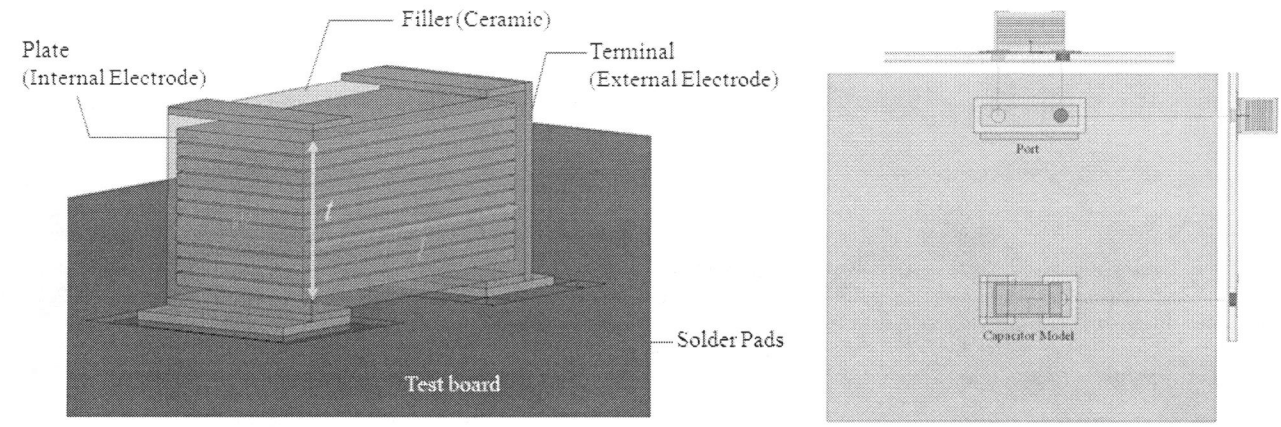

Fig. 4. Left: 3D MLCC model. Right: Top and side view of a 3D model for the mounting fixture.

Ansoft Q3D extractor™ was to determine the effect of the stack size on the effective inductance. The AC frequency was set to 1 GHz. The number of blocks was increased from 1 to 11 with a slight dielectric gap between adjacent blocks in both orientations as illustrated in Fig. 5. The stack order was from bottom to top for the horizontal orientation and from right to left for the vertical orientation. The effective inductance of a vertically oriented block was higher than that of a horizontally oriented block just as it was in the 2D simulation results. As the number of blocks increased so that the outer dimensions of the stacks were the same, the effective inductances approached the same value for both block orientations as shown in the right side of Fig. 5.

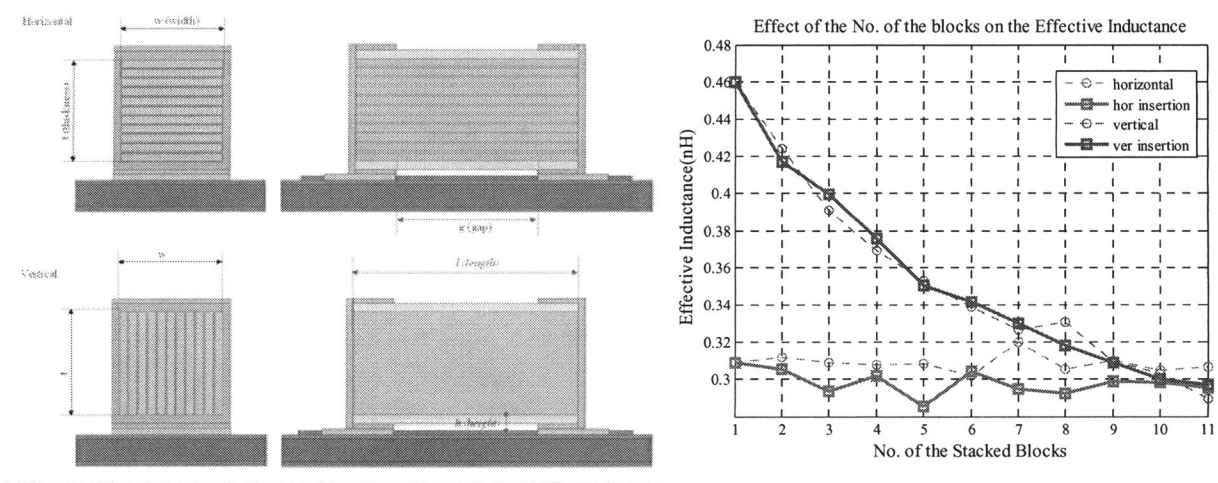

Fig. 5. Left: Three-dimensional view of multiple blocks. Right: Effective inductance by the number of blocks.

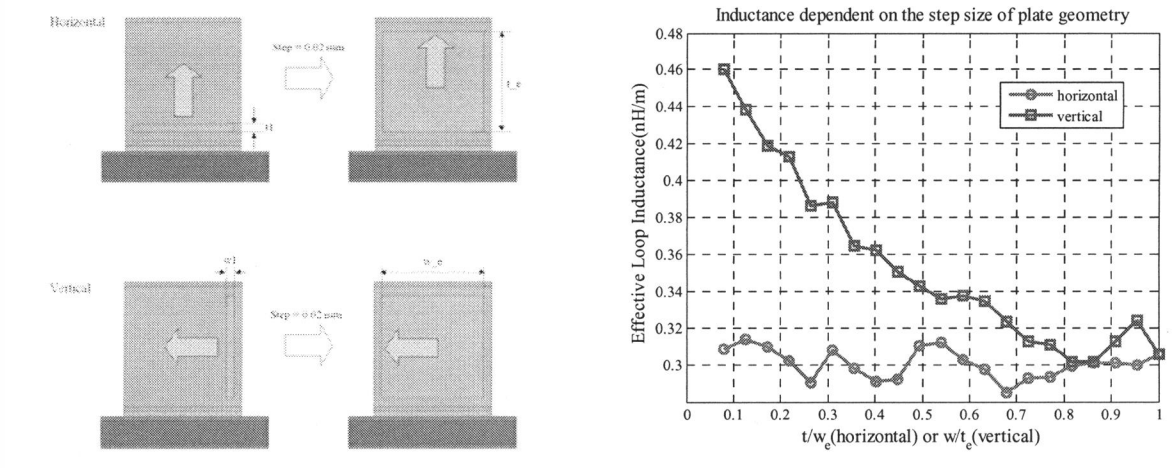

Fig. 6. Left: Parameter variation of a 3D single block. Right: Effective inductance as a function of stack size.

E. Effect of the Dimensions of a Single Block on the Effective Inductance

This process was repeated without the dielectric gaps between blocks as illustrated in the left side of Fig. 6. The effective inductance of a single block was analyzed as a function of the parameters t or w. The stackup size was incremented in 0.02-mm steps, with the final dimension being denoted as t_e or w_e. As shown in Fig. 6, the results mimic the results obtained with the dielectric between each block. For the horizontal orientation, as the height, t, increased, the effective inductance varied little. For the vertical orientation, the effective inductance decreased as the width of the stackup increased.

III. CONCLUSIONS

The results here demonstrate that a vertically oriented single plate has higher inductance than a horizontally oriented single plate. The simulation of multiple plates indicates that as more vertically oriented plates are stacked to increase the overall width of the capacitor, the value of the capacitor's inductance decreases. Stacking horizontal plates vertically has relatively little effect on the inductance, since most of the high frequency current flows only on the lower plate. The inductance of the plate stack was primarily a function of the width and height of the stack and relatively independent of the plate orientation. Therefore, the capacitor designs with vertically oriented multiple plates do not necessarily provide an advantage over designs with horizontally oriented multiple plates in terms of providing the lowest possible ESL.

REFERENCES

[1] Andrew P. Ritter and Roberto N. Garrafa, "Low Inductance Land-Grid Array Decoupling Capacitors," IMAP 2006