

Incorporating Vertical Discontinuities in Power-Bus Modeling using a Mixed-Potential Integral Equation and Circuit Extraction Formulation

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Abstract

Noise on the DC power-bus attributed to device switching is among the primary sources of EMI and signal integrity problems. A mixed-potential integral equation formulation with circuit extraction approach is used to model the planar multi-layer power-bus geometry, which can also include arbitrary shaped power regions on multiple layers. Incorporating vertical discontinuities, e.g., decoupling capacitor interconnects, is a critical aspect of the modeling, and must be done properly since they are included as a lumped element model and not a part of the MPIE formulation. Agreement with experimental results demonstrate the present approach.

I. Introduction

Multi-layer printed circuit boards (PCBs) are commonly used in high-speed digital design, where the DC power is distributed to all the attached devices through a power-bus structure consisting of at least one pair of ground and power planes. As a known source of electromagnetic interference (EMI) and signal integrity (SI) problems, the power-bus structure is a critical design aspect in mitigating the simultaneous switching noise (SSN) that contributes to these problems.

Though many design issues can be investigated at the hardware level, the knowledge gained may be limited to specific cases. A good CAD model is desirable. Power-bus design issues can be investigated at a lower cost and early in the design cycle. Further, general design guidelines can be developed using this aid.

A Circuit Extraction approach based on a Mixed-Potential Integral Equation (CEMPIE) formulation has been developed [1], [2]. This approach can be used to model various power-bus structures that include arbitrary power plane metallization, as well as multiple layers. The circuit extraction approach is advantageous because of the availability of general purpose circuit solvers, as well as being compatible with device and transmission-line models for more detailed PCB level modeling. The modeling approach agrees well with measurements into the gigahertz range. However, vertical discontinuities, e.g., for decoupling capacitors are not included in the first principles formulation, and are incorporated as lumped circuit elements. However, doing this properly is essential for agreement with measurements. This paper presents a method to incorporate these discontinuities into the CEMPIE approach. A brief overview of the present CEMPIE tool is given. The procedures to incorporate the vertical discontinuities are discussed, and measured and modeled results are compared.

II. CEMPIE Modeling

The CEMPIE tool is formulated from first principles using a mixed-potential integral equation formulation. In responding to an incident electric field \vec{E}^{inc} , a surface current is induced on the metallization surface in the multi-layer PCB design of concern. Let \vec{J}_s and Φ represent the induced surface current density and the scalar potential, respectively. Then the scattered electric field is

$$\vec{E}^s = -j\omega\mu \int_S \vec{G}^A(\vec{r}, \vec{r}') \cdot \vec{J}_s ds' - \nabla\Phi, \quad (1)$$

where $\vec{G}^A(\vec{r}, \vec{r}')$ is the dyadic Green's function. Applying the boundary condition on this metallization surface, the electric field integral equation results

$$\hat{n} \times \vec{E}^{inc} = \hat{n} \times (j\omega\mu \int_S \vec{G}^A(\vec{r}, \vec{r}') \cdot \vec{J}_s ds' + \nabla\Phi + Z_s \vec{J}_s). \quad (2)$$

The integral equation is discretized using the method of moments (MOM) with a triangular mesh and vector basis functions [3]. Furthermore, assuming the scalar potential in each cell is constant, a MPIE results [4]. Finally, an admittance matrix is derived neglecting losses, and a circuit model extracted without solving the matrix equation [1].

For a specific power-bus structure, first, a triangular mesh is generated for the arbitrary metallization surface of concern. Then the Green's functions for arbitrary multi-layer media are calculated. The integral equation is discretized, and the matrix elements are then calculated. The matrix equation is not solved, rather, an equivalent circuit model is extracted using a static Green's function approximation. Specific locations for ports and attached elements can then be specified. The resulting circuit model is generated in a SPICE netlist format.

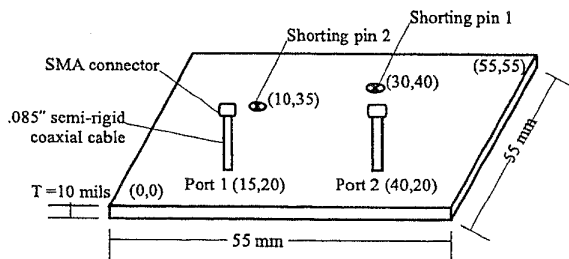


Figure 1: Power-bus geometry for comparison of modeling and measurements (coordinates in mm).

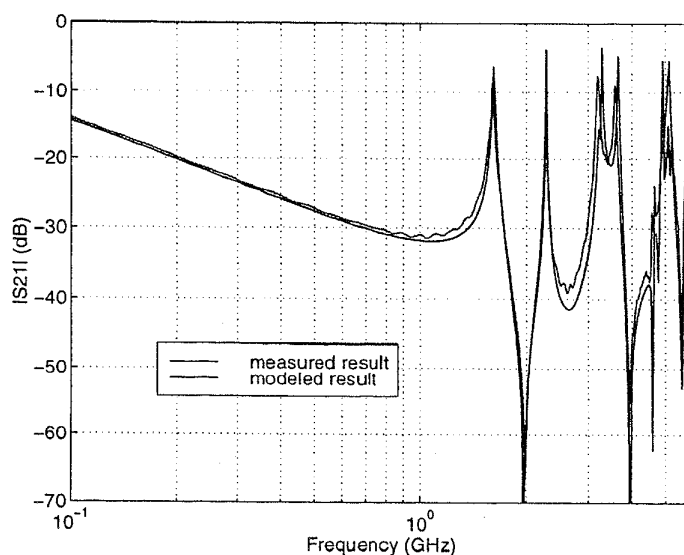


Figure 2: Comparison of measured and modeled $|S_{21}|$ results for the case when no shorting pins are present.

The CEMPIE tool has been used to investigate various power-bus and power-island structures without vertical discontinuities. The modeled and measured results agree very well up to 3GHz. A specific power-bus geometry is shown in Figure 1. The measured and modeled results for $|S_{21}|$ are compared in Figure 2 when the shorting posts are not present.

III. Incorporating Vertical Discontinuities

A simple power-bus structure with two solid metallization planes is studied, as shown in Figure 1. Two shorting pins are added to represent vertical discontinuities associated with vias and interconnects for SMT decoupling capacitors. The top layer is discretized into triangular cells. The CEMPIE tool is used to extract an equivalent circuit model for this specific power-bus geometry, and $|S_{21}|$ is calculated. The resulting extracted circuit model predicts the frequency response well for the case when no shorting pins are present, as shown in Figure 2. However, vertical discontinuities are not included in the first principles formulation. Though vertical discontinuities may be dealt with in the formulation, theoretically, by enforcing the boundary, for a practical PCB with many vias, it is impractical.

The inductance associated with each shorting pin is determined experimentally [5]. Then, the measured lumped inductance of each shorting pin is added to the resulting CEMPIE circuit model. Compared with the measured result, as shown in Figure 3, the modeled first resonant frequency is lower. This resonance is caused by the interplane capacitance of the power-bus structure in parallel with the inductance related to the shorting pins. The case with only one of the shorting pins present is similar, and any mutual inductance between the two shorting pins alone does not account for the discrepancy.

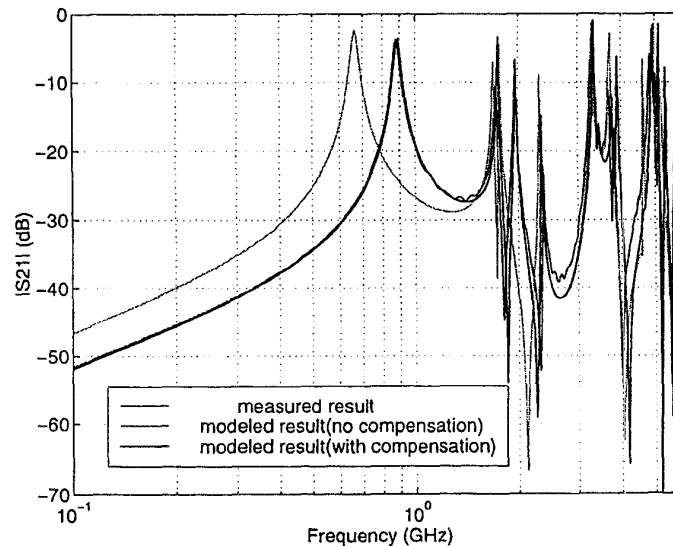


Figure 3: Comparison of measured and modeled $|S_{21}|$ with two shorting pins.

Compensation is introduced to each shorting pin individually to reconcile the modeled and measured results. When looking into the CEMPIE circuit model at the node where the shorting pin is located, before the inductances of the shorting pins are added, the input impedance exhibits a series resonance. Assuming that there is an inductance in series with the board interplane capacitance, the value of this equivalent inductance is determined from the resonant frequency and capacitance. Then, this value is subtracted from the measured inductance of the shorting pin and the resulting compensated value is used in the CEMPIE circuit model. After compensation, the modeled and the measured results agree.

IV. Conclusions

An approach for DC power bus modeling in multi-layer PCBs based on a mixed potential integral equation formulation with circuit extraction has been presented. For investigating power bus design approaches, vertical via discontinuities and interconnects for SMT decoupling capacitors must be included. Including a lumped element model using a measured inductance, however, results in a predicted resonance lower than the measured value. Compensating for the inductance included in the integral equation formulation of the planar structures results in good agreement between the measured and modeled results. While the compensation procedure works, the relevant physics of associating "partial inductances" with the planes, via, and feed, are not completely understood. Further, in the present case, the feed probes, and shorting pins were spaced sufficiently for the mutual inductance to be negligible for the 10 mil. substrate. Presently, models that include the mutual inductance are being worked out. The effect of the mutual inductance depends on the ratio of the via spacing to board thickness. The mutual inductance effect has considerable implications for power bus design, and SMT decoupling.

V. References

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