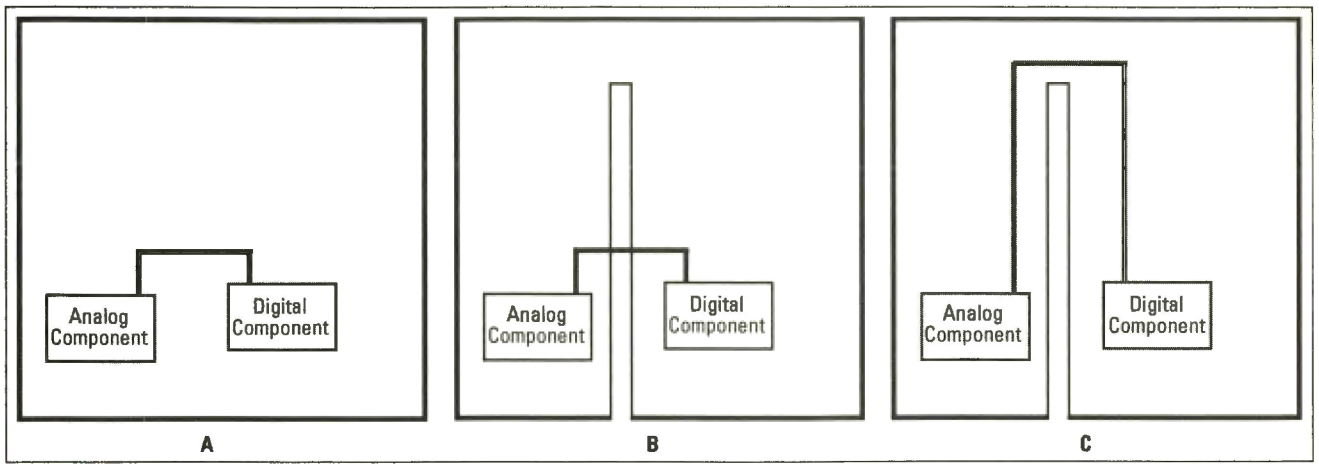

FIGURE 1. Of these routing options, (a) is the only choice that is consistent with our guidelines for minimizing EMC problems. However, if the gap in the ground plane was required, then (c) is the best remaining option.

Designing for EMC: The TOP 4 GUIDELINES

The problem with design guidelines is the more you have, the harder it is to comply with all of them. Knowing how to prioritize makes the difference. **by DR. TODD HUBING and DR. TOM VAN DOREN**

Suppose you're laying out a high-speed multilayer PCB. You need to route a trace carrying a high-frequency analog signal from a transistor in an analog circuit to the input pin of a digital component. You want to minimize the chance of having an electromagnetic compatibility (EMC) problem, so you search the Web and find three guidelines that seem to pertain to your situation:

1. Minimize the length of high-speed traces;
2. Always gap the power and ground planes between analog and digital circuits; and
3. Never let a high-speed trace cross over a gap in the ground plane.

You envision the three possible routing strategies shown in **FIGURE 1.** The first routes the trace directly between the two components, but leaves the plane between them solid. The second gaps the plane, but routes the trace over the gap. The third routing strategy routes the trace around the gap. Each of these alternatives violates one of the guidelines. Is each alternative equally good because it satisfies two of the three guidelines? Are they all bad because they all violate at least one guideline?

These are questions designers face everyday. Making the right choice can be the difference between a board that meets all requirements and a board that has severe radiated emissions or susceptibility problems. In this case our choice should be clear, but we'll address that later.

The problem with design guidelines is that the more you have, the less likely you will be able to comply with all of them. For this reason it is important to be able to prioritize your guidelines. At the University of Missouri-Rolla, we teach an electromagnetic compatibility course for seniors and graduate students. Each year, students are given various design problems in which they are required to place components and manually layout simple circuit boards. These students are familiar with the concepts of parasitic inductance, capacitance and antenna theory. They are provided with a list of 40 EMC design guidelines and each of these guidelines is discussed at length in class. Nevertheless, invariably the first-pass designs range from "not good" to "terrible." In many cases, these first-pass designs are worse than they would have been had they not followed any of the guidelines.

The problem comes down to prioritizing. Design guidelines can be helpful if they are well understood and if they are part of an overall design strategy. Once designers learn to prioritize them and understand how each guideline is used to accomplish certain objectives, they are able to consistently design good boards.

These top four EMC guidelines are based on common design features that have led to EMC problems in electronics products we have evaluated. In many cases, board designers have intentionally violated one of these guidelines in an attempt to comply with much less important guidelines.

Rule 1. Minimize Signal Current Path Loop Areas. This simple rule is on nearly every list of EMC guidelines, but it often gets ignored or compromised in favor of other guidelines. Often the board designer doesn't even know

where the signal currents flow. Digital circuit designers like to think of signals in terms of their voltage. Signal integrity and EMC engineers must think of signals in terms of their current.

There are two things that every circuit designer should know about signal currents:

- Signal currents always return to their source; i.e., current paths are always loops.
- Signal currents take the path(s) of least impedance.

At megahertz frequencies and higher, signal current paths are relatively easy to identify. This is because the path of least impedance at high frequencies is generally the path of least inductance, which is generally the path that minimizes the loop area. **FIGURE 2** shows two components on a PCB. A 50 MHz signal propagates on a trace above a plane from Component A to Component B. We know that an equal amount of current must therefore flow from Component B to Component A. In this case we'll assume that this current exits the pin of Component B labeled GND and makes its way back to the pin of Component A labeled GND.

Since a solid plane is provided and the ground pins of both components are close, it is tempting to conclude that the current takes the shortest path between them. However, this is not correct. High-frequency currents take the path of least inductance or the path of least loop area. The majority of the signal current returning on the plane flows in a narrow path (Path 2) directly underneath the signal trace.

If the plane were to be gapped for any reason, as shown in **FIGURE 3**, a gap in position 1 would have little effect on the signal integrity or on radiated emissions. A gap in position 2, however, could result in significant problems. The gap in position 2 violates Rule 1. The signal loop area increases dramatically when return currents are forced to flow around the gap.

At low frequencies (generally kHz frequencies and below), the path of least impedance tends to be the path of least resistance. On a PCB with solid return planes, the resistance of the planes tends to spread the current so

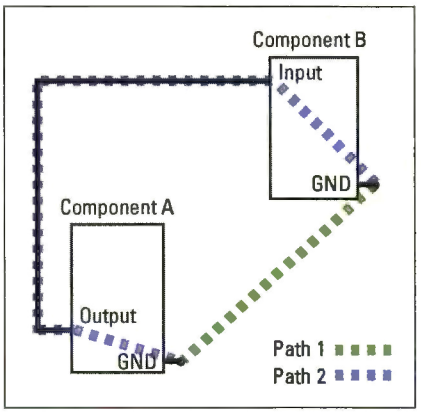

FIGURE 2. High-frequency currents take the path of least inductance or the path of least loop area. Thus, in this example the majority of the return signal current flows on Path 2 directly underneath the signal trace.

that current flowing between two distant points can cover most of the board as shown in **FIGURE 4**. On mixed-signal boards, with low-frequency analog and digital components, this can create problems. **FIGURE 5** illustrates how a well-placed gap in the ground plane can protect circuits located in a particular region from low-frequency return

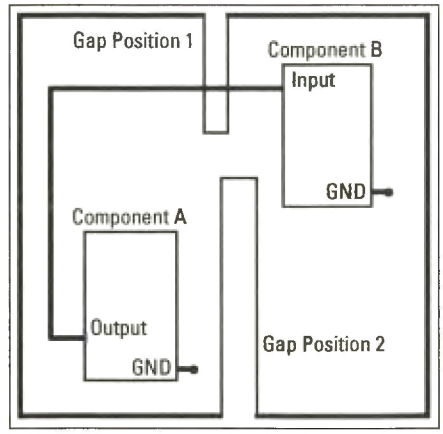

FIGURE 3. Signal loop area increases dramatically when return currents are forced to flow around the gap, as in position 2.

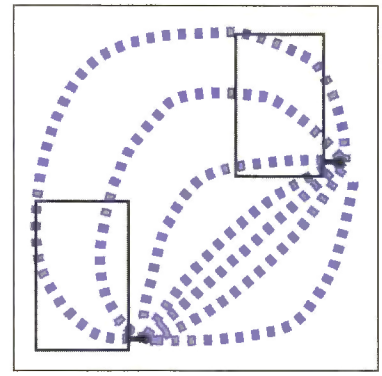

FIGURE 4. The return current path of a low frequency (kHz or less) design. Here, the resistance of the planes tends to spread the current.

currents flowing in the plane.

Rule 2. Don't Split the Signal Return Plane. That's right. We just provided an excellent example of a situation where gapping a signal return plane was the correct choice. Then, like typical EMC engineers, we advise you never to do this. Why? Because so many problem designs we've encountered were the result of well-meaning people inadvertently violating Rule 1 by gapping their return plane. More often than not, the gap was ineffective and unnecessary.

There is one school of thinking that says analog returns must always be isolated from digital returns. This idea became popular when analog and digital circuits tended to work at kHz frequencies. For example, boards that contained digital audio and analog audio circuits often exhibited noise problems due to interference arising when the low-frequency digital signal currents spread under the region of the board where sensitive analog amplifiers were located. Years ago, audio circuit board designers learned to avoid this problem by gapping the return plane in order to control the low-frequency current return paths and keep the analog currents away from the digital currents.

Our students are given a design problem requiring them to protect sensitive analog components (usually audio amplifiers or phase-locked loop oscillators) from digital circuitry by gapping the return plane in such a way that the low-frequency currents are isolated and the high-frequency currents are not impeded. It is usually not obvious how this can be accomplished and quite often well-intended gaps in the plane create more problems than they solve.

A similar situation arises when laying out automotive or avionics boards. These boards often isolate their digital circuit returns from their frame (or chassis) grounds in order to protect the digital circuits from damage due to large low-frequency currents that may flow on the vehicle's metallic structure. EMI filtering and transient protection normally require connections to frame ground, while signal carrying circuits must be connected to the digital return plane.

When the frame ground and digital current return planes share the same layer, they appear to be one plane with a gap. This sometimes creates confusion regarding which "ground" a particular component should be connected to. In this situation, it is usually a good idea to route frame ground and digital current return on separate layers. The digital return plane should be solid and fill the area beneath all digital components, traces and connectors. The frame ground should be confined to the region of the board near the connectors.

Sure, there are some situations where a well-placed gap in the return plane is called for. However, the safest rule-of-thumb is to provide one solid plane for returning all signal currents. In situations where a particular low-frequency signal is susceptible or is capable of interfering with the circuitry on the board, use a trace on a separate layer to return that current to its source. In general, never split, gap or cut the board's signal return plane. If you are convinced that a gap is necessary to prevent a low-frequency cou-

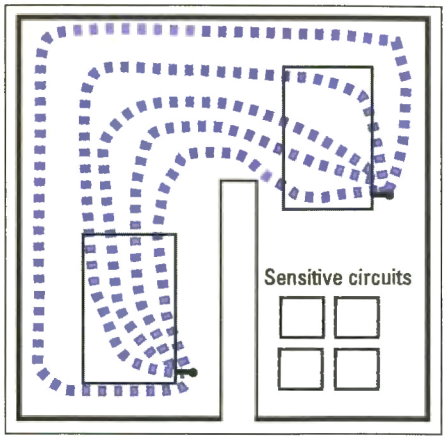

FIGURE 5. Low-frequency return current path with a gapped plane. A well-placed gap protects circuits from low-frequency return currents.

pling problem, seek advice from an expert. Don't rely on design guidelines or application notes, and don't try to implement a scheme that worked in someone else's "similar" design.

Now that we are familiar with the top two EMC design guidelines, we are ready to revisit the problem in Figure 1. Which trace routing alternative is best? The first option is the only routing choice that is consistent with the guidelines. If by some chance, the gap in the ground plane was required (for reasons beyond the designer's control), then the third routing strategy is the best remaining option. Routing the trace around the gap minimizes the signal current loop area.

Rule 3. Don't Locate High-Speed Circuitry Between Connectors. This is one of the most common problems among board designs that we have reviewed or evaluated in our lab. Simple board designs that should have had no trouble at all meeting EMC requirements at no additional cost or effort wind up being heavily shielded and filtered because they violated this simple rule.

Why is the location of connectors so important? At frequencies below a few hundred megahertz, wavelengths are on the order of a meter or longer. Any possible antennae on the PCB itself tend to be electrically small and therefore inefficient. However, cables or other devices connected to a board can serve as relatively efficient antennas.

Signal currents flowing on traces and returning through solid planes result in small voltage differences between any two points on the plane. These voltage differences are generally proportional to the current flowing in the plane. When all connectors are placed along one edge of a board, the voltage between them tends to be negligible. However, high-speed circuitry located between connectors can easily develop potential differences of a few millivolts or greater between the connectors. These voltages can drive currents onto attached cables, causing a product to exceed radiated emissions requirements.

A board that easily meets all the specifications when the connectors are located on one edge can become an EMC engineer's worst nightmare if even one connector with a cable attached is located on the opposite edge of the board. Products that exhibit this type of problem (cables driven by voltages induced across a solid plane) are particularly difficult to bring into compliance. Often rather extensive shielding is required. In many cases, this shielding would have been completely unnecessary if the connectors had just been located on one edge or one corner of the board.

Rule 4. Control Signal Transition Times. A board operating with a clock speed of 100 MHz should never fail to meet a radiated emissions requirement at 2 GHz. A well-formed digital signal will have a significant amount of power in the lower harmonic frequencies, but not so much power in the upper harmonics. Power in the upper harmonic frequencies is best controlled by controlling the transition times in digital signals. Longer transition times are preferred for EMC. Excessively long transition times can cause signal integrity and thermal problems. An engineering compromise must be reached between these competing requirements. A transition time that is approximately 20% of a bit period results in a reasonably good-looking waveform, while minimizing problems due to crosstalk and radiated emissions. Depending on the application, transitions times may need to be more or less than 20% of the bit period; however, transition times should not be left to chance.

There are three common methods for controlling rise and fall times in digital logic:

- Use a logic family that is only as fast

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as the application requires.

- Put a resistor or a ferrite in series with a device's output.
- Put a capacitor in parallel with a device's output.

The first choice is often the easiest and most effective option. However, the use of a resistor or ferrite gives the designer more control and is less affected by changes that occur in logic families over time. The advantage of using a capacitor to control transition times is that capacitors can be removed from the board if they are not needed. However, capacitors can actually increase the amount of high-frequency current drawn by the source device.

Note that it is never a good idea to try to slow or filter a single-ended signal by impeding the flow of current in the return path. For example, never intentionally route a low-speed trace over a gap in a return plane in an attempt to filter out the high-frequency noise. After reviewing the first two design guidelines, this should be obvious. Nevertheless, boards employing this flawed design strategy occasionally show up in our lab.

Generally speaking, give these four EMC guidelines top priority during the design and layout of a PCB. These guidelines shouldn't be compromised in any attempt to comply with other EMC guidelines. Nevertheless, there are a few additional guidelines worth mentioning. For example, it's important to provide adequate power bus decoupling, to keep input/output traces short and to provide for filtering of traces carrying signals that leave the board.

It's also a good idea to choose your active devices carefully. Not all pin-compatible semiconductors are equal when it comes to noise. Two devices with the same specifications made by different manufacturers can vary greatly when it comes to the amount of noise that they put out on their power, output and input pins. This is especially true for more complex devices like microprocessors and large ASICs. It's a good idea to evaluate components from different vendors whenever possible.

And finally, have your design reviewed. Even if you're an experienced PCB designer and an expert in EMC, it's a good idea to have someone who is knowledgeable about EMC design review your layout and offer suggestions. A person who is intimately familiar with a board's design may be less likely to notice problems that someone less attached to the design might spot fairly quickly.

But whose advice can you trust? Trust anyone whose recommendations clearly helped you to meet the top four design guidelines. A little bit of extra attention during the design and layout can save a lot of time, money and effort that would otherwise be wasted trying to fix a non-compliant product. PCD&M

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