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Final Report – NCMS Embedded Capacitance Project

Electrical Model and Test Results for Embedded Capacitance Boards

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Executive Summary

This report describes the electrical models developed and the electrical validation tests performed at the University of Missouri-Rolla for the NCMS Embedded Capacitance Project. The purpose of this work was to evaluate the performance of embedded capacitance relative to traditional printed circuit board decoupling techniques in various applications. A primary goal of this project was to develop models and guidelines to help designers decide when and how to use embedded capacitance in their printed circuit board designs.

Electrical models available at the beginning of the project suggested that embedded capacitance materials would be capable of reducing power bus noise at frequencies well above the useful range of surface mounted capacitors. However, there were concerns that high-dielectric-constant materials might be ineffective at high frequencies or introduce new problems due to power bus resonances.

The results of the tests performed during the course of this project were very encouraging. All of the embedded capacitance materials did a good job of reducing power bus noise over the entire frequency range evaluated (up to 5 GHz). The materials with the thinnest dielectric layers were the most effective. For a given thickness, the materials with the highest dielectric constant worked best. One surprising observation was that all of the embedded capacitance materials tested dampened the resonances in the power bus significantly. The two thinnest materials effectively eliminated all power bus resonances.

New power bus models for embedded capacitance boards have been developed at the University of Missouri-Rolla that can be used to predict how well a given embedded capacitance material will perform and what characteristics an embedded capacitance layer must have in order to optimize its effectiveness. Although work on these models is continuing, enough information has been obtained to develop design guidelines that can help printed circuit board designers decide whether embedded capacitance will benefit their design and choose an embedded capacitance material that will meet their needs.

1. Introduction

This work was performed for the National Center for Manufacturing Sciences (NCMS) Embedded Capacitance project. The purpose of this project was to investigate the viability of different forms of embedded capacitance for improving the performance and/or reducing the cost of printed circuit boards. The role of the University of Missouri-Rolla in this project was to help design and evaluate the electrical performance of test boards that implemented embedded capacitance layers provided by various materials suppliers and assembled by different board manufacturers.

Four embedded capacitance materials were evaluated. Two of these, BC2000 and EMCAP, were commercially available prior to the start of this project. BC2000 is a 2-mil layer of FR-4 sandwiched between copper power and ground planes. EMCAP is a 4-mil layer of high-dielectric-constant material between power and ground planes. Two new materials were also evaluated. Dupont Hi-K is a 1.2-mil layer[1] of high-dielectric-constant material between planes and 3M C-Ply is a very thin (~5 micron) layer of dielectric between planes.

2. Decoupling Overview and Models

A sudden change in the amount of current drawn by a component on a printed circuit board can cause a momentary drop (or surge) in the voltage on the power distribution bus. This voltage transient can be sufficiently large to interfere with the normal operation of other components on the board. Ground bounce or delta-I noise, as this phenomenon is called, is a common problem in high-speed printed circuit board (PCB) and multi-chip module (MCM) designs. Decoupling capacitors connected to power and ground are typically added to mitigate this problem. Decoupling capacitors help to stabilize the power distribution bus by supplying current that opposes any change in the power bus voltage. However, decoupling capacitors take up space and add cost to printed circuit board designs.

2.1 Basic decoupling models

Consider the simple model of an electronic system illustrated in Figure 2.1. This model can be applied at frequencies where the impedance of the printed circuit board traces is low enough to

[1] All of the Dupont Hi-K results in this report are for 1.2-mil material. However, Dupont is currently marketing thinner versions of this material.

ensure that the voltage difference between any two points on the power distribution traces or planes is negligible. If the current demands of each component on the printed circuit board are constant, the voltage at each component is equal to the power supply voltage. However, a change in the current drawn by the components on the board results in a voltage drop across the inductance of the power distribution wires. The voltage at the input of the printed circuit board is reduced by the amount of this voltage drop,

$$V_{board}(t) = V_{supply} - (L_P + L_G)\frac{di(t)}{dt}. \quad (1)$$

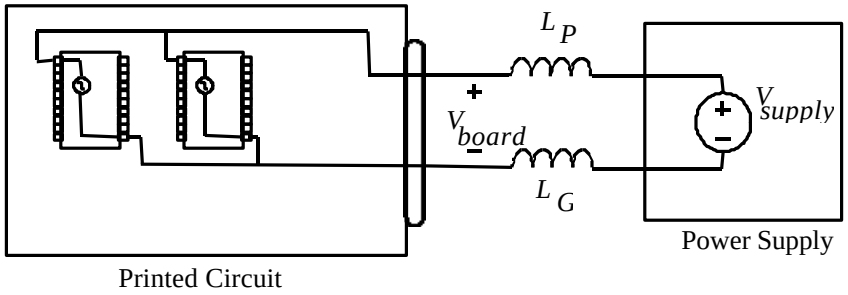

Figure 2.1 Simple Power Distribution Model

For example, a printed circuit board drawing 200 mA in 1 μsec through a 10-μH inductance will experience a 2-volt drop in the supply voltage. This could be sufficient to cause components on the board to malfunction.

A bulk decoupling capacitor on the board near the power input can help to alleviate this problem. In the time domain, the capacitor can be viewed as a local source of charge. As the voltage of the board begins to drop, the current supplied by the bulk decoupling capacitor is,

$$i = C_B\frac{dV}{dt}. \quad (2)$$

This current helps to meet the needs of the components on the board and reduces the delta-I voltage drop across the power line inductance. After the momentary need for current has been met, the capacitor is recharged by the power supply.

In the frequency domain, the bulk decoupling capacitor can be viewed as a low-impedance power source. In the absence of the bulk decoupling capacitor, the impedance of the power supply as viewed from the board is,

$$Z_{supply} = jw(L_P + L_G). \quad (3)$$

The voltage at the power input of the printed circuit board is,

$$V_{board}(t) = V_{supply} - I(w)Z_{supply}(w). \quad (4)$$

For a given amount of current drawn by the board, a larger Z_{supply} results in a greater deviation from V_{supply}. A bulk decoupling capacitor at the power input reduces the power supply impedance as viewed from the board to,

$$Z_{supply} = \frac{jw(L_P + L_G)}{1 - w^2(L_P + L_G)C_B}. \quad (5)$$

Figure 2.2 illustrates a power distribution model that is valid at higher frequencies where the inductance of the power distribution traces on the board is no longer negligible. The inductance of these traces is typically on the order of 100 nH or greater on a board without internal power and ground planes. A device drawing as little as 30 mA in 1 nsec through 100 nH can produce a 3-volt transient at its own power pins and at the pins of every component connected to the power traces beyond the switching device.

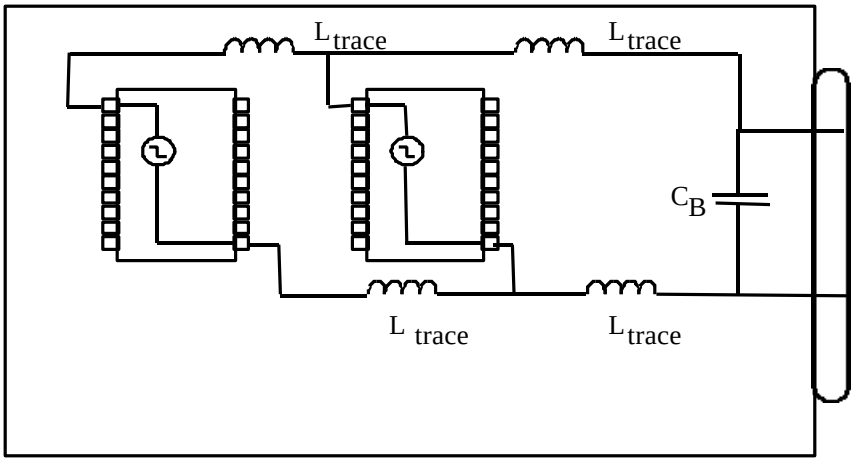

Figure 2.2 Simple Power Bus Model Accounting for Power and Ground Trace Inductance

A decoupling capacitor located near the active device helps to mitigate this problem. In the time domain, this capacitor is a local source of current that is specified to meet the needs of a single component. In the frequency domain, the decoupling capacitor lowers the impedance of the power bus as viewed from the active device.

At higher frequencies, the inductance associated with the current path formed by the traces connecting the decoupling capacitor to the component being decoupled can no longer be neglected. The circuit model of the power distribution traces on the board must be modified to include these inductances as shown in Figure 2.3. In the time domain, this inductance can be viewed as limiting the maximum rate of change of current supplied by the decoupling capacitor. In the frequency domain, this inductance prevents the impedance provided by the decoupling capacitor from decreasing with frequency indefinitely.

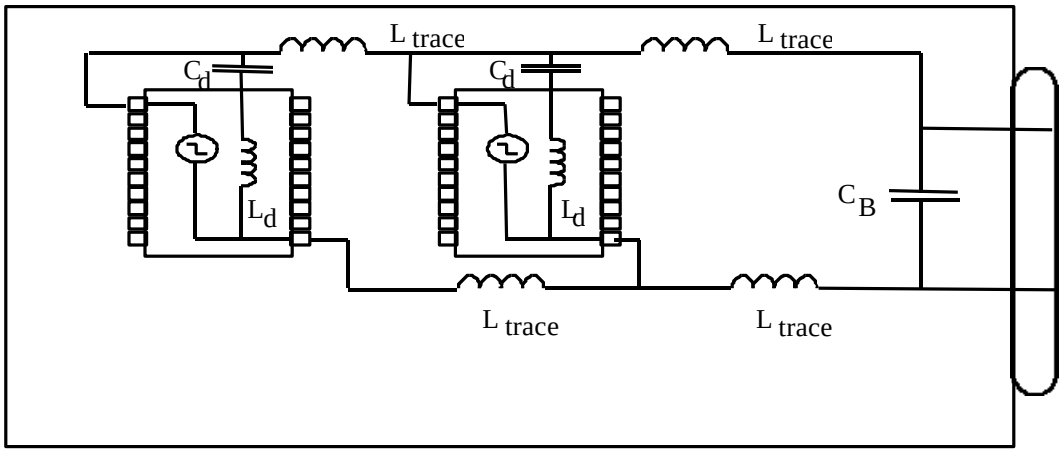

Figure 2.3 Power Bus Model Accounting for Capacitor Lead Inductance

2.2 Lumped element models for boards with closely spaced power and ground planes

Figure 2.4 shows a lumped-element model for the power distribution impedance on a board with closely spaced[2] power and ground planes. At high frequencies, the inter-plane capacitance plays an important role in reducing the impedance of the planes. At frequencies where the maximum dimensions of the board are much less than a wavelength, the plane inductance is negligible and the plane can be modeled with a single capacitor. The effectiveness of capacitors mounted on the surface of a printed circuit board is limited by their interconnect inductance. The model in Figure 2.4 can be used to calculate the power bus impedance at frequencies well below the first board resonance. This model is fully explained and validated in [3].

At low frequencies, the impedance of the power bus is approximately equal to,

[2] "closely spaced" is a relative term that depends on how the decoupling capacitors are connected. For typical board designs, this model is valid for a power-ground spacing of 10 mils or less. Models for boards with wider plane spacing must account for the mutual inductance between vias [1] [2].

$$Z_{powerbus} = 1/jw(C_B + C_1 + C_2 + \cdots + C_n) \tag{6}$$

and all of the capacitors on the board help to decouple the power bus, although the larger-valued capacitors are most effective. At higher frequencies, some of the decoupling capacitors begin to look like inductors. The inductance of these capacitors forms a resonant circuit with the inter-plane capacitance and the capacitors that do not yet look like inductors. At resonant frequencies, the impedance of the power bus can be very high and the board will tend to ring at these frequencies if there is not sufficient loss in the board or the capacitors to dampen these resonances. A procedure for selecting decoupling capacitors in order to reduce the power bus impedance over a wide band of frequencies is described in [4].

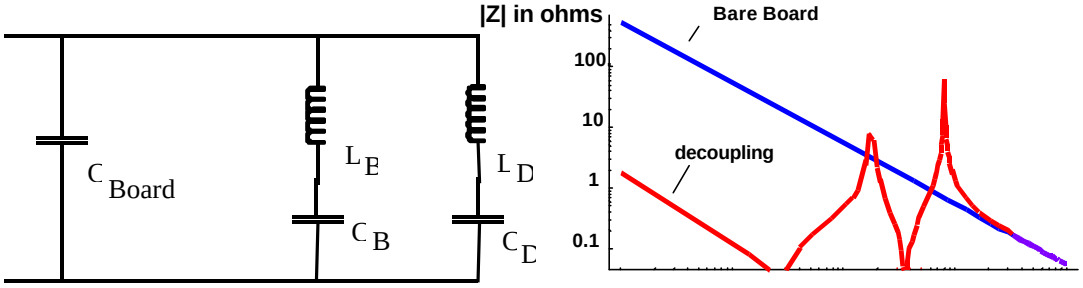

Figure 2.4 Lumped-Element Model for Power Distribution on a Board with Closely Spaced Power and Ground Planes

2.2 Distributed models for boards with closely spaced power and ground planes

The lumped element model described in the previous section works very well for estimating the power bus impedance at frequencies below the first board resonance. However, at frequencies where the dimensions of the board are not electrically small, it is necessary to employ more complex distributed models. Rubin and Becker [5] and others have modeled electrically large printed circuit boards using a grid of lumped resistors, capacitors and inductors. Novak [6] uses a grid of transmission lines to model power bus structures. Shi [7] developed a 2D integral equation code for analyzing power buses. Each of these techniques can be used in conjunction with SPICE models of active devices to model the behavior of power-ground plane pairs. However, these models are relatively complex; they require a significant amount of time and expertise to implement properly; and they are only able to model relatively simple printed circuit board configurations.

2.3 The cavity model

Although the cavity model described in this section is not particularly simple, it is reasonably intuitive. In this report, the cavity model will provide the theoretical foundation for simple closed-form expressions that designers can use to predict the performance of boards with embedded capacitance.

Since most boards are electrically thin, they can be modeled as TM_z cavities with two perfect electric conductor (PEC) walls representing the power and the ground planes. The sides of rectangular boards can be modeled with four perfect magnetic conductor (PMC) sidewalls. For the lossless case, the input impedance of this geometry is given by [8,9,10]:

$$Z_{in} = jwmh \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} \frac{c_{mn}^2 \cos^2(k_{yn} y_i)\cos^2(k_{xm} x_i)}{ab\left(k_{xm}^2 + k_{yn}^2 - k^2\right)} sinc^2\left(\frac{k_{yn} dy_i}{2}\right) sinc^2\left(\frac{k_{xm} dx_i}{2}\right) \qquad (7)$$

where: $k_{xm} = \frac{mp}{a}$, $k_{yn} = \frac{np}{b}$, $k = w\sqrt{em}$.

$c_{mn}^2 = 1$ for m=n=0; $c_{mn}^2 = 2$ for m=0 or n=0; $c_{mn}^2 = 4$ for m≠0, n≠0.

(x_i, y_i) is the center location of the feeding port.

(dx_i, dy_i) is the dimension of the feeding port

An equivalent circuit based on a modal expansion for the power-ground plane structure is shown in Figure 2.5.

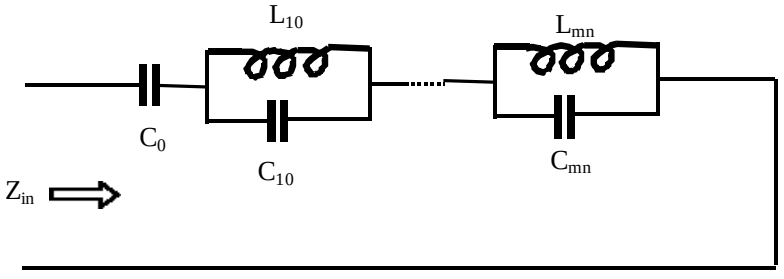

Figure 2.5 Circuit model for a Lossless Power-Ground Plane Structure

In this model, the impedance contributed by the TM_{mn} mode is given by:

$$Z_{mn} = \frac{1}{jwC_{mn} - j/(wL_{mn})} \tag{8}$$

where

$$C_{mn} = \frac{abe}{hc_{mn}^2}\frac{1}{A^2B^2} \qquad L_{mn} = mh\frac{c_{mn}^2}{ab}\frac{A^2B^2}{k_{xm}^2 + k_{yn}^2}$$

$$A = sinc(\frac{k_{yn}dy_i}{2})sinc(\frac{k_{xm}dx_i}{2})$$

$$B = cos(k_{yn}y_i)cos(k_{xm}x_i).$$

The impedance contributed by a particular TM_{mn} mode can be modeled by an LC parallel branch with a resonance frequency ω_{pmn} equal to the cutoff frequency ω_{cmn} of this mode. According to this model, the TM_{mn} mode has an inductive contribution to the input impedance below its cutoff frequency and a capacitive contribution above its cutoff frequency [8]. Therefore, below the cutoff frequency of the TM_{10} mode, the contribution from every mode is inductive. Hence, the power-ground plane structure can be simply modeled as an L_eC series branch below the TM_{10} cutoff frequency. The series resonance of this branch creates a null on the input impedance curve. This null occurs just before the first resonant peak at a frequency $f_{null} = 1/2p\sqrt{L_eC}$. Here C is the inter-plane capacitance and the effective inductance L_e is given by:

$$L_e = \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} L_{emn} \tag{9}$$

where: $$L_{emn} = \frac{L_{mn}}{1-\left(\frac{w}{w_{cmn}}\right)^2}.$$

In general, L_e is a function of frequency. However, at frequencies just below the TM_{10} cutoff frequency, L_e is relatively constant.

According to Equation (8), beyond the first series resonance frequency, the input impedance of the power-ground structure is inductive except at cavity resonance frequencies given by,

$$f_{mn} = \frac{1}{2p\sqrt{me}}\sqrt{\left(\frac{mp}{a}\right)^2 + \left(\frac{np}{b}\right)^2} \quad . \tag{10}$$

When the plane spacing is not very thin at the highest frequency of interest, the effect of fringing fields must be taken into consideration by adjusting the dimensions of the structure to an effective length and width. Several formulas have been proposed to calculate the resonance frequencies in the presence of a fringing field [11]. Most of the test boards built for this project employed very thin dielectric substrates, so the fringing effect could be neglected.

The input impedance of a 15.2-cm by 10.2-cm FR-4 board was calculated using Equation (7). A comparison between the calculated and measured input impedance from 0-2 GHz is shown in Figure 2.6. In general, the calculation agrees fairly well with the measurement. The slight frequency shift between the calculated and measured resonance frequencies is mainly due to the fringing effect for this 40-mil thick board. The most significant difference between the two curves in Figure 2.6 is the magnitude of the input impedance at resonance frequencies. The measured result has finite impedance values at resonance due to copper, dielectric and radiation losses. The cavity model, Equation (7), predicts an infinite $|Z_{in}|$ at resonance frequencies, since it does not account for loss.

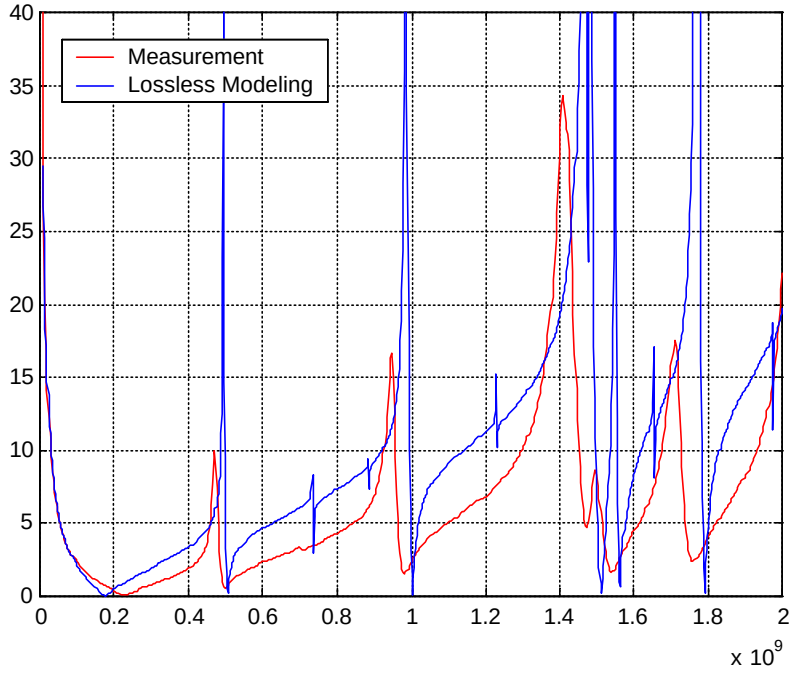

Figure 2.6 Input Impedance of a 15.2-cm by 10.2-cm FR-4 Board

2.4 The quality factor for power-ground plane structures

At cavity resonance frequencies, the magnitudes of the input impedance are related to the quality factor (or Q factor) of the resonance. Real power-ground plane structures exhibit loss due to the finite resistance of the copper walls, conduction loss in the dielectric, radiation loss, and losses due to surface waves induced on the outer surface of the copper. Surface wave losses are usually small compared to the other losses in normal power-bus geometries. Therefore, they can safely be neglected.

Formulas for conductive loss and dielectric loss are well documented [12,13]. For very thin dielectric layers between power and ground planes, an approximate formula for the quality factor due to conductive losses in the top and bottom planes is given by,

$$Q_c \approx h\sqrt{pfms} \ . \tag{11}$$

The quality factor due to dielectric losses is given by,

$$Q_d = 1/tand \ . \tag{12}$$

In general, the quality factor due to the radiation loss has to be numerically evaluated for a specific mode. However, an approximate closed form expression is provided in [11] for the

quality factor due to radiation loss at the dominant TM_{10} mode of structures with thin dielectric layers. The radiation quality factor is given by,

$$Q_{rad} = \frac{3}{16}\frac{e_r L_e l_0}{p c_1 w_e h} \tag{13}$$

where:

$$p = 1 + \frac{a_2}{10}(k_0 w_e)^2 + \left(a_2^2 + 2a_4\left(\frac{3}{560}\right)(k_0 w_e)^4 + c_2\left(\frac{1}{5}\right)(k_0 L_e)^2\right.$$
$$+ a_2 c_2\left(\frac{1}{70}\right)(k_0 w_e)^2 (k_0 L_e)^2$$
$$a_2 = -0.16605 \qquad a_4 = 0.00761 \qquad c_2 = -0.0914153$$
$$c_1 = \frac{1}{n_1^2} + \frac{2/5}{n_1^4} \qquad n_1 = \sqrt{e_r m_r}\ .$$

W_e and L_e are the effective dimensions of the structure after accounting for the fringing effect.

The overall quality factor can be approximated by,

$$\frac{1}{Q} = \frac{1}{Q_c} + \frac{1}{Q_d} + \frac{1}{Q_{rad}}. \tag{14}$$

In general, Q is related to a specific cavity mode, and is a function of frequency. With the loss taken into consideration, the narrow band model of the power-ground plane structure around the resonant frequency of a specific TM_{mn} mode can be represented as shown in Figure 2.7.

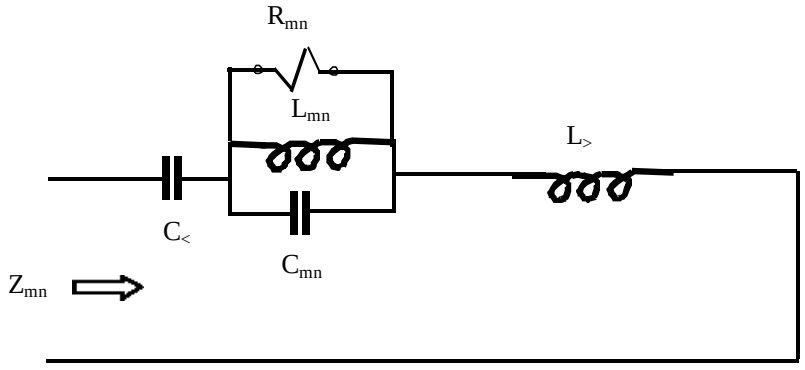

Figure 2.7 Narrow Band Equivalent Circuit for Lossy Power-Ground Plane

Here $C_<$ is the total contribution to the impedance from those modes whose cutoff frequency is lower than the cutoff frequency of the TM_{mn} mode, w_{mn}. And $L_>$ is the inductive contribution of all modes whose cutoff frequency is higher than $w_{mn.}$. The loss resistance for the TM_{mn} mode can be calculated using the expression,

$$R_{mn} = \frac{Q_{mn}}{w_{mn} C_{mn}}. \tag{15}$$

Then the input impedance at a frequency w_0 that is slightly higher than w_{mn} can be approximately calculated as,

$$Z(w_0) = j(w_0 L_> - \frac{1}{w_0 C_<}) + \frac{R_{mn}}{1 + 2jQ_{mn}\frac{(w_0 - w_{mn})}{w_{mn}}}. \tag{16}$$

Substituting Equation (16) into Equation (17) yields,

$$Z(w_0) = j(w_0 L_> - \frac{1}{w_0 C_<}) + \frac{1}{\frac{w_{mn} C_{mn}}{Q_{mn}} + 2j(w_0 - w_{mn})C_{mn}}. \tag{17}$$

According to these expressions, the magnitude of $Z(w_0)$ is related to the quality factor. Higher losses result in lower quality factors, which in turn lead to lower power bus impedances at resonance frequencies.

The input impedance around resonance frequencies is related to the quality factor of the structure. Formulas to calculate the quality factor associated with the conductive loss, the dielectric loss, and the radiation loss can be applied to estimate the overall quality factor at each resonant frequency. The input impedance around the resonance frequency can then be calculated from the narrow band equivalent circuit of the cavity model. Plugging typical values of dielectric loss, copper conductivity and circuit board dimensions into Equations (11-13), suggests that copper losses will be the dominant loss mechanism in most embedded capacitance boards. This will be confirmed by the measurement results presented in Section 4. Note that a Q-factor of 1 implies that a resonance has been completely damped and the impedance will not peak at that frequency. Therefore, resonances can be eliminated by choosing the materials and dimensions such that the Q-factor in Equation (11) is less than or equal to 1.

2.5 Estimating power bus noise based on device currents and board impedance

Well-designed power distribution buses have a very low impedance (usually much less than 1 ohm) at all frequencies of interest. The impedance associated with active devices mounted on a board's surface tend to be much higher than the power bus impedance; therefore most active devices can be modeled as ideal current sources.

For a given set of active devices on a board, the power bus noise voltage can be calculated using the equation,

$$V_{noise} = I_{devices} \times Z_{powerbus} \tag{18}$$

Several texts and papers (e.g. [4], [14]) propose methods of estimating the total transient current drawn by active devices. These estimations usually involve calculating the current as the sum of the load capacitances times the change in signal voltage over the transition time. Van Doren [15] outlines a procedure for estimating the shoot-through current in CMOS devices using the value of the power dissipation capacitance provided in most CMOS data sheets. Regardless of the technique used to determine the current drawn by the devices, the key to reducing the noise voltage on the power bus is minimizing the power bus impedance at all frequencies of interest.

3. Description of the TV1 Test Vehicle

The TV1 test vehicle is a set of printed circuit boards designed to evaluate the effectiveness of different embedded capacitance materials in various configurations. TV1 test boards were built by five manufacturers – 3M, HADCO, Litton, Merix, and Raytheon. These test boards employed four different embedded capacitance materials (Hadco BC2000, 3M C-Ply, Polycad EMCAP, Dupont Hi-K) and FR-4. Moreover, there were three different layer stack-ups used in these test boards. There were also three different layouts corresponding to three different board sizes.

In general, a test board was labeled as **TV1-X-Y**. Here **X** indicates the layer stack-up and can have a value of *1, 2,* or *3*. **Y** indicates the board size and layout and can have a value of 1, 4, or 12. The three stack-ups and the three board layouts are described in the following sections.

3.1 Stack-up of the TV1 test boards

Figures 3.1, 3.2 and 3.3 illustrate the three layer stack-ups used in the TV1 test boards. The power and ground planes are represented by the thick solid lines in these figures.

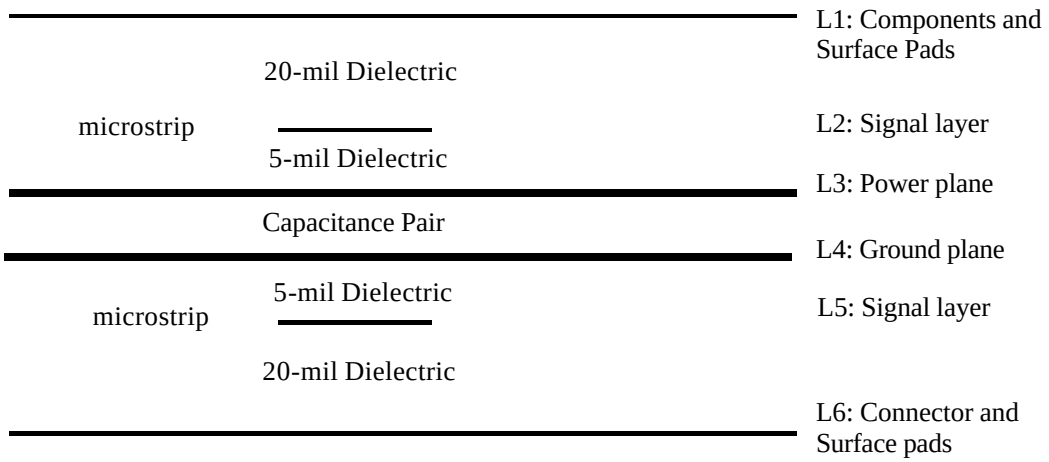

Figure 3.1 TV1-1-Y Stack-Up

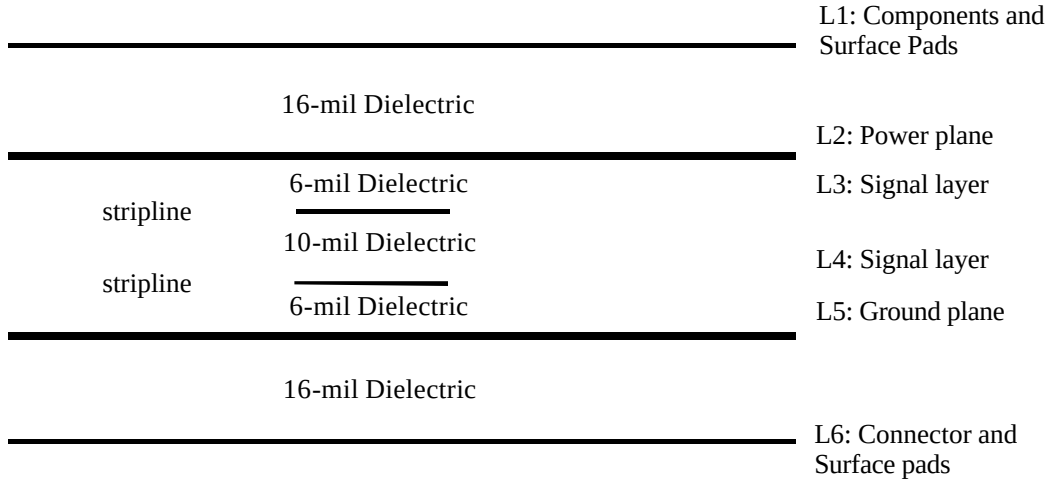

Figure 3.2 TV1-2-Y Stack-Up

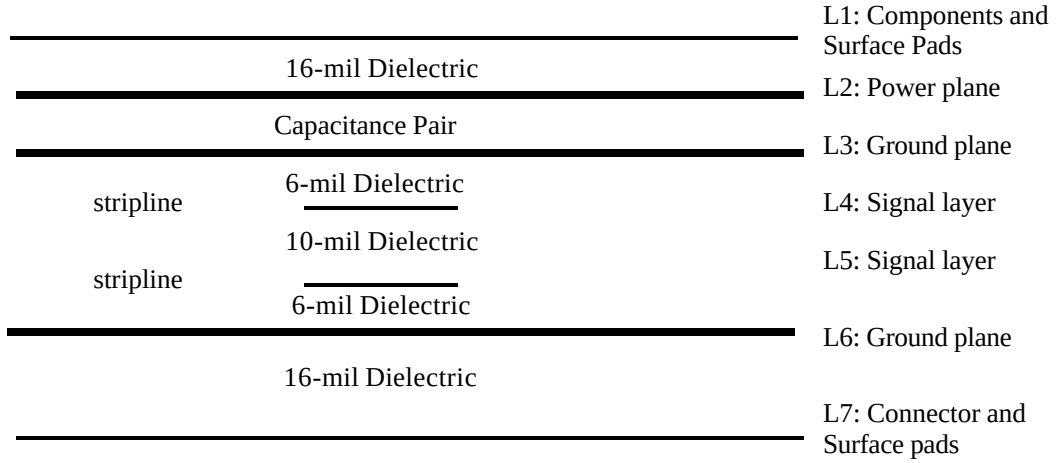

Figure 3.3 TV1-3-Y Stack-Up

As shown in Figure 3.1, TV1-1-Y boards had six layers with power and ground planes on Layers 3 and 4, respectively. The spacing between these two planes was nominally 4.5 mils when the boards were made with FR-4. TV1-2-Y boards also had six layers, but the power and ground planes were on Layers 2 and 5, respectively. Consequently, the spacing between power and ground planes was about 22 mils. The TV1-2-Y structure was only used in test boards made with FR-4. TV1-3-Y boards consisted of seven layers with a power plane on Layer 2 and two solid ground planes on Layers 3 and 6. Although this is not a typical layer stack-up, the purpose of the TV1-3-Y boards was to allow us to investigate the effects of layer placement within the stack-up and also the effect of shielding the signal traces between planes.

The spacing between layers varied slightly depending on the board manufacturer. The layer spacings indicated in Figures 3.1-3.3 are nominal values. Components were mounted on Layer 1 for all of the TV1 boards. A coaxial SMA connector was mounted on the backside (Layer 6 or 7) of each TV1 board. This connector was used to measure the voltage on the power and ground planes.

3.2 Layout of the TV1 test boards

There were three sizes of TV1 boards. There were also three board layouts corresponding to each of the three board sizes. The TV1-X-1 board (1-up board) contained the basic layout. All the components were placed in a 3-inch by 2-inch area as illustrated in Figure 3.4. The components consisted of an oscillator, a bulk decoupling capacitor, eight octal clock drivers, and a number of load capacitors. The fundamental frequency of the oscillator was 50 MHz. An SMA coaxial connector (J1) and a 2-pin connector (P1) provided electrical access to the power bus structure. The center conductor of the SMA connector was connected to the power plane while the outer shield was connected to the ground plane through 4 vias. The 2-pin connector had one pin connected to the power plane and the other pin connected to the ground plane. Both of these connectors were mounted on the bottom of the board (Layer 6 or 7), while the rest of the components were mounted on the top of the board (Layer 1).

A 50-MHz oscillator was used to drive the input pins of one of the octal clock drivers (U7). The clock drivers on U7 were used to drive all eight inputs on six of the remaining clock drivers. The outputs of these clock drivers were loaded with capacitors. The remaining clock driver was reserved for input current measurements and was not powered in the measurements described in the rest of this report.

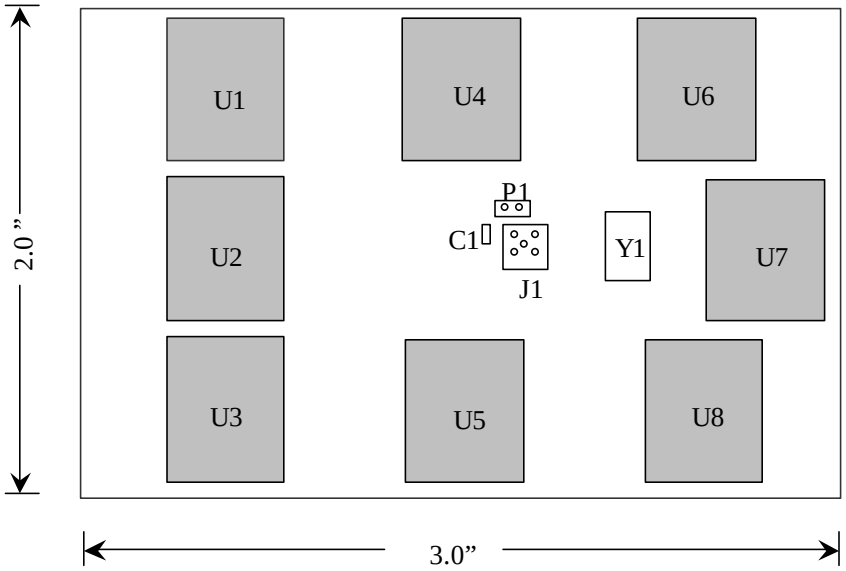

Figure 3.4 TV1-X-1 Board Layout

The TV1-X-4 board (4-up board) contained four copies of the 1-up board in a 6.1-inch by 4.1-inch area. This layout is illustrated in Figure 3.5. Although each of the circuits operated independently, the power and ground planes were solid (i.e. there was no gap in the planes between the different circuit areas). On some of the 4-up TV1 boards, all possible components were placed. These were designated “fully populated” boards. On other 4-up boards, only the top-left copy (as oriented in Figure 3.5) was populated. These were designated “one-copy populated” boards.

The TV1-X-12 board (12-up board) consisted of 12 copies of the 1-up board in a 9.3-inch by 8.6-inch area. The 12-up layout is illustrated in Figure 3.6. Again, the power and ground planes were solid. Some of the boards were fully populated, while one-copy-populated boards only had components in the circuit located on the second row, second column as oriented in Figure 3.6. The size of a 12-up board was approximately equal to the size of a personal computer motherboard.

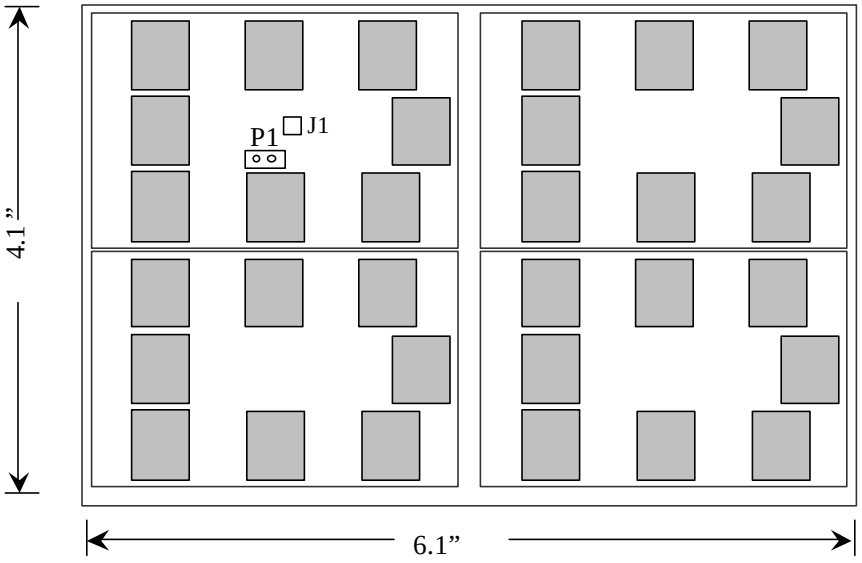

Figure 3.5 TV1-X-4 Board Layout

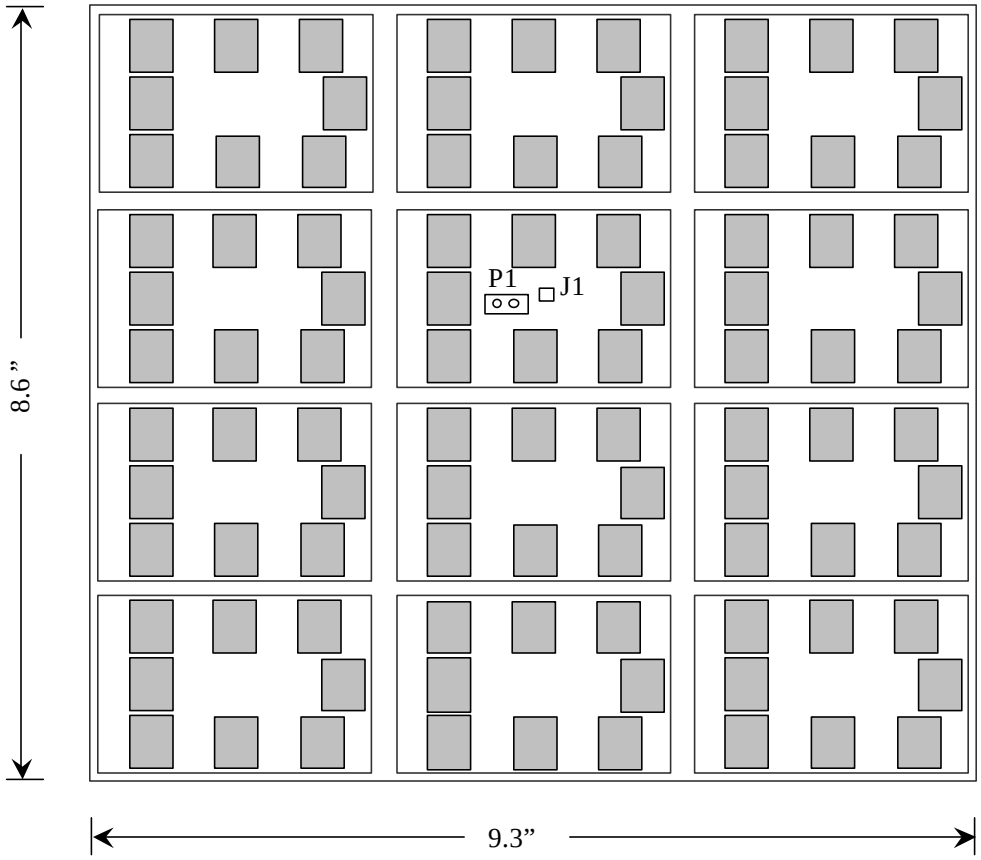

Figure 3.6 TV1-X-12 Board Layout

4. Impedance Measurements

Test boards with different embedded capacitance materials were evaluated using swept frequency measurements of the power bus input impedance. As indicated in Section 2, input impedance is perhaps the best indicator of how "good" or "bad" a power bus is in terms of minimizing power bus noise voltage. Actual power bus noise measurements with active components as the source are highly dependent on the exact frequency and location of the source. Swept frequency measurements are more likely to capture any resonant peaks in the board's response. Since components look like relatively high-impedance sources, the noise voltage at any point on the board due to a component drawing current at that point is directly proportional to the board impedance at that point. In this section, measured power bus impedance data is presented for both unpopulated and populated test boards.

4.1 Measurement setup

The power bus input impedance of TV1 boards was measured using an HP8753D network analyzer. The SMA connector on the test board was connected to Port 1 of the network analyzer through a low-loss precision cable. A one-port calibration was performed to set the measurement plane to the end of the coaxial cable. Then a port extension was performed with a shorted SMA connector to extend the measurement plane to the plane of the board. To make the shorted connector, the four outside conductor pins were removed from an SMA bulkhead connector. Then the center conductor and the shield of the connector were connected by a piece of copper tape and soldered together. Figure 4.1 shows a close-up view of the shorted connector.

Figure 4.1 Close-up of the Shorted Connector Used in Port Extension

S11 was measured and converted to an input impedance using a built-in function of the network analyzer. The measurements were performed between 30 kHz and 5 GHz. Figure 42.shows the experimental setup with the network analyzer and a 12-up TV1 board.

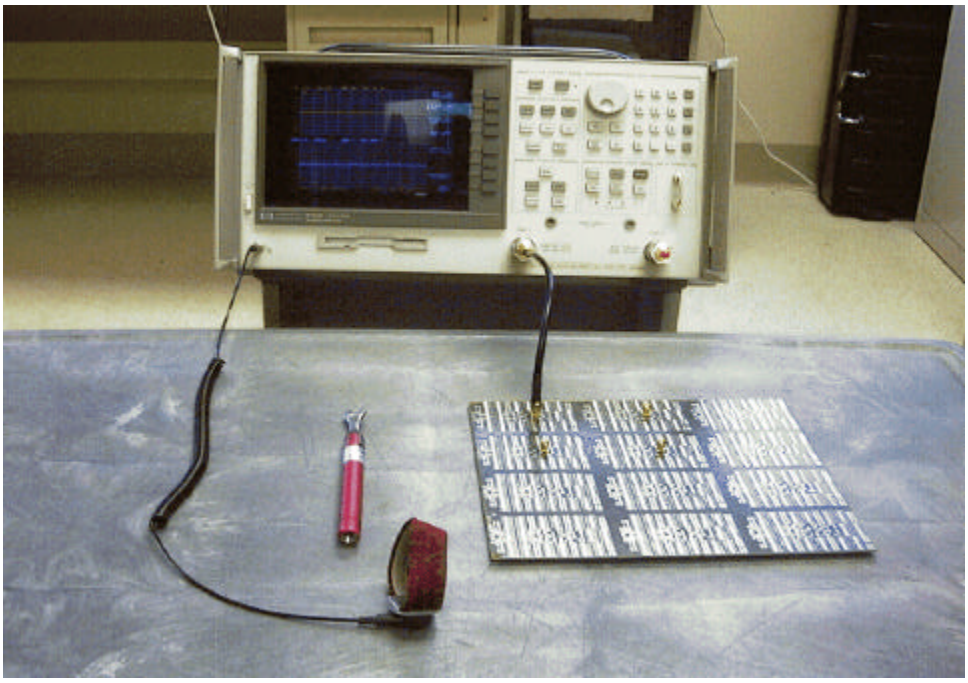

Figure 4.2 Experimental Setup for Power Bus Input Impedance Measurements

4.2 Input impedance of unpopulated test boards

For several months the only boards available for testing were unpopulated. This provided plenty of opportunity to study the behavior of boards that were relatively easy to model and to focus on the properties of the different embedded capacitance materials. Literally hundreds of measurements were taken and it would not be practical or helpful to present them all here. This section presents a selection of measurements that illustrate key points.

Figure 4.3 compares the input impedance of a TV1-2-1 FR-4 board with that of a TV1-1-1 EMCAP board. Resonant peaks in the power impedance are significantly damped in the EMCAP board. Damping of resonances is due to loss in the system as described in Section 2.4. However, the EMCAP material itself has a slightly lower loss tangent than FR-4. The damping is due to the relatively close spacing between the planes in the EMCAP board (4 mils as opposed to 19 mils for the TV1-2-1 FR4 board). According to the equations for the Q-factor presented in Section 2.4, the dominant loss mechanism in the EMCAP board is the copper loss in the planes. Q-factor calculations for the various boards tested during this project will be reviewed in Section 4.6. Figure 4.4 compares the input impedance of TV1-1-1 boards employing EMCAP and C-Ply

materials. The input impedance curve for the C-Ply board is even smoother than that of the EMCAP board.

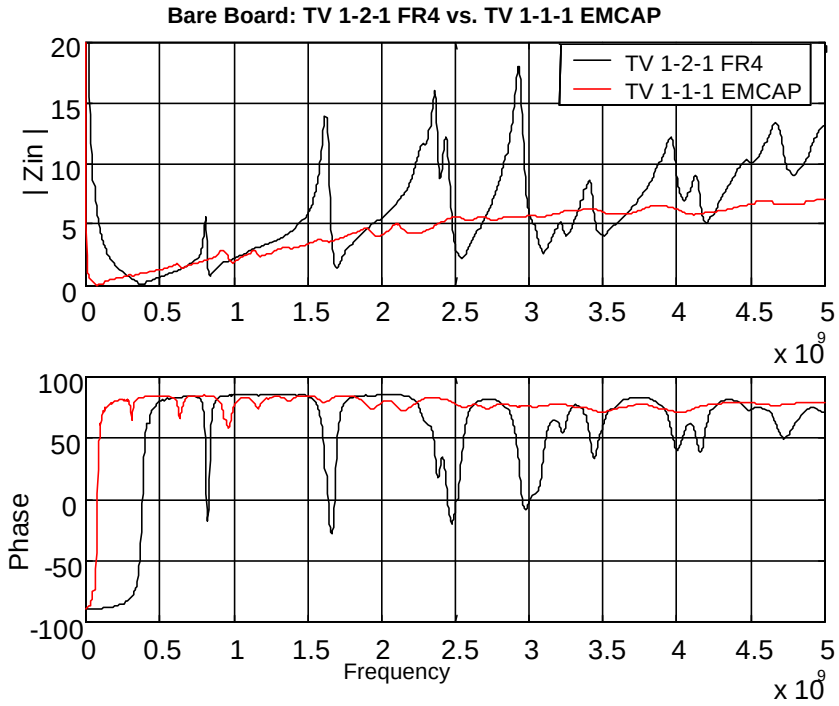

Figure 4.3 Input Impedance of Unpopulated Boards: TV 1-2-1 FR-4 vs. TV 1-1-1 EMCAP

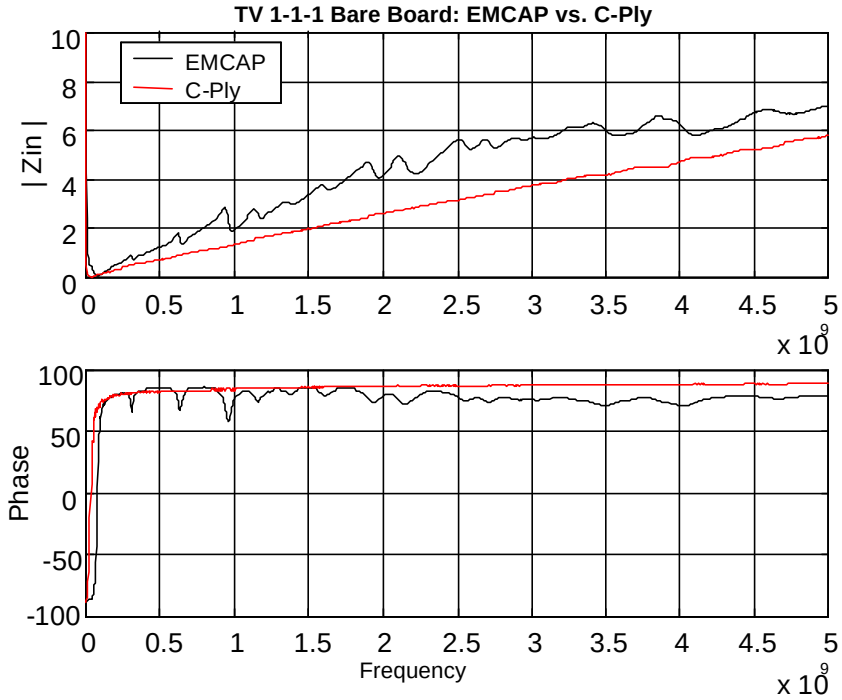

Figure 4.4 Input Impedance of Unpopulated TV 1-1-1 Boards: EMCAP vs. C-Ply

Figure 4.5 shows the input impedance of two FR-4 boards manufactured by Litton. These boards both have the same TV1-1-Y stack-up. One is a 4-up board and one is a 12-up board. The power-ground plane spacing in both these boards is 7 mils. The impedance curve for the 12-up board is slightly smoother.

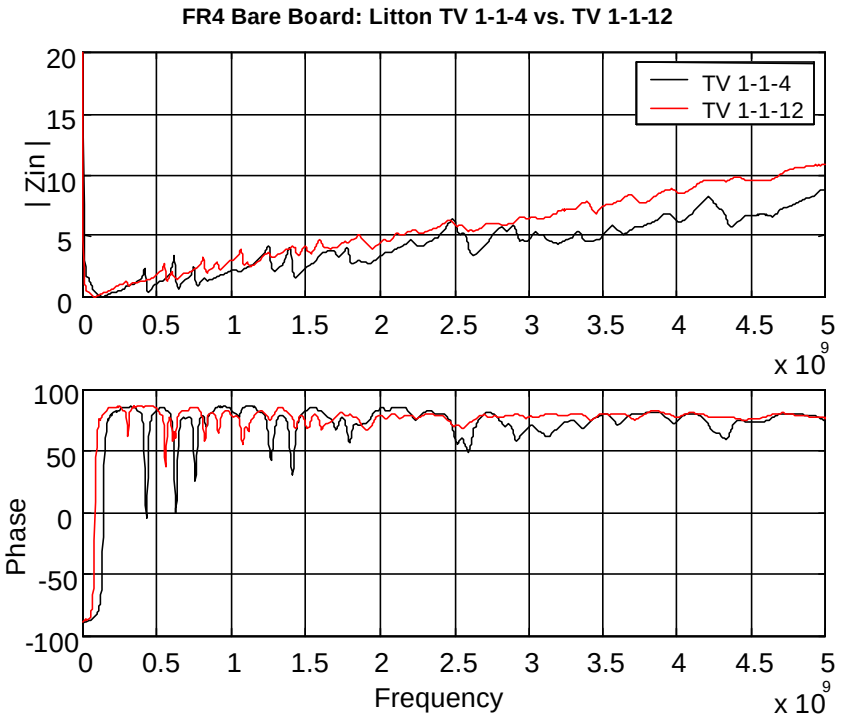

Figure 4.5 Input Impedance of Litton FR-4 Bare Boards: TV 1-1-4 vs. TV 1-1-12

Figure 4.6 shows the input impedance measured for three sizes of EMCAP boards. All the boards employed exactly the same TV1-1-Y stack-up. Again, the resonance peaks for 12-up board are slightly more damped than the resonance peaks in the smaller boards.

Figure 4.7 shows the input impedance of two EMCAP boards with different stack-ups. The power-ground plane pair in a TV1-3-1 board is on layers 2 and 3. The power-ground plane pair in a TV1-1-1 board is on layers 3 and 4. These impedance curves are nearly identical, except that the TV1-3-1 board's curve has a slightly higher slope. This slope is due to the inductance of the SMA connector's connection to the planes. This connection inductance is described more fully in Section 4.7.

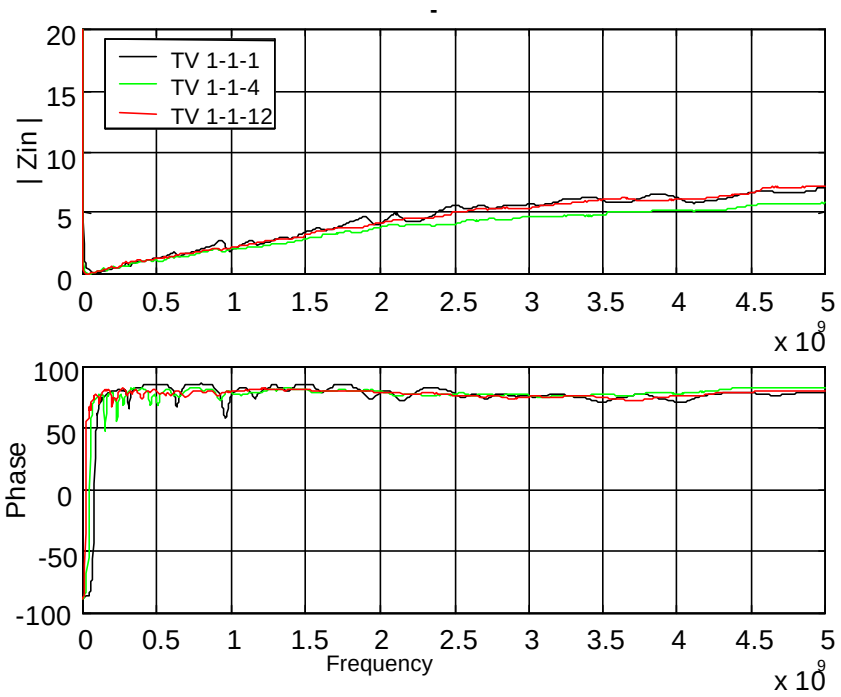

Figure 4.6 Input Impedance of Unpopulated 6-Layer EMCAP Boards with Different Sizes

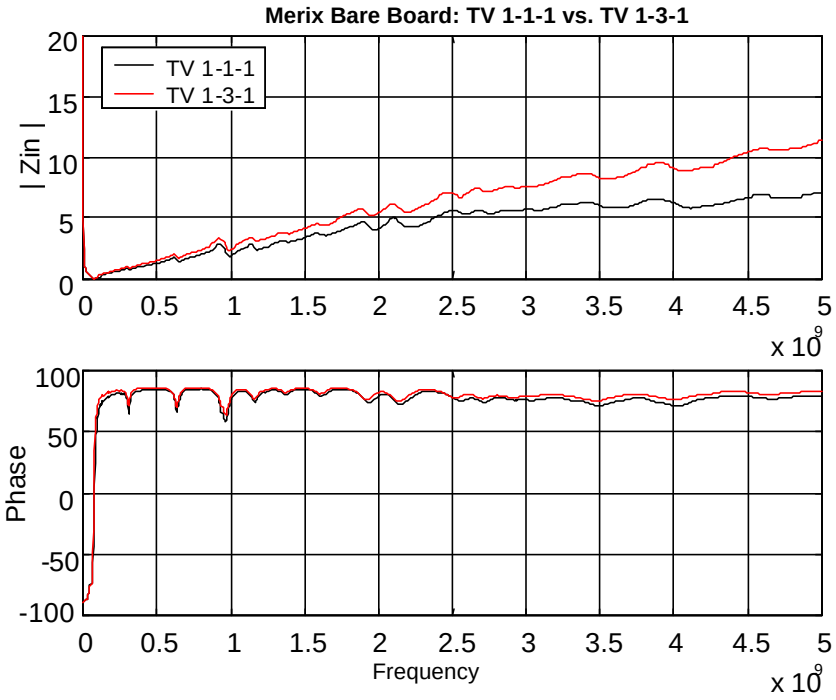

Figure 4.7 Input Impedance of Unpopulated EMCAP Boards: TV 1-1-1 vs. TV1-3-1

4.3 Input impedance of populated FR-4 test boards

Figure 4.8 shows the input impedance of two TV1-1-1 FR-4 boards manufactured by Raytheon. The board without decoupling capacitors has a sharp resonance peak below 200 MHz. This is not a board resonance, but rather a resonance between the board's inter-plane capacitance and the inductance of the connections to devices mounted on the surface. At low frequencies, the decoupling capacitors do a good job of eliminating this resonance. However, above 100 MHz, all of the surface decoupling capacitors have too much connection inductance to be effective. There is no significant difference between these two curves above 100 MHz other than a slight shift in the resonance frequencies.

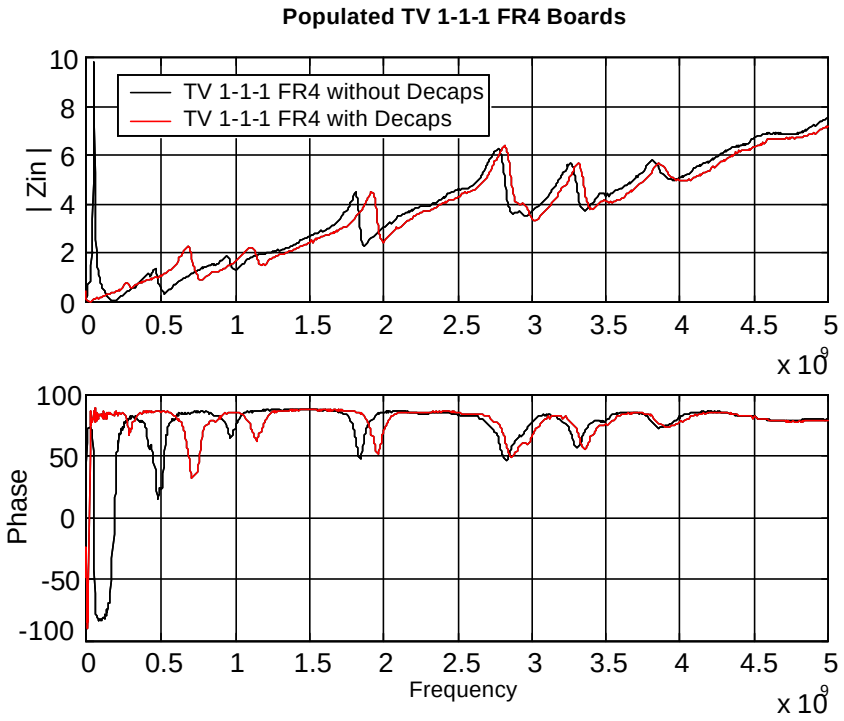

Figure 4.8 Input Impedance of TV1-1-1 FR-4 boards: with/without Decoupling Capacitors

Figure 4.9 shows the input impedance of TV1-2-1 FR-4 boards manufactured by Merix with and without local decoupling capacitors. Again, the sharp low frequency peak (which is not a board resonance) is eliminated by adding discrete decoupling capacitors. As described in Section 3, TV1-2-1 boards have a much wider power-ground plane spacing than TV1-1-1 boards. Since the inter-plane capacitance is smaller, the decoupling capacitors have more of an effect. However notice that on average they still do not reduce power bus impedance above about 1000 MHz.

Figure 4.10 compares the measured power bus impedance of two Merix TV1-2-1 FR-4 boards. One is an unpopulated sample; the other is populated with components but without any

decoupling capacitors. With components mounted to the board, the resonances are significantly damped, but not eliminated. Components introduce a loss that can be significant in heavily populated boards. Although we currently do not have an accurate means of predicting this loss, measurements with the TV1 boards indicate that the component loss is small relative to the copper loss in the planes for boards with embedded capacitance.

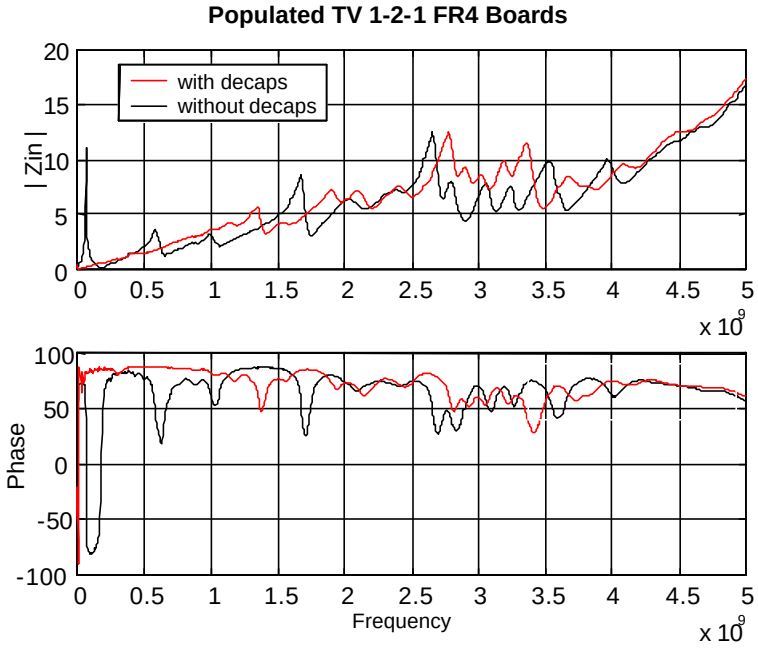

Figure 4.9 Input Impedance of TV1-2-1 FR-4 boards: with/without Decoupling Capacitors

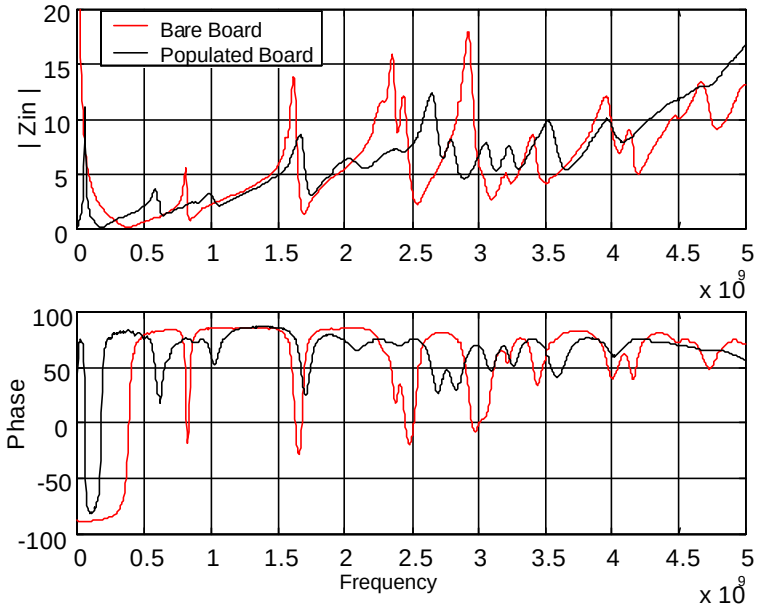

Figure 4.10 Input Impedance of TV1-2-1 FR-4 Boards: Bare Board vs. Populated Board

4.4 Input impedance of populated test boards with embedded capacitance

The input impedance of populated TV1-1-1 boards employing different dielectric materials is plotted in Figure 4.11. The test samples include a TV1-1-1 FR-4 board manufactured by Raytheon (without decoupling capacitors); a TV1-1-1 BC2000 board manufactured by Litton; a TV1-1-1 Hi-K board manufactured by Litton; a TV1-1-1 EMCAP board manufactured by HADCO; and a TV1-1-1 C-Ply board manufactured by 3M. The FR-4 board has the most significant peaks at power bus resonant frequencies, while the impedance curve for the C-Ply board is a rather smooth upward slope. This slope is due to the inductance of the SMA connector's attachment to the planes.

Figure 4.12 is a magnified view of the lower-frequency portion of Figure 4.13. It shows the low-frequency resonance resulting from the interaction between the component inductance and the inter-plane capacitance. Notice that as the inter-plane capacitance increases, the resonance shifts to a lower frequency and becomes more damped. This is exactly the behavior predicted by simple lumped element models of the power bus structure.

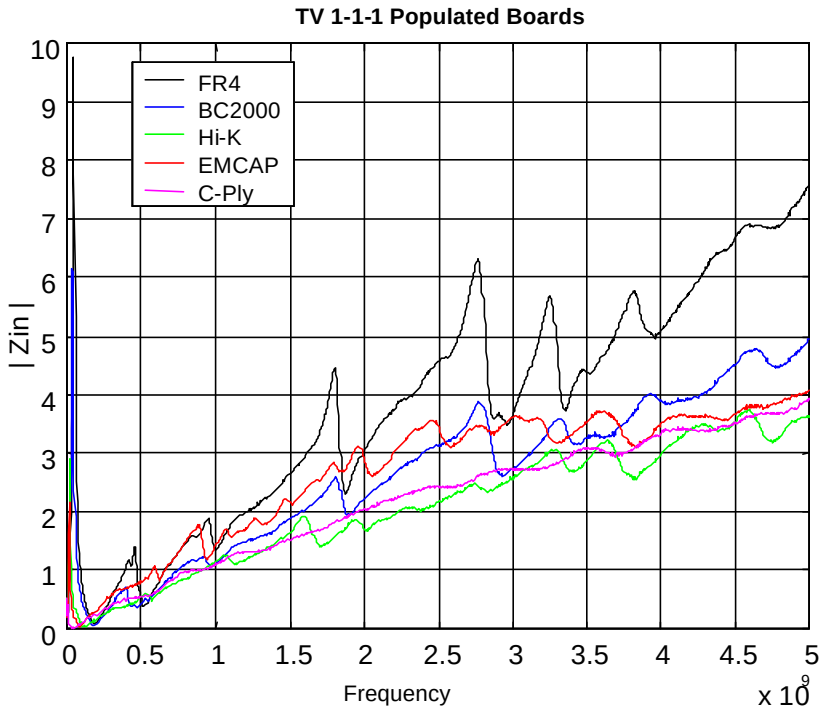

Figure 4.11 Input Impedance of TV 1-1-1 Boards Employing Different Materials

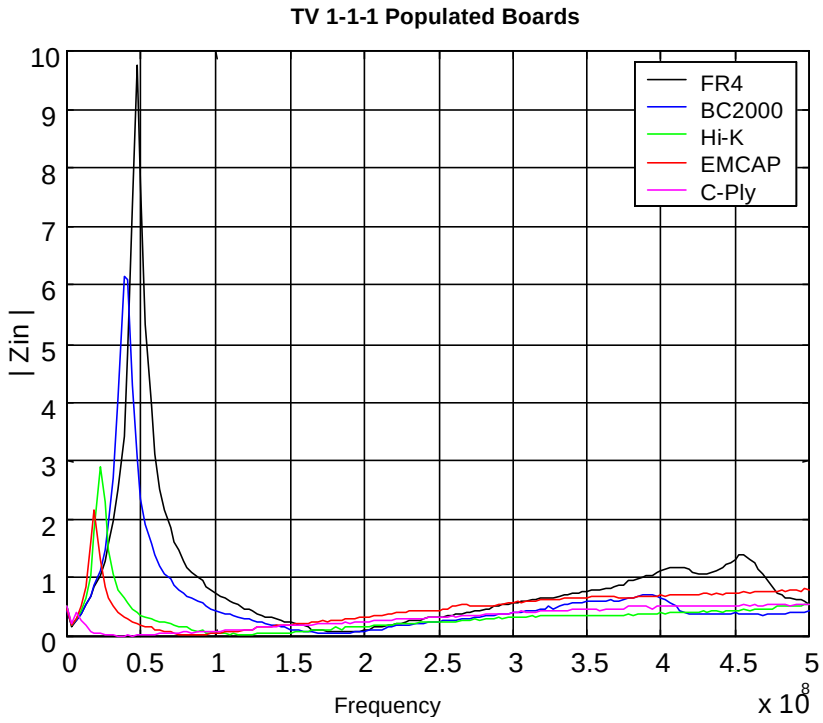

Figure 4.12 Input Impedance of TV1-1-1 Boards below 500 MHz

4.5 Resonant frequency analysis

The measured input impedance of an unpopulated printed circuit board is plotted in Figure 4.13.

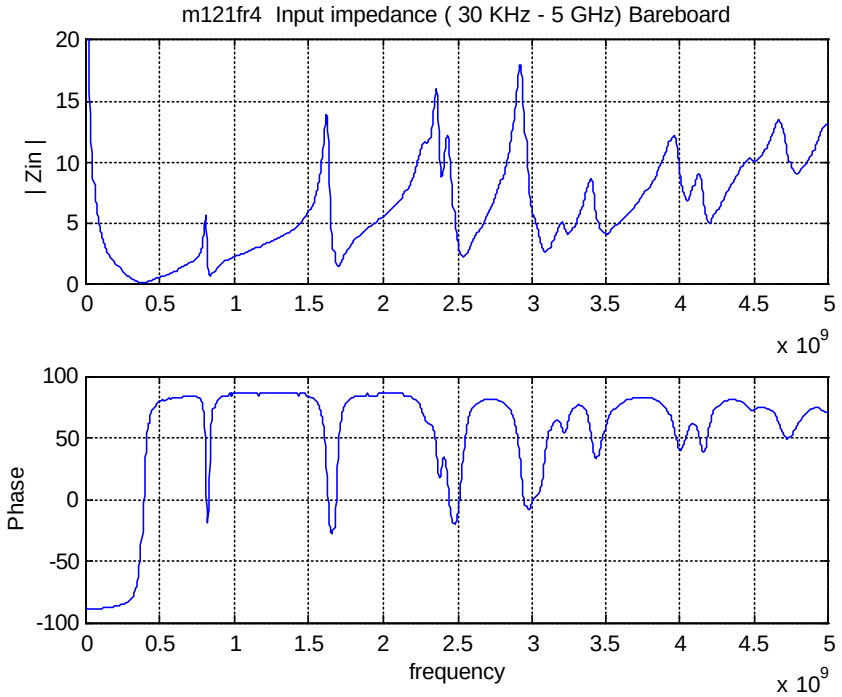

Figure 4.13 Input Impedance of an Unpopulated TV1-2-1 FR-4 Board

As previously indicated, this test board was 3 inches long and 2 inches wide. The ground and power planes were on Layers 2 and 5, respectively. Between the two solid planes, there was a 19.4-mil FR-4 dielectric layer. The relative permittivity of the dielectric layer was about 5 and the total board capacitance was about 350 pF. The structure was fed by an SMA jack located at (1.1", 1.0"). The radius of the center conductor of the SMA jack was 25 mils. Figure 4.13 indicates that the test board behaved like a capacitance at very low frequencies. It exhibited a series resonance at 387 MHz and at higher frequencies the input impedance was inductive except at the resonance frequencies.

At low frequencies, the lumped circuit model for the unpopulated board is simply the board capacitance. As the frequency approaches the series resonance at 387 MHz, the length of the test board is more than one-fifth of a wavelength. To characterize the input impedance at frequencies above 387 MHz, we can switch from the lumped element model to the modal expansion cavity model. The first few cut-off frequencies predicted by the cavity model are listed in Table 4.1.

Table 4.1 Resonance Frequencies Calculated for the TV1-2-1 FR-4 Bare Board (MHz)

TM 10	TM 01	TM 11	TM 20	TM 21	TM 02	TM 30	TM 12	TM 31
883	1315	1584	1765	2201	2631	2648	2775	2957
TM 22	TM 40	TM 32	TM 41	TM03	TM13	TM 23	TM 42	TM 50
3168	3531	3733	3768	3946	4044	4323	4403	4413

Due to the location of the measurement port, some modes were not excited and do not appear in the measured input impedance. In addition, a frequency shift is observed between the calculated cut-off frequencies and the measured results. For example, the first cavity resonance was measured at 825 MHz, while the cavity model prediction was 883 MHz. These shifts are primarily due to fringing effects. The field does not stop abruptly at the edge of the board as the cavity model assumes. Fringing fields at the board edge make the board appear slightly larger than it really is resulting in a downward shift in the resonance frequencies. Fringing is more of a factor in boards that have greater plane spacing or smaller board areas. The 1-up samples had the smallest dimensions among the three layouts, and the TV1-2 stack-up had the widest plane spacing. Consequently, the TV1-2-1 FR-4 sample exhibited the largest frequency shift due to fringing effects.

4.6 Quality factor analysis

For test boards employing embedded capacitance materials, the input impedance curves were relatively smooth with small ripples at resonance frequencies. The FR-4 board exhibited significant peaks at power bus resonant frequencies. Several resonant peaks and nulls are also evident in the BC2000 curve. Ripples in the EMCAP and Hi-K curves are less pronounced. The C-Ply curve is nearly a straight line. All of the TV1 boards employing embedded capacitance materials significantly damped power bus resonances, however some boards clearly performed better than others.

As discussed in Section 2.4, the magnitude of input impedance near resonance frequencies is related to the quality factor of the power-ground plane structure. The relative permittivities and loss tangents of the embedded capacitance materials were measured by NIST at several frequencies. Table 4.2 shows the calculated resonant frequency of the TM_{10} mode for several of the TV1 configurations tested. Estimated values for the relative permittivity and the loss tangent at this resonant frequency (based on the NIST results) are also provided in this table.

Table 4.2 Geometry and Material Parameters of Populated TV1 Test Boards

Sample	Length (cm)	Width (cm)	Thickness (mil)	ε_r	Loss tand	f_{10} (MHz)
Merix TV1-2-1 FR-4	7.6	5.1	19.4	3.92	0.021	997
Raytheon TV1-1-1 FR-4	7.6	5.1	4.5	3.92	0.021	997
Litton TV1-1-4 FR-4	15.7	10.6	3.3	4.13	0.023	470
Litton TV1-1-12 FR-4	23.8	21.8	3.3	4.13	0.023	310
HADCO TV1-1-1 BC2000	7.6	5.1	2.1	3.88	0.021	1002
Litton TV1-1-4 BC2000	15.7	10.6	2.1	3.93	0.024	482
Litton TV1-1-12 BC2000	23.8	21.8	2.1	3.93	0.024	318
HADCO TV1-1-1 EMCAP	7.6	5.1	4	36.30	0.0151	328
Merix TV1-1-4 EMCAP	15.7	10.6	4	36.30	0.0168	159
Merix TV1-1-12 EMCAP	23.8	21.8	4	36.60	0.0182	104
Litton TV1-1-1 Hi-K	7.6	5.1	1.4	12.10	0.011	567
Litton TV1-1-4 Hi-K	15.7	10.6	1.4	11.90	0.0082	277
Litton TV1-1-12 Hi-K	23.8	21.8	1.4	11.90	0.0082	183
3M TV1-1-1 C-Ply	7.6	5.1	0.5	21.50	0.0436	426
3M TV1-1-4 C-Ply	15.7	10.6	0.5	21.50	0.0436	206

Using these geometry and material parameters, the quality factors related to the dielectric loss, the conductive loss, and the radiation loss were calculated for the dominant TM_{10} mode for each test board. The total quality factor for the TM_{10} mode of each test board was calculated from these three partial quality factors using Equation (14). The results are summarized in Table 4.3.

As the data in Table 4.3 indicates, the radiation loss is relatively small compared to the dielectric loss and conductive loss for all test boards (i.e. Q_{rad} was much higher than Q_d or Q_c). Radiation loss had little effect on the total quality factor for the TM_{10} mode.

The quality factors due to the conductive loss and the dielectric loss were generally of the same order of magnitude for the boards tested. The dominant loss depended on the thickness of the dielectric. Q_c is proportional to the thickness of the dielectric layer and proportional to the square root of the frequency while Q_d is independent of thickness and nearly independent of frequency. For power-ground plane structures with very thin dielectric layers, especially at low frequencies, conductive loss is the dominant factor. At higher frequencies and in thicker materials, the quality factor is generally dominated by the dielectric loss of the material. Higher loss equates to more effective dampening of the power-ground structure resonances especially at high frequency.

Table 4.3 Quality Factors of TV1 Test Boards

Samples	f_{10} (MHz)	Q_d	Q_c	Q_{rad}	Total Q
Merix TV 1-2-1 FR-4	997	47.6	235.4	1582	38.64
Raytheon TV 1-1-1FR-4	997	47.6	54.6	6819	25.34
Litton TV 1-1-4 FR-4	470	43.5	27.5	21312	16.83
Litton TV 1-1-12 FR-4	310	43.5	22.3	25265	14.75
HADCO TV 1-1-1 BC2000	1002	47.6	25.5	14302	16.61
Litton TV 1-1-4 BC2000	482	41.7	17.7	29713	12.43
Litton TV 1-1-12 BC2000	318	41.7	14.4	35790	10.69
HADCO TV 1-1-1 EMCAP	328	66.2	27.8	7.17E+05	19.59
Merix TV 1-1-4 EMCAP	159	59.5	19.4	1.47E+06	14.61
Merix TV 1-1-12 EMCAP	104	54.9	15.7	1.77E+06	12.21
Litton TV 1-1-1 Hi-K	567	90.9	12.8	2.23E+05	11.23
Litton TV 1-1-4 Hi-K	277	122.0	9.0	4.36E+05	8.34
Litton TV 1-1-12 Hi-K	183	122.0	7.3	5.25E+05	6.86
3M TV 1-1-1 C-Ply	426	22.9	4.0	2.00E+06	3.38
3M TV 1-1-4 C-Ply	206	22.9	2.8	4.04E+06	2.46

According to Table 4.3, all test boards employing embedded capacitance materials have smaller quality factors (higher loss) than the corresponding FR-4 version for the dominant TM_{10}

mode. The quality factor of the TV1-1-1 C-Ply board was about one-eighth that of the TV1-1-1 FR-4 board. This low quality factor resulted in the smooth input impedance curves in Figure 4.11. A Q-factor of 1 implies the board is well damped and exhibits no resonant peaks.

4.7 Probe inductance

The input impedance curves of test boards with low quality factors are characterized by an upward-sloping line with ripples at cavity resonance frequencies. To investigate the source of the slope, the input impedance of two unpopulated Merix EMCAP boards is plotted in Figure 4.14 and the input impedance of two populated Litton Hi-K boards is plotted in Figure 4.15. All four samples were 1-up boards. In both plots, the difference between two curves is the layer stack-up of the test boards. The TV1-3 stack-up exhibits a steeper slope than the TV1-1 stack-up.

A linear change in the magnitude with frequency and a 90-degree phase suggest the measured impedance is a constant inductance. TV1-1-Y boards had six layers with power and ground planes on Layers 3 and 4, respectively. TV1-3-Y boards consisted of seven layers with a power plane on Layer 2 and solid ground planes on Layers 3 and 6. TV1-1 test boards and TV 1-3 test boards made with the same embedded capacitance material had identical plane-to-plane spacing. In both stack-ups, the components were placed on Layer 1. The SMA jacks used to make measurements were mounted on the opposite side of the boards. In both cases, the center wire of the SMA connector was connected to the power plane, and the four side pins were connected to a ground plane. Figure 4.16 and Figure 4.17 illustrate these two layer stack-ups with the SMA connector. From the illustration, it is apparent that the “connection inductance” of TV1-3 stack-ups is higher than that of the TV1-1 stack-ups. For test boards with low quality factors, this connection inductance was the dominant factor affecting the measured input impedance. The slope of the input impedance curve is approximately proportional to the connection inductance. This connection inductance was approximately 350 pH for the TV1-3-1 EMCAP board and 120 pH for the TV1-1-1 Hi-K board.

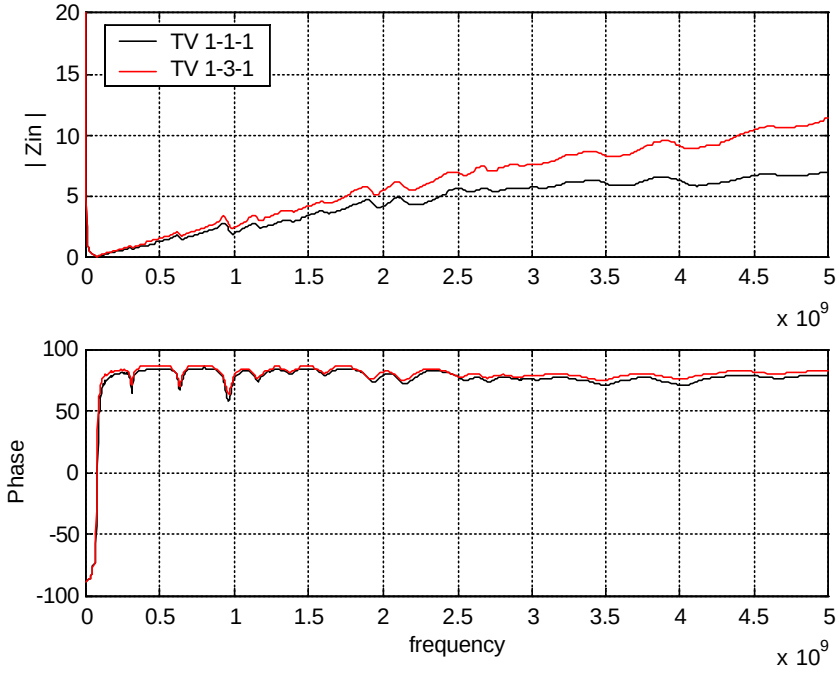

Figure 4.14 Input Impedance of Unpopulated Merix EMCAP Boards: TV 1-1-1 vs. TV1-3-1

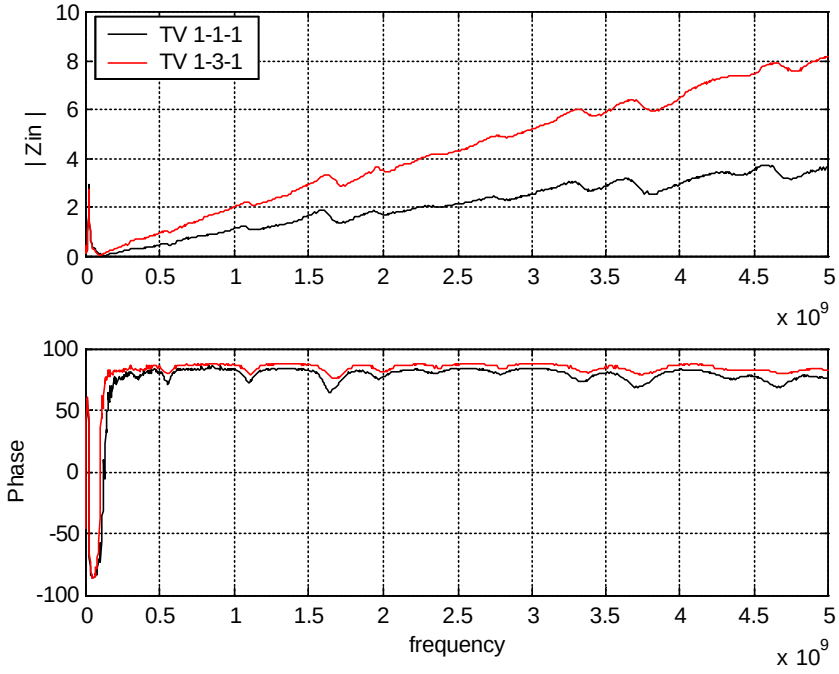

Figure 4.15 Input Impedance of Populated Litton Hi-K Boards: TV1-1-1 vs. TV1-3-1

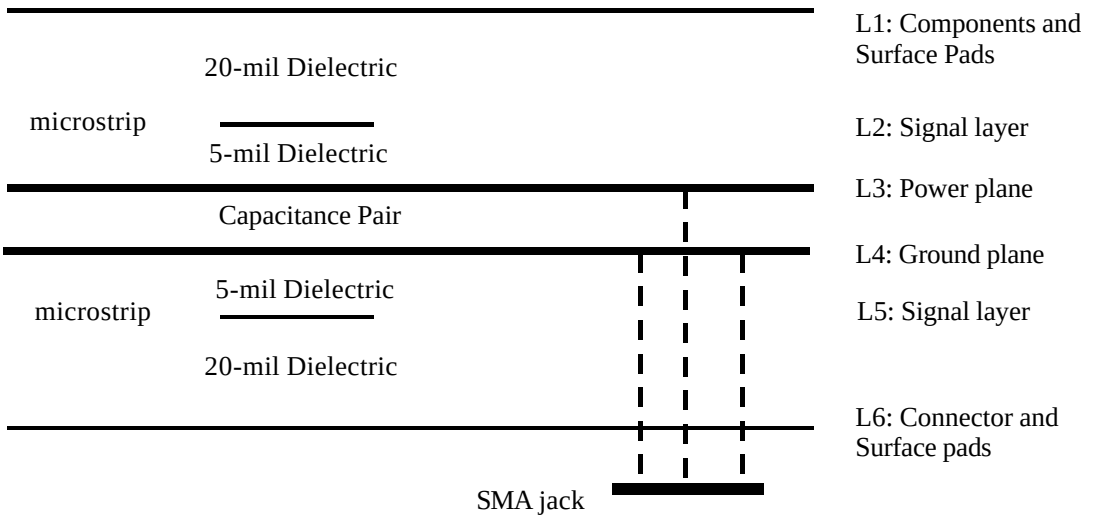

Figure 4.16 Probe position for TV1-1-Y Stack-Up

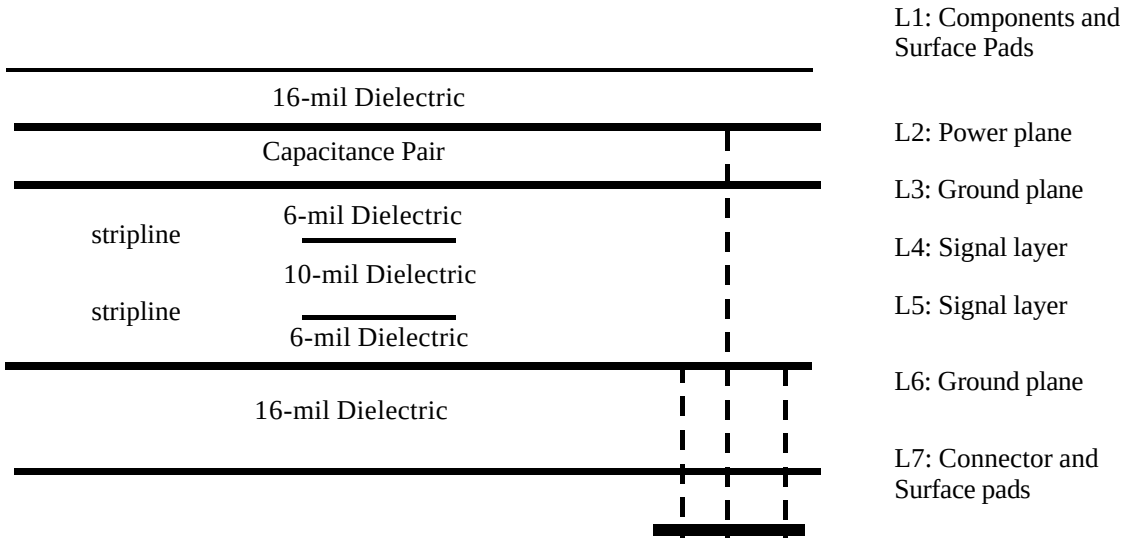

Figure 4.17 Probe position for TV1-3-Y Stack-Up

4.8 Input impedance measurements summary

Based on the measurement results presented in this chapter, it is clear that a key factor affecting the value of the input impedance is the Q-factor, which affects the height of resonant peaks. All of the test boards with embedded capacitance exhibited power bus resonances that were significantly damped relative to standard FR-4 boards. The dominant source of loss was the copper loss, which is inversely proportional to the plane spacing (i.e. thinner materials result in higher copper losses).

For test boards with the same material and the same stack-up, larger boards exhibited slightly lower resonant peaks. However, this effect was minor compared to the effect of the plane spacing. Active components on the board also contributed to the overall loss and significantly reduced the resonant peaks on FR-4 boards. However, on the boards with very small plane spacing, the effect of the component loss was minor. With the resonances well damped, the measured input impedance was dominated by the connection inductance.

5. Time Domain Measurements

This section examines power bus noise measurements made in the time domain using an oscilloscope. First, the experimental setup is described then measurement results are presented. Measured results are summarized at the end of the section.

5.1 Measurement setup

To power the one-copy populated test boards, an HPE3630A DC power supply set to 3.3 volts was connected to the 2-pin plug on the test board through a 0.6-m unshielded twisted wire pair. Fully populated 4-up and 12-up test boards required levels of current that exceeded the capacity of the HPE3630A; so, an HP6575A DC power supply was used to power these boards. Two solid thick wires were twisted and soldered to the test boards to deliver the necessary current. An unshielded twisted pair was connected to the 2-pin plug and used to sense the voltage drop across the test boards. This feedback helped the power supply to maintain a constant voltage.

The power bus noise voltage was measured using a Tektronix TDS520A two-channel digitizing oscilloscope. The test board was hooked to Channel 1 of the oscilloscope using the on-board SMA connector. One-up boards were mounted directly to the face of the oscilloscope. Larger boards were connected through a low-loss precision coaxial cable. The oscilloscope input was AC coupled and the input impedance was set to 50 ohms. The measured waveforms for the one-copy populated test boards were very smooth, so they could be directly recorded. However, high frequency noise in the measurement results for the fully populated 4-up and 12-up boards required averaging of the measured waveform in order to compare one board to another. The final waveform was determined by averaging 401 frames. The experimental set-up for the one-copy populated boards is shown in Figure 5.1.

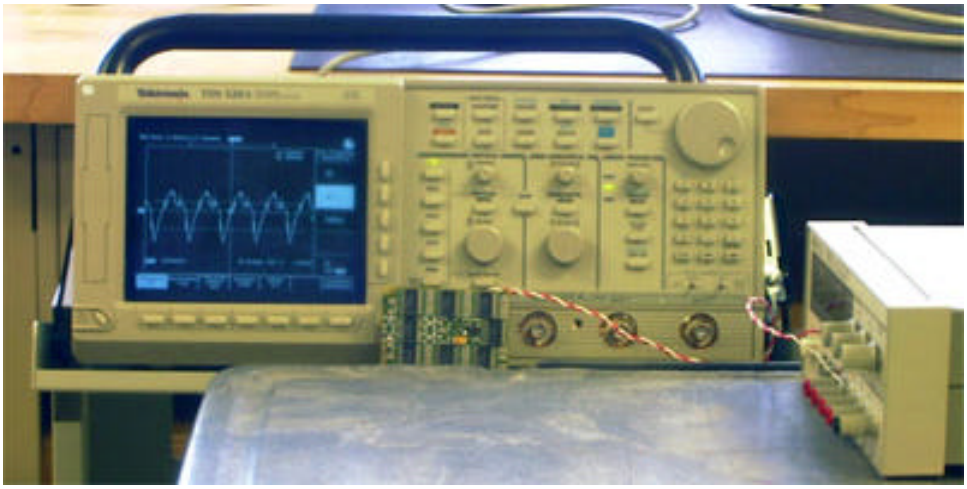

Figure 5.1 Experimental Setup for Time Domain Power Bus Noise Measurement

5.2 Time domain power bus noise measurements

Most of the energy in a digital waveform is concentrated in the lower harmonics. Therefore, time domain power bus noise measurement results exhibited a strong 50-MHz component with identifiable 100 and 150 MHz artifacts. Figure 5.2 compares the power bus noise voltage measurements for TV1-2-1 FR-4 boards with and without local decoupling capacitors.

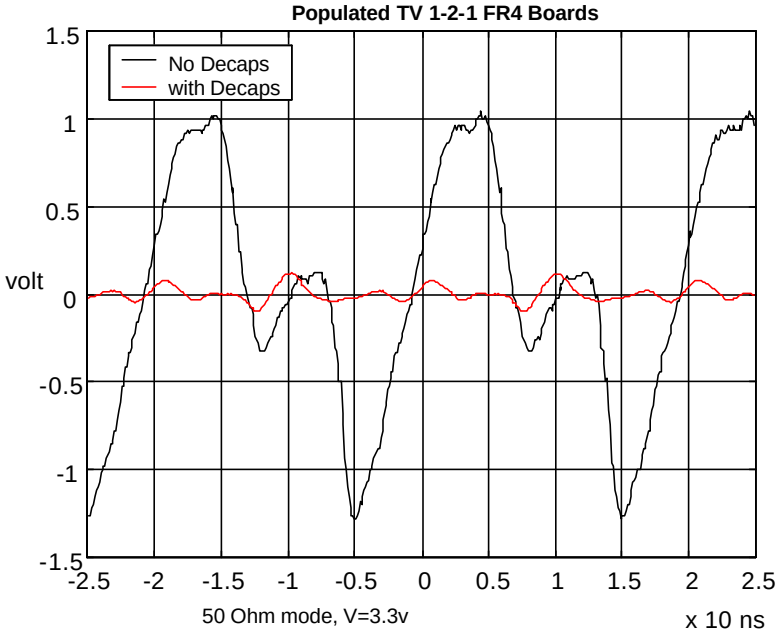

Figure 5.2 Power Bus Noise on TV1-2-1 FR-4 Boards with/without Decoupling Capacitors

The peak-to-peak noise voltage is more than 2 volts for the board without decoupling capacitors. As might be expected, this board had trouble operating consistently. On the board with

decoupling capacitors, the peak-to-peak noise voltage is about 0.2 volts. This dramatic improvement reflects the fact that the local decoupling capacitors are a very effective source of current at 50 MHz and the lower harmonic frequencies. This result also demonstrates that it is very important to supply adequate decoupling capacitance in order for printed circuit boards to work properly.

Figure 5.3 compares the noise voltage waveforms of several 1-up test boards with different materials. None of these boards has local decoupling capacitors mounted. Note that embedded capacitance is just as effective (actually more effective) as an equivalent amount of capacitance mounted on the board's surface. For example, the peak-to-peak magnitude of the noise voltage for the TV1-3-1 C-Ply board is less than 0.1 volt. This was slightly lower than the noise voltage on the FR-4 boards with local decoupling capacitors.

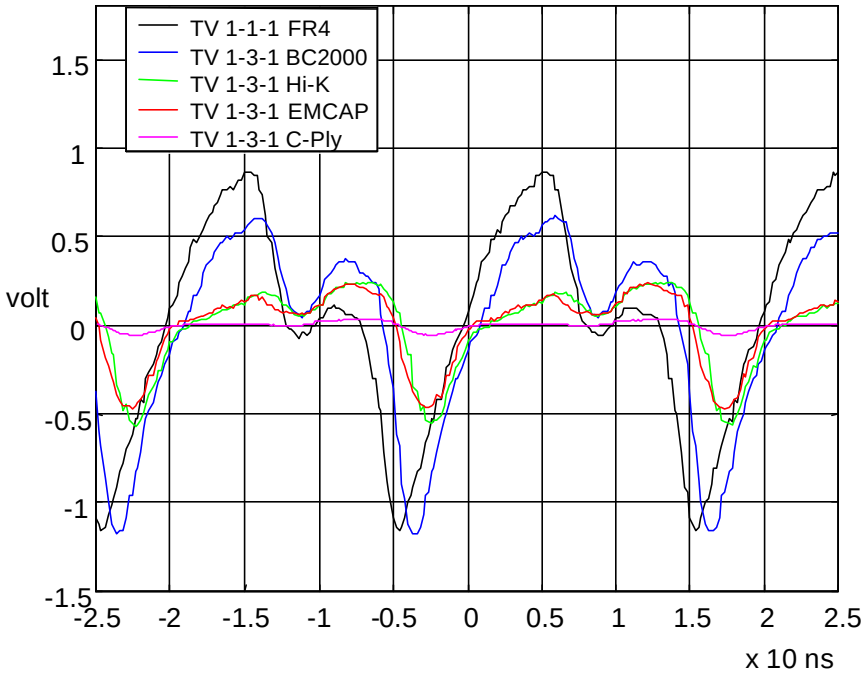

Figure 5.3 Power Bus Noise on 1-up Boards with Different Materials

At 50 MHz and the lower harmonic frequencies, the noise voltage should be inversely proportional to the total available decoupling capacitance (according to lumped element models). For test boards employing the same dielectric materials, increasing the board area also increases the inter-plane capacitance. Consequently, for one-copy populated samples, a 4-up board should have approximately one fourth the noise voltage of a 1-up board. A 12-up board should have

approximately one-twelfth the noise voltage of a 1-up board. This is demonstrated in Figure 5.4, which compares the measured noise on three one-copy populated TV1-1 Hi-K boards.

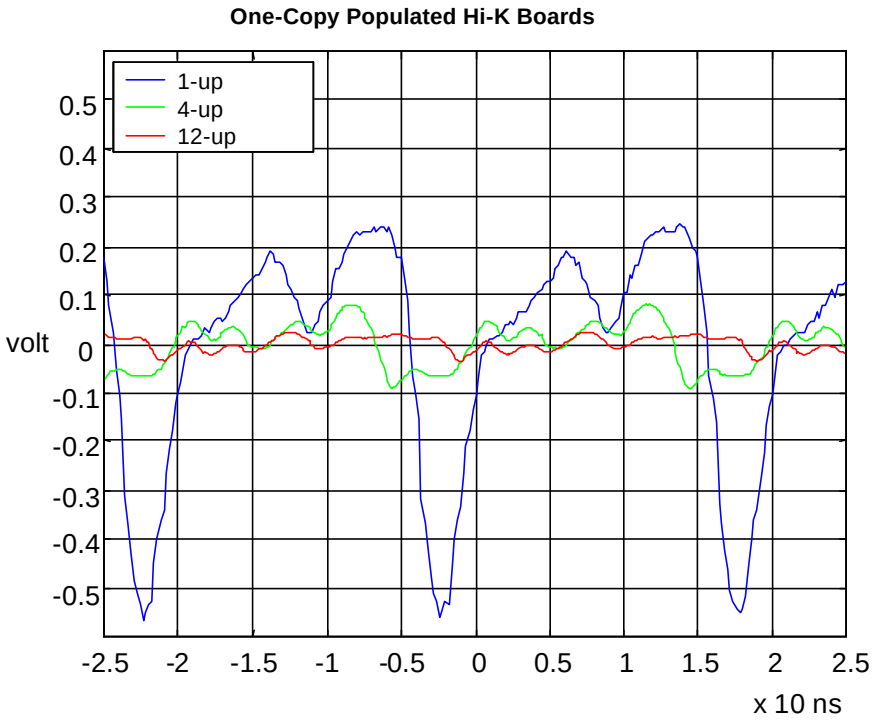

Figure 5.4 Power Bus Noise on One-Copy Populated Boards with Different Dimensions

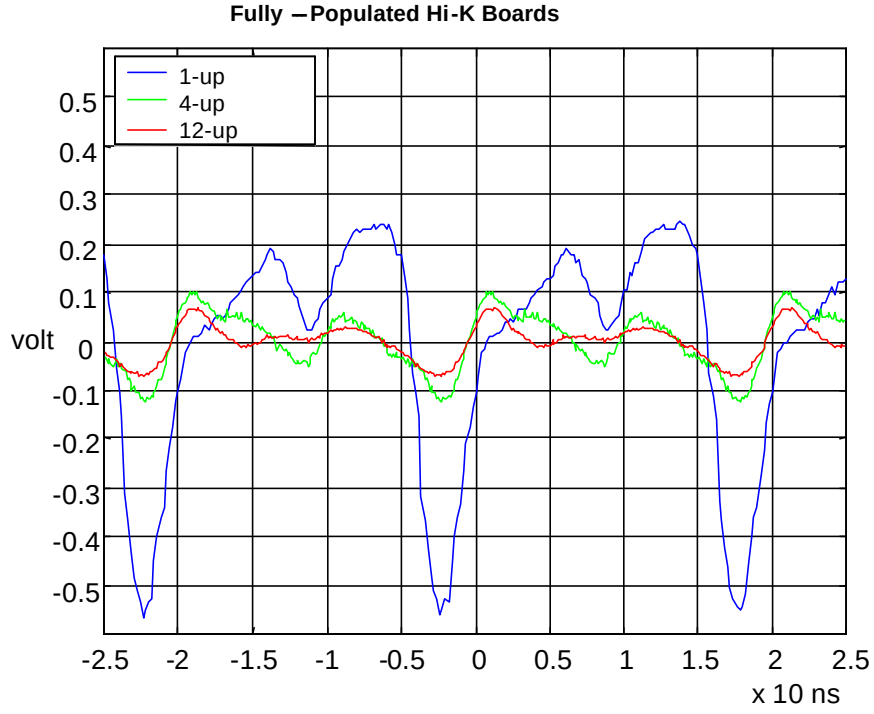

Figure 5.5 Power Bus Noise on Fully Populated Boards with Different Dimensions

Figure 5.5 compares the noise voltage on three fully populated Hi-K boards. It is interesting to note that the magnitude of the noise voltage for 4-up and 12-up fully populated boards was smaller than that for the 1-up board, but higher than the noise voltage for their one-copy populated counterparts. The magnitude of the noise voltage was not simply proportional to the number of the populated circuits on the test boards. This effect will be examined more closely in the next section.

It was also observed that the stack-up had little effect on the time domain noise voltage. The measurement results for two 4-up one-copy populated EMCAP boards with different stack-ups are compared in Figure 5.6. The two curves are so close that they nearly lay on top of each other. This result is to be expected, since the connection inductance has a negligible effect at 50 MHz and the frequencies of the first few harmonics.

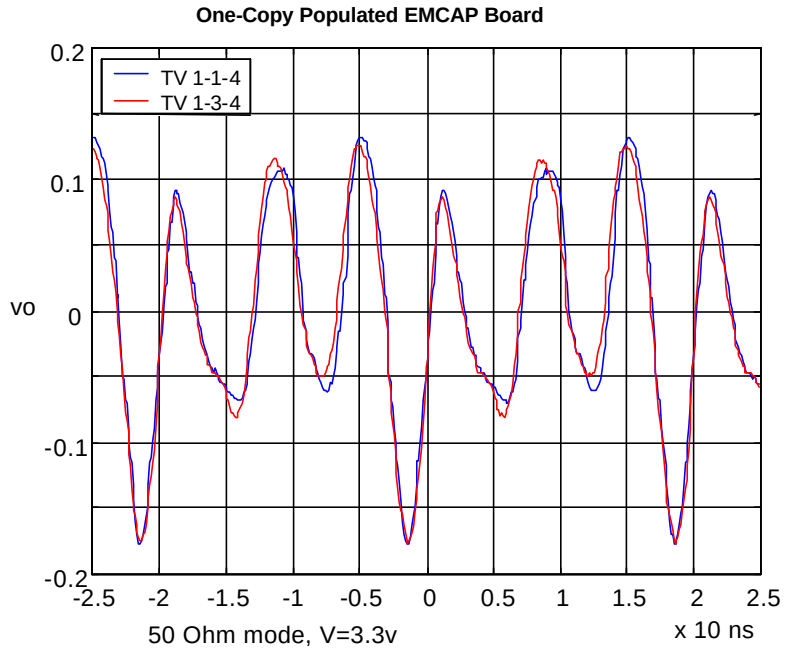

Figure 5.6 Power Bus Noise on One-Copy Populated EMCAP Boards: TV1-1-4 vs. TV1-3-4

In summary, the time domain noise measurements are dominated by the effects of the decoupling at the first few harmonics of the signal. As the results indicate, it is critical to provide enough decoupling capacitance to ensure the correct operation of the board. This decoupling capacitance can be achieved by adding decoupling capacitors or by taking advantage of the available inter-plane capacitance. All embedded materials tested exhibited lower power bus noise levels than similar FR-4 boards without local decoupling capacitors. Some boards with embedded capacitance exhibited lower power bus noise than the FR-4 boards with decoupling capacitors.

6. Frequency Domain Measurements

Frequency domain measurements of power bus noise voltage were also conducted on the populated test boards. This section describes the frequency domain measurement set-up and presents the measured data. Boards with different materials, dimensions, stack-ups and loading conditions are evaluated.

6.1 Measurement setup

For all populated test boards, the power bus noise voltage between 1 MHz and 5 GHz was measured using a Rohde & Schwarz FSEB30 spectrum analyzer. A Rohde & Schwarz FSE-Z3 DC block was added to the RF input port of the spectrum analyzer to prevent direct DC input. A 1-meter long SMA precision coaxial cable was used to connect the input port to the SMA jack on the populated test boards. Two ferrite chokes were placed around this SMA coaxial cable to reduce the common mode current flowing on the exterior of the cable shield. As described in the previous section, the one-copy populated test boards were powered by an HPE3630A triple-output DC power supply, and the fully populated test boards were powered by an HP6575A DC power supply. All boards were tested at 3.3 volts. The test setup for the one-copy populated samples is shown in Figure 6.1.

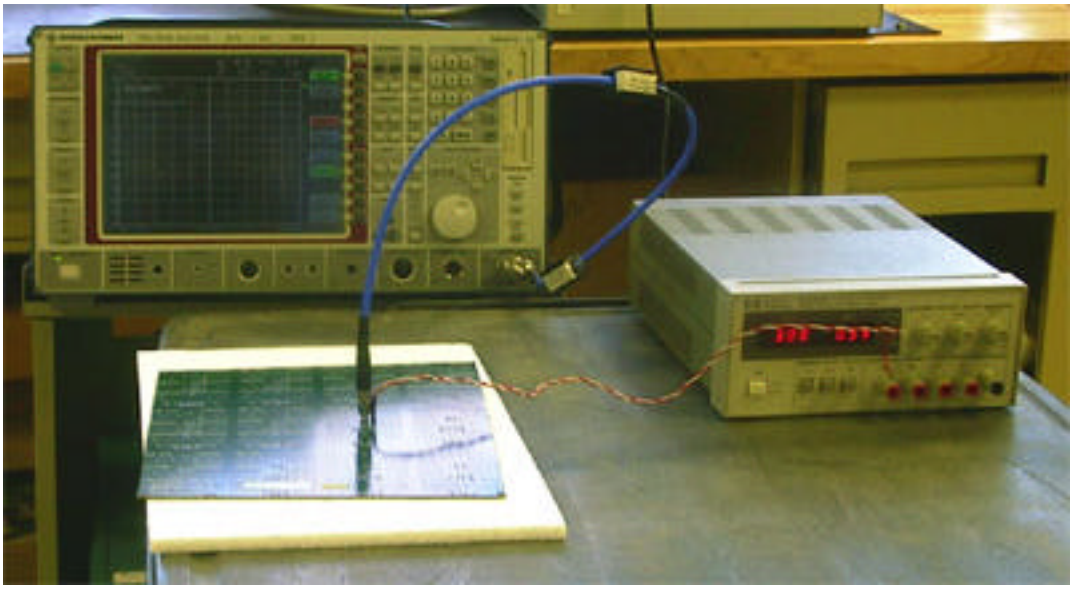

Figure 6.1 Experimental Setup of Frequency Domain Power Bus Noise Measurement

In order to achieve a low noise floor and to keep the sweep time reasonable, the measurement was broken into three frequency ranges: from 1 MHz to 1 GHz, from 1GHz to 3GHz, and from

3 GHz to 5 GHz. The analyzer settings for the resolution bandwidth (RBW), video bandwidth (VBW) and the internal attenuation of the spectrum analyzer for each frequency range are indicated in Table 6.1. The corresponding sweep time and the noise floor level are also listed in the table.

Table 6.1 Spectrum Analyzer Settings for Each Frequency Range

Frequency Range	RBW (Hz)	VBW (Hz)	Internal Attenuation (dBm)	Sweep Time (Second)	Noise Floor (dBm)
1 MHz – 1 GHz	20 K	2 K	-20	64	-87.5
1 GHz – 3 GHz	30 K	3 K	0	56	-107.5
3 GHz – 5 GHz	30 K	3 K	0	56	-107.5

6.2 Presentation of frequency domain power bus noise data

The measured data for two Litton TV1-1-4 FR-4 boards is plotted in Figure 6.2, Figure 6.3, and Figure 6.4 for each of the three frequency ranges. Both boards were one-copy populated. One of the boards had local decoupling capacitors and one did not. The spikes in these plots represented power received at the 50-ohm input of the spectrum analyzer at a specific harmonic frequency. The red curve (no decoupling caps) is shifted by +10 MHz in order to make a comparison of the levels easier. As indicated in Figure 6.2, adding decoupling capacitors significantly reduces the power bus noise in the first few harmonics. However, their effectiveness above a few hundred megahertz is questionable.

It is inconvenient to evaluate the performance of different test boards by comparing the amplitudes of all 20-40 harmonics in each plot. So, in order to develop a criterion for comparison, the amplitude of the power at all harmonics in a specific frequency range was summed. For example, the total power in the twenty harmonics between 1 MHz and 1 GHz was calculated as,

$$P_{total}(dBm) = 10\log_{10}\left(\sum_{n=1}^{20} 10^{P_n/10}\right) \tag{19}$$

where P_n is the power in the nth harmonic in dBm. The total power, P_{total}, was then used to evaluate the performance of test boards with different materials, stack-ups, dimensions and loading conditions.

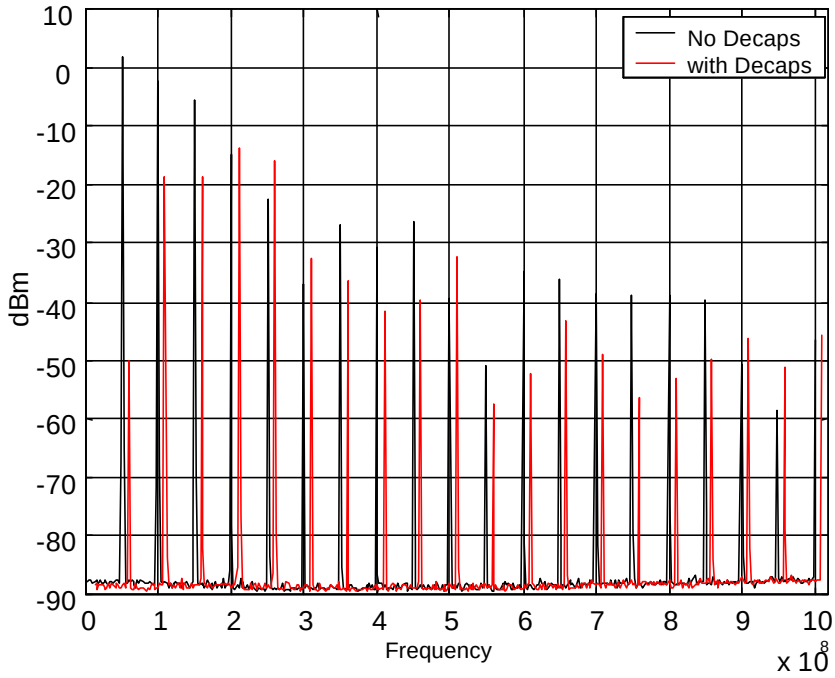

Figure 6.2 Power Bus Noise on One-Copy Populated Litton TV1-1-4 FR-4 boards with/without Decoupling Capacitors: 1 MHz - 1 GHz

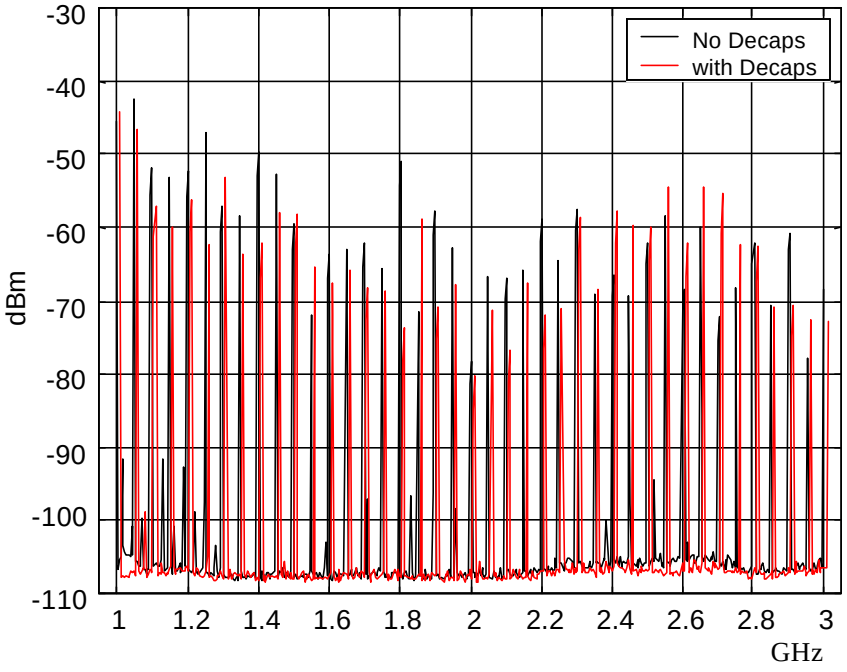

Figure 6.3 Power Bus Noise on One-Copy Populated Litton TV1-1-4 FR-4 boards with/without Decoupling Capacitors: 1 GHz - 3 GHz

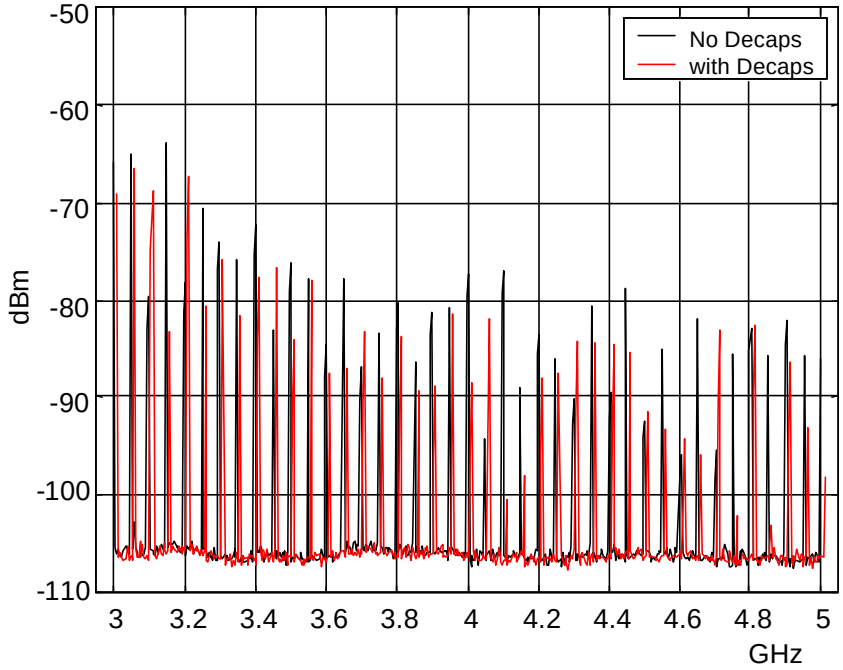

Figure 6.4 Power Bus Noise on One-Copy Populated Litton TV1-1-4 FR-4 boards with/without Decoupling Capacitors: 3 GHz – 5 GHz

6.3 Measurements of one-copy populated test boards

The power bus noise measurement results for TV1-1-1 test samples are summarized in Figures 6.5, 6.6 and 6.7 for each of the three measurement frequency ranges. In these figures, bars of different color represent different materials. Each bar is labeled to indicate the board fabricator, the type of board and the material between the power and ground planes. “fr4” in the label indicates the board was made with FR-4 material. “fr4d” indicates FR-4 material was used and local decoupling capacitors were mounted. The height of each bar indicates the total power in all harmonics within the measurement frequency range.

In the 1 MHz – 1 GHz range, adding decoupling capacitors to an FR-4 board reduces the power bus noise by about 20 dB. However, in the medium and high frequency ranges, the difference between FR-4 boards with and without decoupling capacitors is negligible. In all three ranges, test boards employing embedded capacitance materials exhibited less power bus noise than similar FR-4 boards without decoupling capacitors. Different materials performed differently and some were more efficient than others. In particular, boards made with the C-Ply material (which was much thinner than the other materials), consistently exhibited less power bus noise than similar boards made with the other materials.

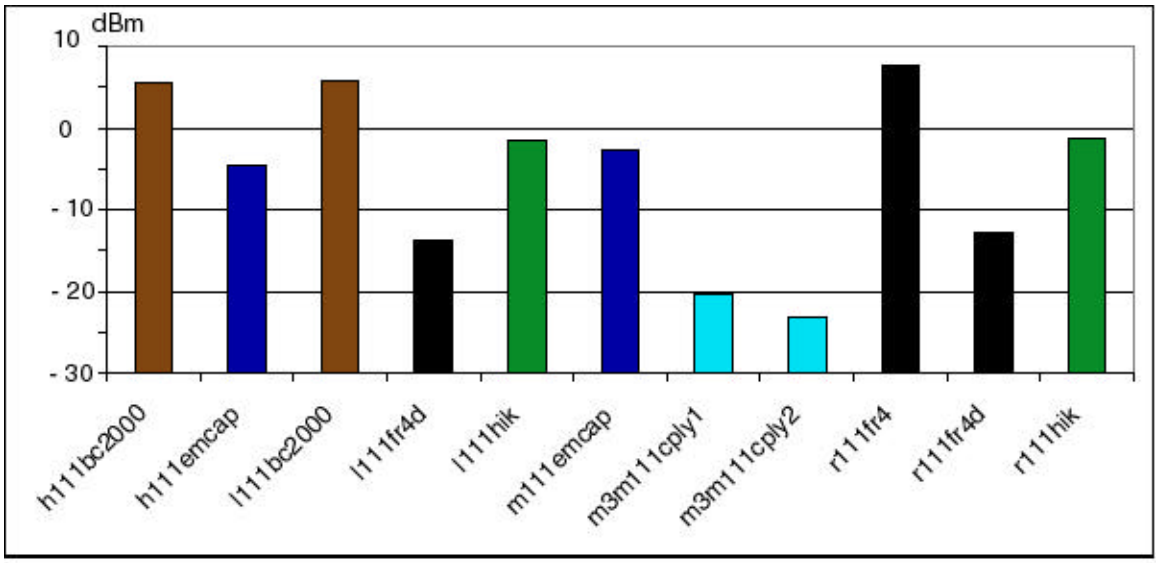

Figure 6.5 Summary of Power Bus Noise Measurement Results for TV1-1-1 Boards (1 MHz – 1 GHz)

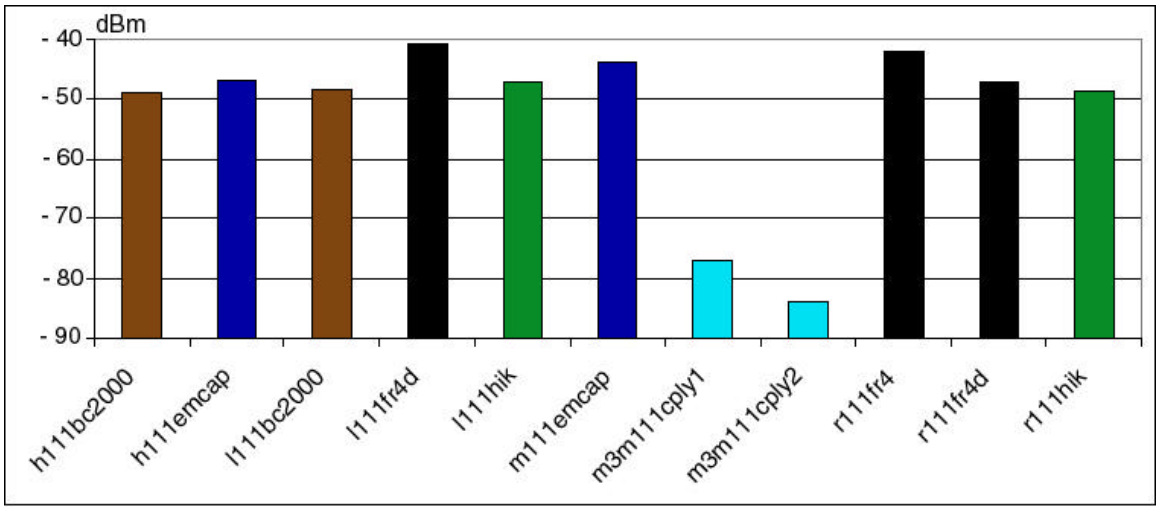

Figure 6.6 Summary of Power Bus Noise Measurement Results for TV1-1-1 Boards (1 GHz – 3 GHz)

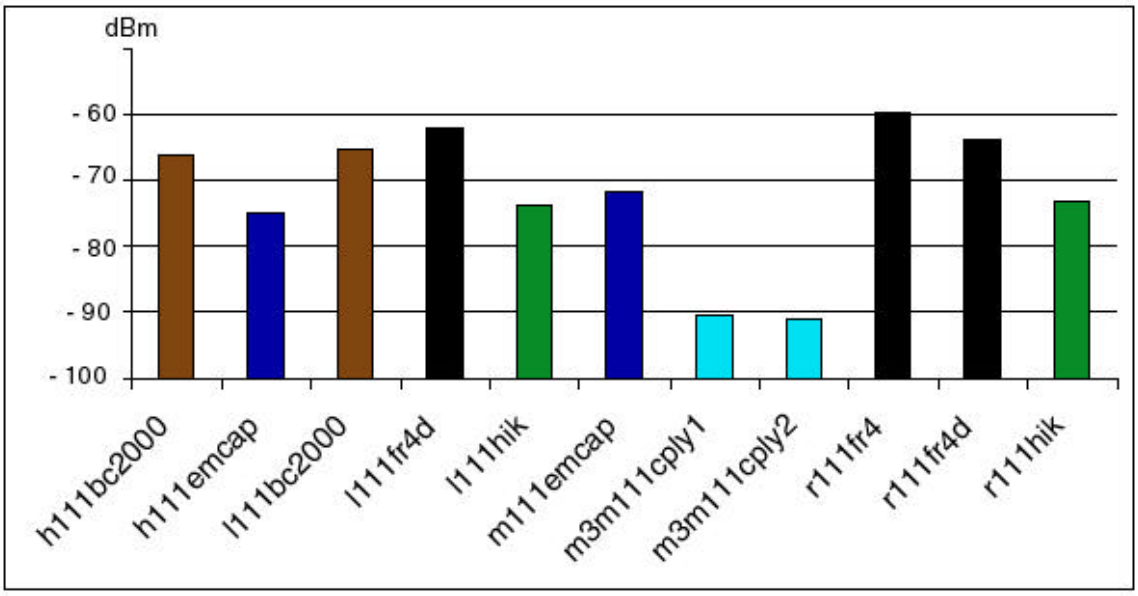

Figure 6.7 Summary of Power Bus Noise Measurement Results for TV1-1-1 Boards (3 GHz – 5 GHz)

6.4 Comparing boards with different stack-ups

According to the measurement results presented in Section 4 and Section 5, TV1-1-Y and TV1-3-Y samples with the same materials and same dimensions had similar power bus impedance and similar levels of time-domain power bus noise. This same conclusion can be drawn from the power bus noise measurements in the frequency domain. Table 6.2 shows the measured power bus noise for three pair of Litton Hi-K boards with different dimensions. All samples were one-copy populated. There is no significant difference between test boards with different stack-ups.

Table 6.2 Power Bus Noise for One-Copy Populated Hi-K Boards with Different Stack-ups

Test Samples	1 MHz – 1 GHz (dBm)	1 GHz - 3GHz (dBm)	3 GHz – 5 GHz (dBm)
Litton TV1-3-12 Hi-K	-24.4	-65.1	-80.6
Litton TV1-1-12 Hi-K	-24.7	-57.7	-75.2
Litton TV1-3-4 Hi-K	-13.8	-60.9	-79.9
Litton TV1-1-4 Hi-K	-14.6	-55.3	-77.6
Litton TV1-3-1 Hi-K	-1.2	-53.0	-73.6
Litton TV1-1-1 Hi-K	-1.4	-47.1	-73.8

6.5 Comparing boards with different dimensions and loading

As discussed in Section 4, for one-copy populated test samples, increasing the board area results in higher inter-plane capacitance, which helps to reduce the power bus noise at low frequencies. When the board is no longer electrically small (i.e. small relative to a half-wavelength), increasing the board dimensions shifts the resonant frequencies, but does not necessarily reduce the board impedance or the power bus noise.

Figure 6.8 shows the power bus noise of two sample groups: Raytheon TV1-1-Y Hi-K boards (left) and Litton TV1-1-Y BC2000 boards. All boards were one-copy populated. Test boards of different dimensions are represented by different fill patterns in each subplot. In the 1 MHz – 1 GHz frequency range, the power bus noise decreases linearly with increasing board area. In the higher frequency ranges, the effect of the board area is less significant; although the larger boards tended to have somewhat less power bus noise.

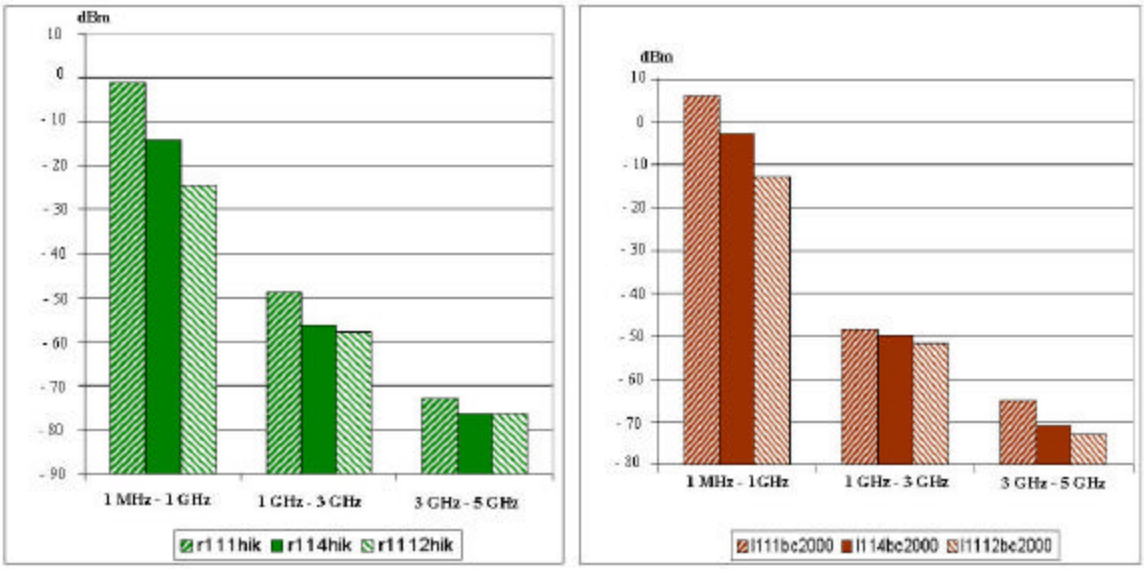

Figure 6.8 Power Bus Noise on One-Copy Populated Samples of Different Dimensions: TV1-1-Y Hi-K Boards (Left) and TV1-1-Y BC2000 Boards (Right)

6.6 Fully populated 4-up and 12-up board results

Table 6.3 summarizes the power bus noise measurements for three fully populated BC2000 boards with a TV1-3-Y stack-up. These test boards were manufactured by Litton. Though the inter-plane capacitance of the fully populated 4-up boards is still four times that of 1-up boards, these boards have four oscillators and four times the total number of components. Consequently, it is reasonable to expect that the larger boards would exhibit higher levels of power bus noise

than the smaller boards. However, the results in Table 6.3 suggest that the larger boards were actually quieter than the smaller boards at low frequencies and exhibited power bus noise levels that were comparable at higher frequencies.

Table 6.3 Power Bus Noise of Fully Populated BC2000 Boards with Different Dimensions

Test Samples	1 MHz – 1 GHz (dBm)	1 GHz - 3 GHz (dBm)	3 GHz – 5 GHz (dBm)
TV 1-3-1	6.0	-55.2	-70.9
TV 1-3-4	0.78	-51.74	-73.92
TV 1-3-12	-3.18	-46.29	-68.99

Table 6.4 summarizes the power bus noise levels on nine fully populated 4-up boards compared to their one-copy populated version in the 1 MHz – 1 GHz range. All five dielectric materials and both stack-ups used in TV1 boards are represented in the table. At first glance, it appears that the differences between the power bus noise in fully populated and one-copy populated samples are random. However, it is worth noting that on the boards with relatively poor decoupling (i.e. the FR-4 boards), fully populated boards are quieter than one-copy populated boards. This is the result that would be expected if the four different circuits on the fully populated board were operating out of phase with each other. Fully populated boards that were well decoupled (e.g. the C-Ply boards) exhibited a power bus noise level that was approximately 6 dB higher than one-copy populated boards. This is the result that would be expected if the four circuits on the fully populated boards were operating independently of each other.

Table 6.4 Power Bus Noise of One-Copy Populated and Fully Populated 4-up Boards in 1 MHz – 1 GHz Range

Samples	One-Copy Populated	Fully Populated	*P2-P1*
	Noise Power P1 (dBm)	Noise Power P2 (dBm)	*(dBm)*
TV 1-1-4 FR-4 no Decaps	3.7	-2.14	-5.88
TV 1-1-4 FR-4 with Decaps	-10.1	-15.16	-5.09
TV 1-1-4 BC2000	-2.5	0.35	2.80
TV1-3-4 BC2000	-2.3	0.78	3.09
TV 1-1-4 EMCAP	-9.0	-2.28	6.67
TV 1-3-4 EMCAP	-9.0	-0.99	7.98
TV 1-1-4 Hi-K	-14.2	-12.02	2.20
TV 1-3-4 Hi-K	-13.4	-9.53	3.86
TV 1-3-4 C-Ply	-26.5	-21.03	5.43

To further investigate this issue, the 12th harmonics of the power bus noise spectrum for the one-copy populated and fully populated TV1-3-12 BC2000 boards are expanded and plotted in Figure 6.9. The 10-dB bandwidth of the one-copy populated board is about 250 Hz, and the 10-dB bandwidth of the fully populated board is about 6 kHz. This results suggests that the various circuits on the 12-up board were not operating at exactly the same frequency.

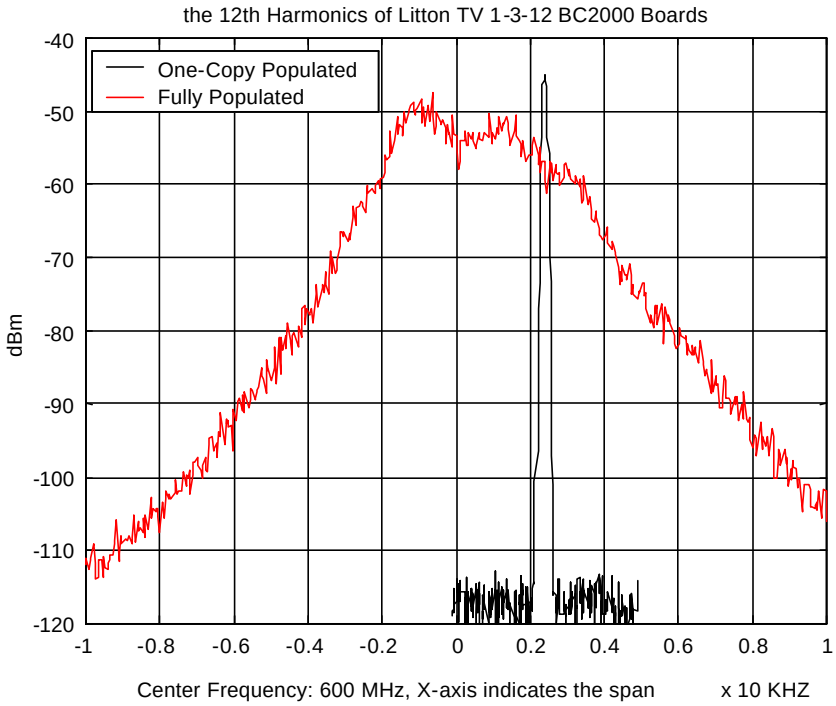

Figure 6.9 12th Harmonic Power Bus Noise for TV1-3-12 BC2000 Boards: One-Copy Populated vs. Fully Populated

This indicates a problem with the 12-up board measurements. The spectrum analyzer adds all spectral levels within the RBW and displays the sum as the level at the center frequency of the filter corresponding to the specific sweep point. Therefore, the RBW in the original measurements (20 kHz for the 1 MHz – 1 GHz range, 30 kHz for the other two frequency ranges) was not wide enough to capture all the harmonic components of the fully populated boards. To verify this, the measurements were repeated for two TV1-1-12 EMCAP boards with three different RBW settings in the 1 MHz – 1 GHz range. One test board is fully populated, while the other is one-copy populated. The measurement results are summarized in Table 6.5. With increased RBW settings, the calculated noise power of the fully populated board was about 10 dB higher than the one-copy populated version. In other words, the fully populated version generated as much as ten times more power bus noise than the one-copy populated version.

Table 6.5 Power Bus Noise of TV1-1-12 EMCAP Boards in 1 MHz – 1 GHz Range with Different RBW Settings

RBW	One-Copy Populated Noise Power P1 (dBm)	Fully Populated Noise Power P2 (dBm)	*P2-P1 (dBm)*
20 KHz	-12.24	-10.06	2.18
2 MHz	-12.15	-2.22	9.93
20 MHz	-12.1	-1.24	10.86

The same procedure was also performed on fully populated and one-copy populated TV1-1-4 FR-4 boards without local decoupling capacitors. The measurement results are listed in Table 6.6. Without decoupling capacitors, even when the RBW of the measurement is wide enough to capture all the harmonics, the fully populated board is still 2 dB quieter than the one-copy version. Additional research is required to explain this, however it appears that on boards with a lot of power bus noise, the circuit clocks tend to operate out of phase with one another.

Table 6.6 Power Bus Noise of TV1-1-4 FR-4 Boards in 1 MHz – 1 GHz Range with Different RBW Settings

RBW	One-Copy Populated Noise Power P1 (dBm)	Fully Populated Noise Power P2 (dBm)	*P2-P1 (dBm)*
20 kHz	-10.08	-15.16	-5.08
2 MHz	-9.82	-12.76	-2.94
20 MHz	-9.81	-12.69	-2.88

7. Conclusions

It is clear from the results presented in this report that embedded capacitance can be a very effective tool for reducing power bus noise. At frequencies above 1 GHz, discrete decoupling capacitors lose their effectiveness due to the inductance associated with their connection to the power bus. Embedded capacitance on the other hand is effective at frequencies well above 1 GHz.

Four types of embedded capacitance were evaluated in this study. All of them provided additional capacitance that (like discrete decoupling capacitors) was capable of supplying low-frequency current to active devices on the board. At low frequencies, the current supplied by embedded capacitance is at least as high as the current supplied by discrete capacitors with the same total capacitance value. At higher frequencies the current supplied by embedded capacitance is greater

because the inductance of the connections to the discrete capacitors limits the amount of charge they can supply is a very short time.

At very high frequencies (typically above a few hundred megahertz), the inductance of the connections to the local decoupling capacitors makes them relatively ineffective. Current is initially drawn from the planes. The frequency at which the discrete capacitors become ineffective depends on the relative inductance of their connections as compared to the impedance of the planes. For most practical board geometries, with planes spaced 10 mils apart or less, discrete capacitors are ineffective at frequencies greater than about 1 GHz.

At frequencies where the board is not electrically small, board resonances (if not sufficiently damped) are the most significant problem. Boards without sufficient loss in the power bus will tend to "ring" at the frequencies at which the power planes resonate. If a source harmonic happens to occur at a board resonance, the power bus noise voltage may be excessive.

Loss is required to dampen board resonances. There are four primary sources of loss in printed circuit board power planes: dielectric loss, copper loss, component loss and radiation loss. Of these four, copper loss dominates if the plane spacing is sufficiently small. The Q-factor is a quantity equal to the ratio of the stored energy in the planes to the power lost per cycle at a given frequency. A Q-factor of 1 implies that the resonance is completely damped. The Q-factor associated with the TM_{10} mode for a power bus structure dominated by copper losses can be approximated as,

$$Q_c \approx h\sqrt{pfms} \ . \tag{11}$$

The power bus noise voltage can be calculated using the equation,

$$V_{noise} = I_{devices} \times Z_{powerbus} \ . \tag{18}$$

The current drawn by the active devices can be calculated or approximated based on the data supplied in component data sheets and a knowledge of how the device is used (signal waveforms, load impedances, etc.) [14][15]. The power bus impedance, $Z_{powerbus}$, may be an input impedance or a transfer impedance. It can be estimated using numerical models, circuit models or cavity modeling techniques.

Cavity modeling is particularly interesting because it provides a level of insight into power bus behavior that is not apparent from other modeling results. The cavity model was used to develop

most of the conclusions about plane resonances presented in this report. Some of these conclusions are repeated below:

- Closely spaced planes will damp resonances due to copper losses
  (i.e. plane spacing is very important)

- Dielectric loss is the most significant loss only when the planes are further apart (approximately >10 mils for FR-4)
  (i.e. dielectric loss is not very important for closely spaced planes)

- When the planes are sufficiently damped, the size of the planes is not so important, since waves reflecting from the edges do not generally get back to the source.
  (i.e. board size is not very important at high frequencies, although it affects the total capacitance available at low frequencies.)

- The dielectric constant (relative permittivity) affects the frequencies at which resonances occur and indirectly the Q-factor associated with a given resonance.
  (i.e. At low frequencies, the capacitance available is directly proportional to the dielectric constant. At high frequencies, high dielectric constants help to reduce the Q-factor associated with a given resonance, but are not as important as plane spacing.)

In general, all of the materials evaluated did a fair job of dampening power bus resonances. However, the C-Ply material, with its ~5 micron plane spacing, was the only material to essentially eliminate these resonances. The modeling suggests that the reason this material performed so well was due to the very small plane spacing. The dielectric constant and the loss tangent of this material had relatively little to due with its ability to suppress power bus noise.

8. Design Guidelines

The design guidelines presented in this section are based on the measurements and models presented in this report. As with any attempt to take a complicated subject and condense it into simple guidelines, many assumptions and approximations are made. In situations where an accurate assessment of the decoupling is required, it is a good idea to enlist the aid of an EMC or signal integrity engineer who is familiar with your particular application.

8.1 Determining the board impedance requirement

The first step in the design of a printed circuit board decoupling scheme is to determine the maximum board impedance requirement. In order to provide adequate amounts of current without an excessive change in voltage, the board's impedance must be held below some maximum level. The procedure for determining the maximum board impedance involves estimating the maximum current required by active devices on the board and dividing that value into the maximum noise

voltage that can be tolerated. This procedure is described in [14] and other signal integrity publications.

8.2 Establishing the total amount of capacitance required

At the frequencies at which local discrete decoupling capacitors are usually effective, the board impedance is calculated as,

$$Z_{powerbus} = 1/jwC \tag{20}$$

where C is the total decoupling capacitance available. More capacitance results in a lower power bus impedance. If embedded capacitance is going to be used to replace existing discrete decoupling capacitors in a printed circuit board design, the total amount of embedded capacitance should be greater than or equal to the amount of capacitance it is replacing. Normally, bulk decoupling capacitors (e.g. capacitors with a value of 1 microfarad or greater) are left in place. Embedded capacitance normally replaces the local decoupling capacitors (e.g. capacitors with a value of 0.01 microfarads or smaller).

8.3 Ensuring that resonances are damped

As discussed previously in this report, when the maximum dimensions of a printed circuit board with solid power and ground planes exceed a half-wavelength, the power bus may exhibit resonances. If a source harmonic excites a power bus resonance, the noise voltage can become excessive. For this reason it is important to be sure that power bus resonances are sufficiently damped.

If the planes are closely spaced (e.g. less than 10 mils), then the dominant loss mechanism will be the copper losses in the planes. For the TM10 mode, the Q-factor associated with this loss is approximately,

$$Q_c \approx h\sqrt{pfms} \ . \tag{11}$$

The resonance is completely damped when the Q-factor is equal to 1. By setting $Q_c=1$ and using the fact that the longest dimension of a rectangular board is one-half wavelength for the TM10 mode, we can derive an expression for the maximum spacing, h, that guarantees the TM10 resonance will be completely damped.

$$h = \sqrt{\frac{2l\sqrt{e_r}}{p\,s\,h_o}} \tag{21}$$

where: l is the length of the maximum board dimension

e_r *is the relative permittivity of the dielectric*

s *is the conductivity of the copper*

h_o *is the intrinsic impedance of free space*

For a board with a relative permittivity of 4, the spacing in microns can be expressed as,

$$h = 0.8\sqrt{l} \tag{22}$$

where: l is the length of the maximum board dimension in centimeters.

Measurements on the TV1 boards suggest that if the TM_{10} mode is damped, then higher order modes will also be damped. The plane spacing rule in Equation (22) is conservative. Based on the measurements made during the course of this study, plane spacings that were two or three times this thickness adequately damped power bus resonances.

8.4 Estimating the board impedance

An estimate of the power bus noise voltage requires an estimate of the board impedance. As discussed in Section 2 of this report, calculating the input impedance of a power bus at high frequencies requires complex numerical modeling. However, a rough approximation for the power bus impedance at resonance peaks is offered below:

$$Z_{powerbus} \approx Z_{damped}\sqrt{Q} \tag{23}$$

Here, Z_{damped} is defined as the input impedance or transfer impedance that would exist if the resonance were critically damped (i.e. Q=1). An estimate of Z_{damped} can be made by modeling the power planes as an infinite radial transmission line (since the resonances are damped, the edges are not a factor). Simple closed-form expressions for Z_{damped} are being developed by the authors.

9. Future Work

The boards built and tested for this project provide a unique opportunity to study the effects of embedded capacitance, board stack-up, component loading and other factors on power bus noise and radiated EMI. During the short time available after the boards became available and before the formal end of the project, a large number of measurements were made that allowed us to draw

the conclusions reported here. However, there are many more tests that can be done and many more questions to be answered. The following tests should provide useful information:

- Evaluate boards that were not completed in time for this report (e.g. TV1-1-1 FR-4 boards and other combinations that were missed in the initial build),
- Evaluate fully populated boards with synchronized clocks to determine the effect of loading boards with many circuits using the same clock signal,
- Explore the effects of component loading with non-active devices and devices not clocked,
- Quantify the Q-factor due to component loading,
- Continue to develop and validate a closed-form expression for approximating the power bus impedance and power bus noise for embedded capacitance boards.

Initial testing conducted at UMR and at StorageTek did not reveal a strong link between power bus noise and radiated EMI on the TV1 boards. Nevertheless, power bus noise is known to be a significant source of radiated EMI in some products. These boards provide us with an opportunity to investigate factors that couple power bus noise to radiated EMI sources, such as:

- The effect of embedded capacitance on radiated EMI from boards mounted in a resonant enclosure,
- The effect of board stack-up on radiated EMI (i.e. determine whether there is any advantage to embedding signal traces between planes),
- The ability of heatsinks to couple power bus noise to enclosures or cables.

Because these materials are so new, there are bound to be many applications that have not yet been conceived. The ability to put significant amounts of capacitance between the planes provides many opportunities to create filters and passive circuits that have very low connection inductance and require relatively little board area. It is also possible to build distributed elements with good high frequency characteristics between the planes. There are many possible directions that this work could lead us. The directions that any future work will take will be primarily determined by the participating companies and individuals.

References

[1] T. H. Hubing, T. P. Van Doren, F. Sha, J. L. Drewniak, and M. Wilhelm, "An experimental investigation of 4-layer printed circuit board decoupling," *Proceedings of the 1995 IEEE International Symposium on Electromagnetic Compatibility*, Atlanta, GA, August 1995, pp. 308- 312.

[2] J. Fan, J. Knighten, A. Orlandi, N. Smith and J. Drewniak, "Quantifying decoupling capacitor location," *Proceedings of the 2000 IEEE International Symposium on Electromagnetic Compatibility*, Washington D.C., August 2000.

[3] Todd H. Hubing, James L. Drewniak, Thomas P. Van Doren, David M. Hockanson, "Power bus decoupling on multiplayer printed circuit boards," *IEEE Transactions on Electromagnetic Compatibility*, vol. 37, no. 2, May 1995, pp. 155-166.

[4] L. Smith, R. Anderson, D. Forehand, T. Pelc and T. Roy, "Power distribution system design methodology and capacitor selection for modern CMOS technology," *IEEE Transactions on Adv. Packaging*, August 1999, pp. 284-291.

[5] B. Rubin and W. Becker, "The modeling of delta-I noise in high performance computer modules," in *Conf. Rec. 17th Asilomar Conf. Circ., Syst., and Comput.*, IEEE Cat. #83CH1939-8, Oct. 31/Nov. 2, 1983.

[6] I. Novak, "Reducing simultaneous switching noise and EMI on ground/power planes by dissipative edge termination," *IEEE Trans. on CPMT*, vol. 22, no. 3, August 1999, pp. 274-283.

[8] G. T. Lei, Robert W. Techentin and Barry K. Gilbert, "High-frequency characterization of power/ground-plane structures", *IEEE Trans. Microwave Theory and Techniques*, vol. 47, No. 5, May 1999, pp. 562-569.

[9] G. T. Lei, Robert W. Techentin, Paul R. Hayes, Daniel J. Schwab and Barry K. Gilbert, "Wave model solution to the ground/power plane noise problem", *IEEE Trans. Instrumentation and Measurement*, vol. 44, no. 2, Apr. 1995, pp. 300-303.

[10] Keith R. Carver and James W. Mink, "Microstrip antenna technology," *IEEE Trans. Antennas and Propagation*, vol. AP-29, no.1, Jan. 1981, pp. 2-24.

[11] Kai F. Lee and Wei Chen, *Advances in Microstrip and Printed Antennas*, New York, John Wiley & Sons, 1997, Ch5.

[12] David M. Pozar, *Microwave Engineering*, New York, John Wiley & Sons, 1997, Ch6.

[13] Constantine A. Balanis, *Antenna Theory: Analysis and Design*, New York, John Wiley & Sons, 1997, Chapter 14.

[14] H. Johnson and M. Graham, *High-Speed Digital Design: A Handbook of Black Magic*, Prentice Hall, 1993, Chapter 8.

[15] T. P. Van Doren, "Power bus noise estimation algorithm," *UMR Electromagnetic Compatibility Laboratory Report, TR99-3-024*, Mar. 1999.