UMR EMC Laboratory
Dept. of Electrical & Computer Engineering
1870 Miner Circle
University of Missouri – Rolla
Rolla, MO 65409-0040

UMR EMC Laboratory Technical Report: TR01-2-031

Differential Clock Driver Evaluation

C.L. Guo

H. Wang

T. H. Hubing

April 5, 2001

Executive Summary

Differential clock signals tend to be more immune to electromagnetic interference and crosstalk than single-ended clock signals. They are also less likely to produce excessive radiated emissions. Radiation problems with differential circuits are generally due to the conversion of differential signal currents to common-mode currents. Susceptibility problems are often the result of induced common-mode currents that are converted to differential-mode noise. Conversions from differential-mode to common-mode (or from common to differential mode) are generally due to imbalance in the circuit. Imbalance may be introduced by the source, load or transmission path. This report summarizes an investigation of one particular differential clock generator. This device is capable of generating four differential clock signals. Both the amount of current supplied and the clock frequencies of the differential outputs are programmable.

Differential output signal waveforms were measured directly using a digital oscilloscope and the common-mode voltage was obtained as the sum of the output voltages from each differential pair. Averaging the measured signals over many periods solved problems associated with the low single-sweep sampling rate of the oscilloscope.

The common-mode currents were measured on the power supply cable and the differential output cables that were connected to oscilloscope. No difference in the common mode current was observed when the levels or frequencies of the differential signals were varied. Based on this result, it appears that the primary source of common-mode currents on the cable attached to the test board was the power bus noise.

Different SMA terminators were used to introduce different amounts of skew between the differential pairs. Again, the common-mode currents on the power supply cable didn't change significantly. This is consistent with the idea that power bus noise was the primary source of induced common mode currents and not the differential signals.

Although the common-mode voltage produced by the clock driver was not the primary source of induced common-mode currents on the cables, it was still measurable. The peak-to-peak common-mode voltage was about 0.1 volts at all clock frequencies evaluated. By observing the output waveforms, it is apparent that the risetime of the drivers is slightly faster than the falltime. This is the primary source of imbalance resulting in the common-mode voltage. Future investigations will examine the effect of loading on the transition times of this driver.

Acknowledgement

The test board for this study was provided by Intel Corporation.

1 Introduction

Differential clock signals are generally more immune to noise than single-ended clock signals. At the receiving location, the two waveforms making up the differential signal are compared to determine their logic polarity. This comparison requires no local reference voltage. Therefore, differential reception is not affected by ground voltage shifts between the transmitter and receiver [1]. Also, if the differential signals are perfectly balanced, the common mode currents on the interconnected ground paths are zero resulting in lower radiated emissions.

However, any imbalance at the source, or in the circuit path will result in skew between the two signals. Skew refers to a difference in phase and/or wave shape between the two sides of the differential signal pair. Skew creates common mode currents, which can be a significant source of radiated emissions.

In order to understand the effects of differential clock drivers on emissions, we need to quantify the amount of skew for a typical differential clock driver and determine the effect of driver skew on EMI. This report describes the experimental evaluation of a particular clock driver used in high-speed computer circuits.

2 Test Setup

2.1 Clock Driver Description

The clock driver under investigation is a two-way multi-processor motherboard clock generator IC. It generates four differential current-mode clock pairs. The current supplied at the differential outputs is programmable. A resistor determines the reference current, and there are four different output current levels based on this reference. The clock frequency of the output is also programmable.

2.2 Test Board Description

The photo of the test board used for this study is shown in Fig. 1. It has four layers, one solid power plane, one solid ground plane and two outer layers for signals. Four differential clock pairs are connected to eight of the SMA connectors shown in Fig. 1.

2.3 Measurement Setup

Figure 2 illustrates the measurement setup. A DC power supply was connected to the test board through two wires (red and black). One side of a differential output pair was connected to Channel 1 of the oscilloscope (Tektronix TDS 520A); the other side was connected to Channel 2. Both oscilloscope inputs were referenced to ground.

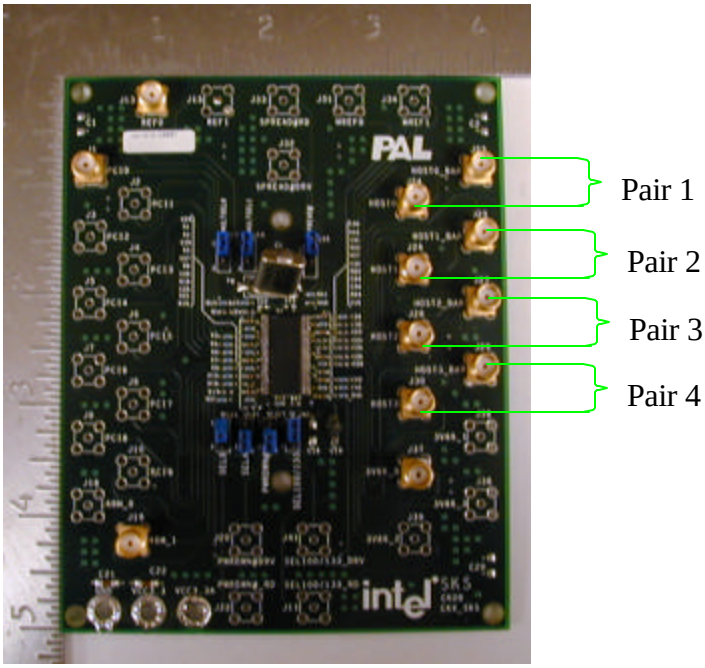


Fig. 1. Test Board.

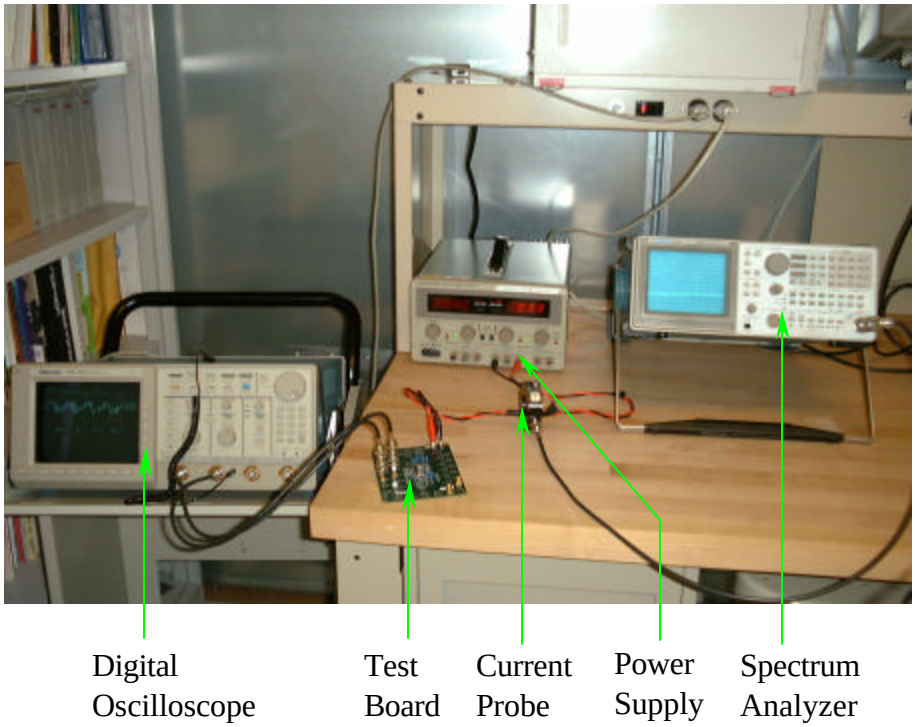


Fig. 2. Experimental setup for measurements.

The power supply, the test board and oscilloscope were put in the shielded chamber. A current probe was used to measure the common-mode current on the power supply cable and connected with the spectrum analyzer (Tektronix 2712) outside the chamber through a cable, as shown in Fig. 3.

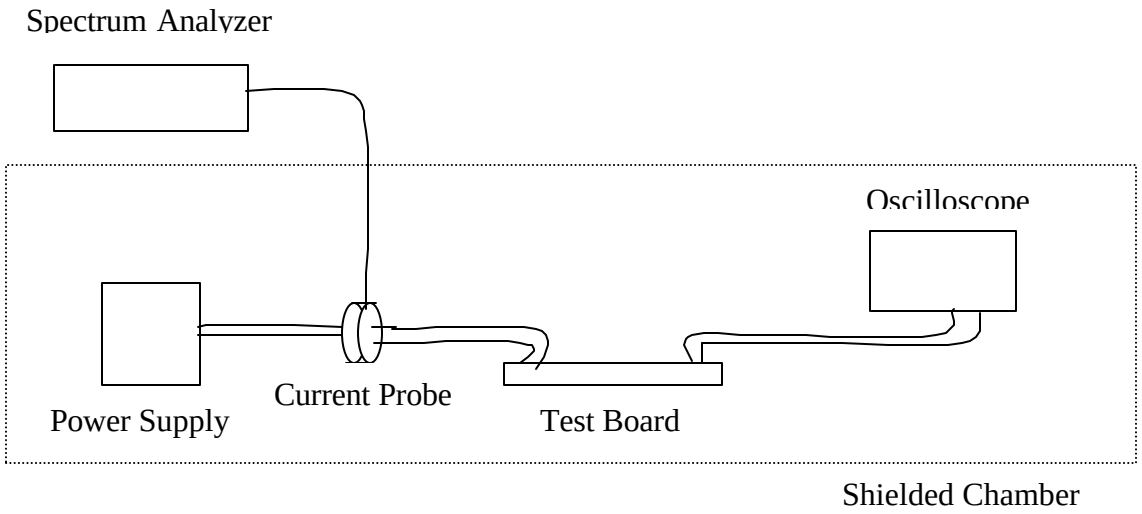


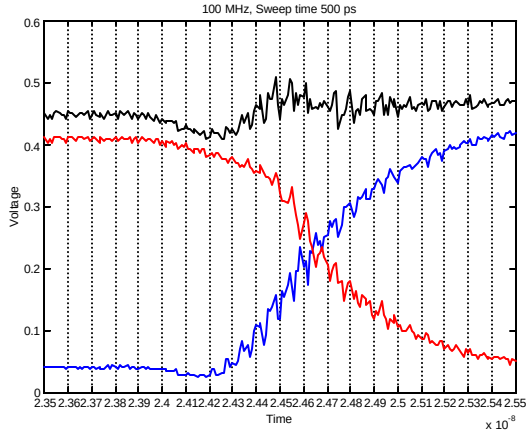
Fig. 3. Experimental setup.

3 Common-Mode Voltage Measurements

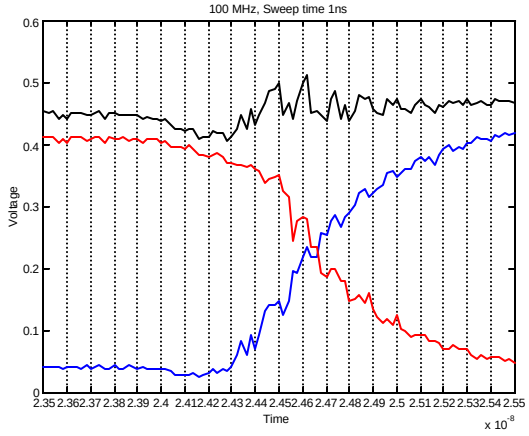
First, the differential outputs were measured directly on the oscilloscope. The results are shown in Fig. 4. The red curve and the blue curve are two sides of the same differential output. The black curve is the sum of these two signals, thus it was the common-mode voltage. The units of the vertical axis are volts. The time difference between two adjacent vertical grid lines is 0.1 ns.

The behavior of common-mode voltage appeared quite different at different clock frequencies and using different sweep times. Noise was observable almost everywhere on each of the three signals. It was soon determined that this noise was not real, but introduced by the sampling mechanism of the digital oscilloscope. On this scope, the displayed waveform is the sum of 5 separate sweeps. Each sweep samples at 1/5 of the overall sampling frequency and successive sweeps are offset by 1/5 of the sample period. Jitter in the waveform appears as noise, since successive data points are not taken from the same sample.

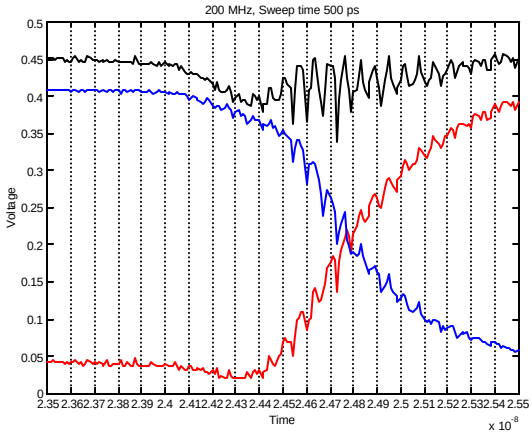
In order to reduce this noise, the differential signals were averaged over about 1,000 cycles, as shown in Fig. 5. The average waveforms were then summed together to get the common-mode voltages. This averaged out the sampling noise. The resulting common-mode voltage was independent of clock frequency. Its peak-to-peak value was about 0.1 Volts. This voltage appears to be due to the fact that the risetime is slightly faster than the falltime of these signals.



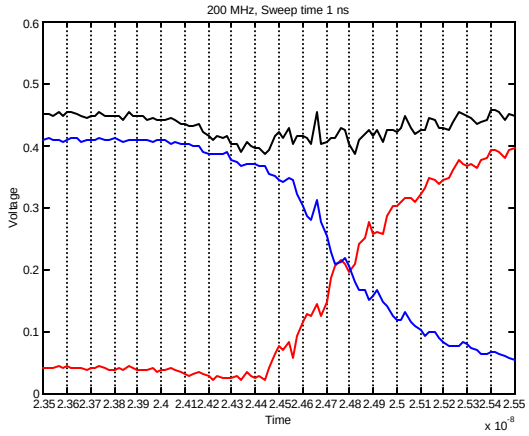
(a) 100 MHz Freq, 500 ps Sweep Time



(b) 100 MHz Freq, 1 ns Sweep Time



(c) 200 MHz Freq, 500 ps Sweep Time

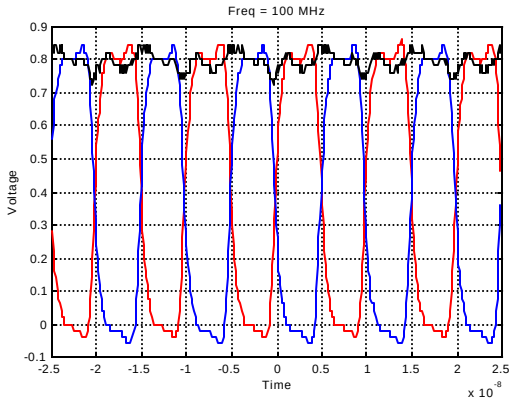


(d) 200 MHz Freq, 1 ns Sweep Time

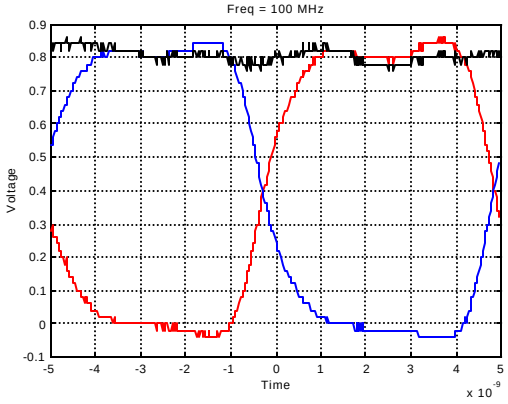
Fig. 4. Direct common-mode voltage measurement results.

4 Common-Mode Current Measurements

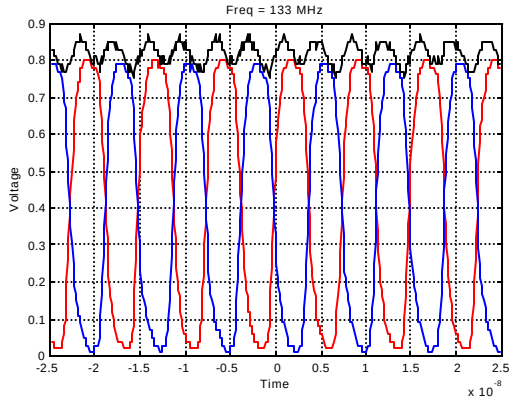
With the clock driver under investigation, it is possible to adjust the output current of the differential clocks. Three differential output current levels were used in this study. One was a high output that was seven times the reference current, another was a low output that was four times the reference current and the third was a zero output. The common-mode current measured on the power supply cable is shown in Fig. 6 for high, low and zero output current when the clock frequency is 100 MHz or 200 MHz. No difference between high and low output current was observed. The common-mode current is actually 2-5 dB higher at many frequencies when there is no output current. [*Note: The current amplitude is expressed in dB. The top of the graph (labeled –50 dB) corresponds to approximately +57 dBmA.*]



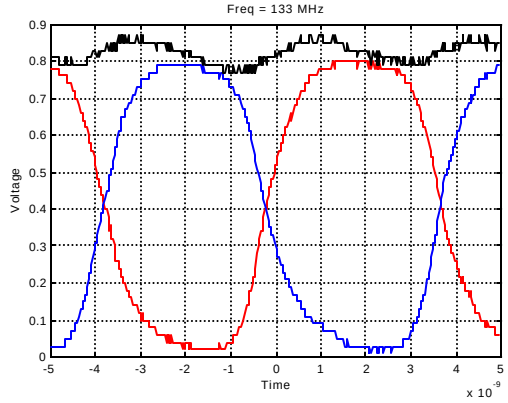
(a) 100 MHz



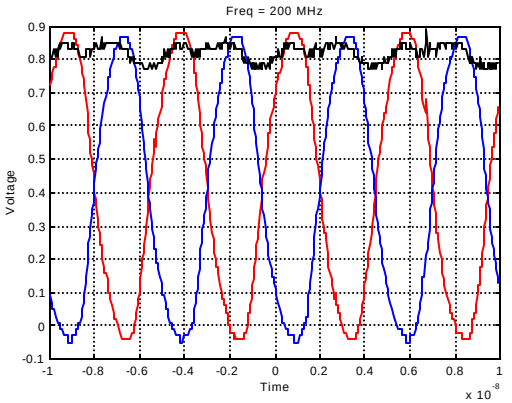
(b) 100 MHz, sweep time increased



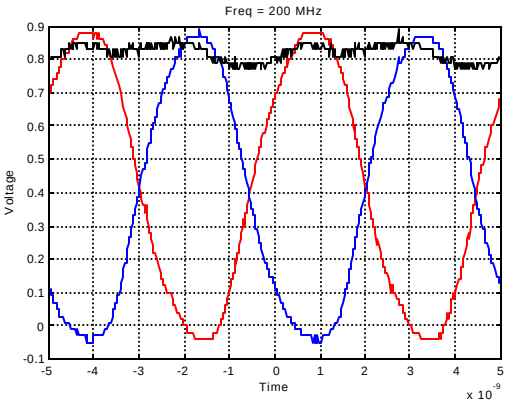
(c) 133 MHz



(d) 133 MHz, sweep time increased

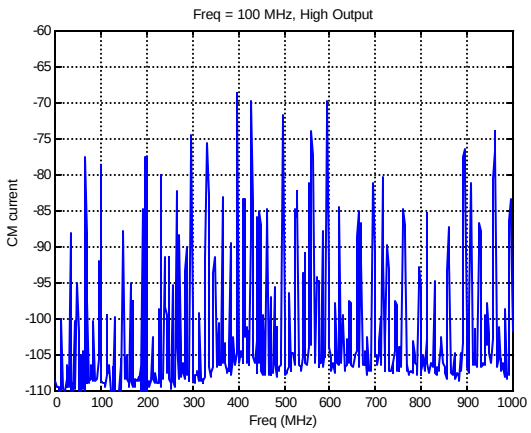


(e) 200 MHz

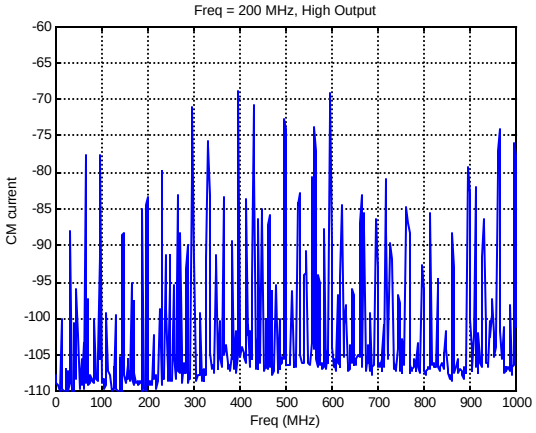


(f) 200 MHz, sweep time increased

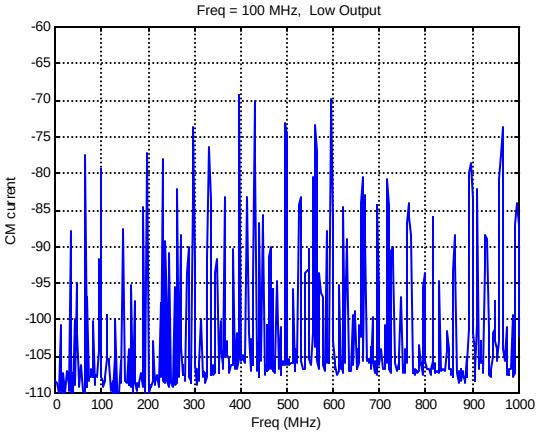
Fig. 5. Common-mode voltage measurement results after averaging.



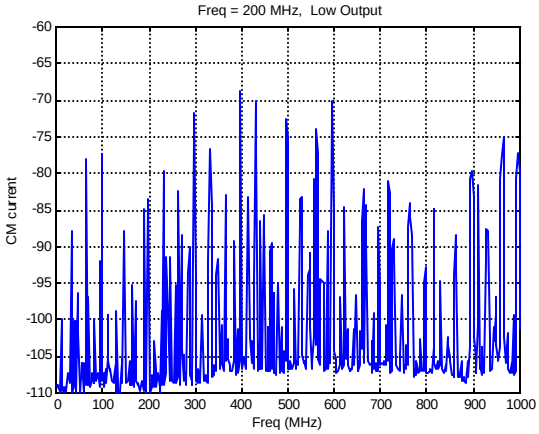
(a) Freq = 100 MHz, High Output



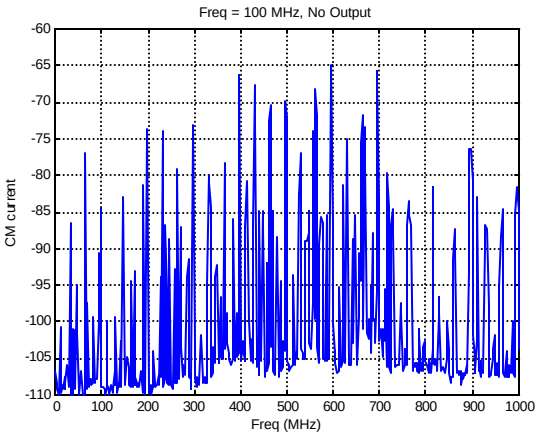
(b) Freq = 200 MHz, High Output



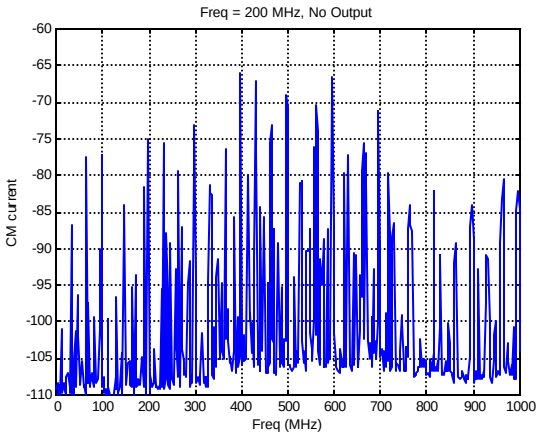
(c) Freq = 100 MHz, Low Output



(d) Freq = 200 MHz, Low Output

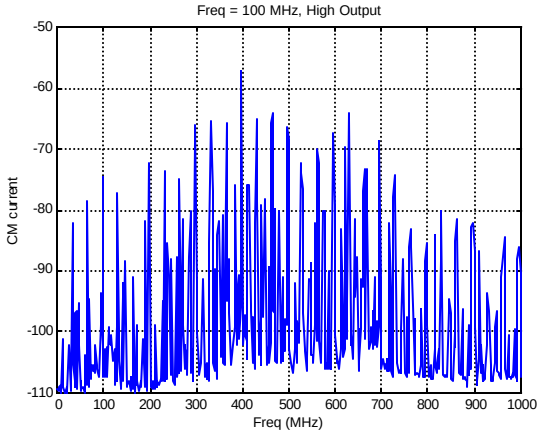


(e) Freq = 100 MHz, Zero Output

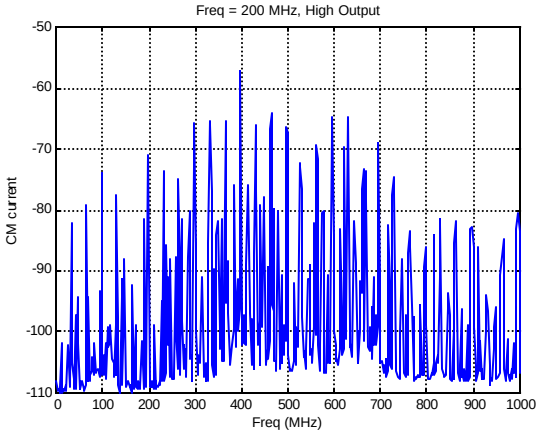


(f) Freq = 200 MHz, Zero Output

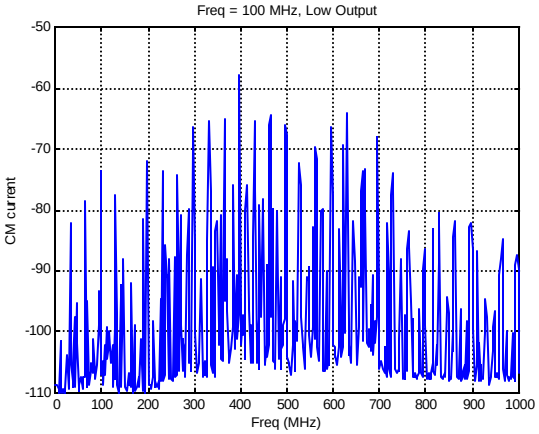
Fig. 6. Common-mode currents measured from power supply cable.



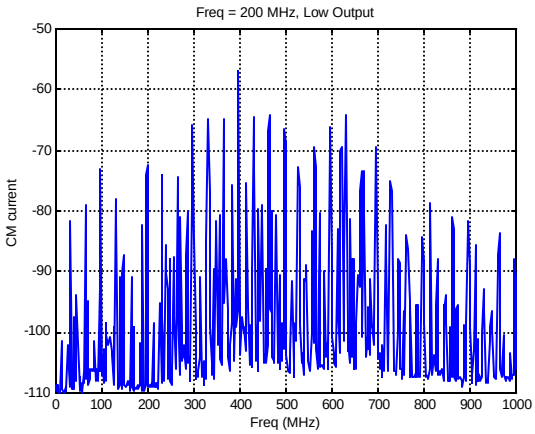
(a) Freq = 100 MHz, High Output



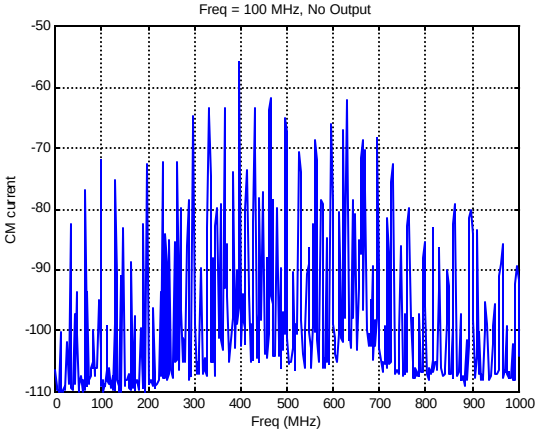
(b) Freq = 200 MHz, High Output



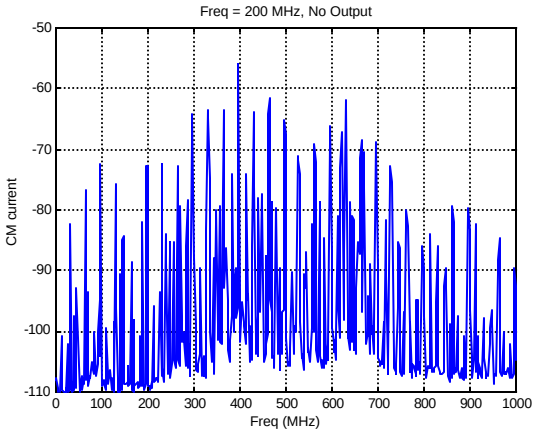
(c) Freq = 100 MHz, Low Output



(d) Freq = 200 MHz, Low Output



(e) Freq = 100 MHz, Zero Output

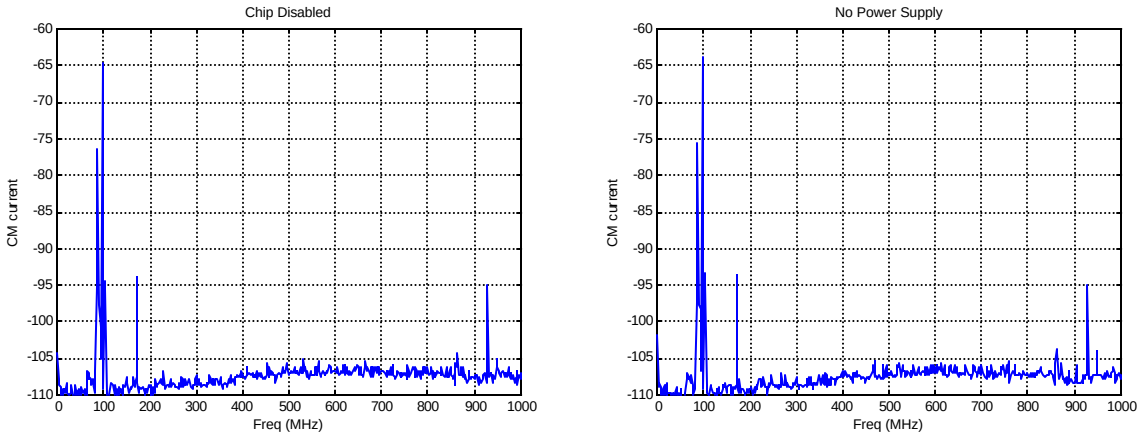


(f) Freq = 200 MHz, Zero Output

Fig. 7. Common-mode currents measured on the oscilloscope cables.

Also, the common-mode currents on the cables that connected the differential outputs to the oscilloscope were measured and are shown in Fig. 7. Although the differential output currents changed greatly, the common-mode currents on this cable did not vary much. They were within 2 dB at almost all frequencies when the clock frequency was set to 100 MHz or 200 MHz. No significant difference between the high, low and zero output currents was observed.

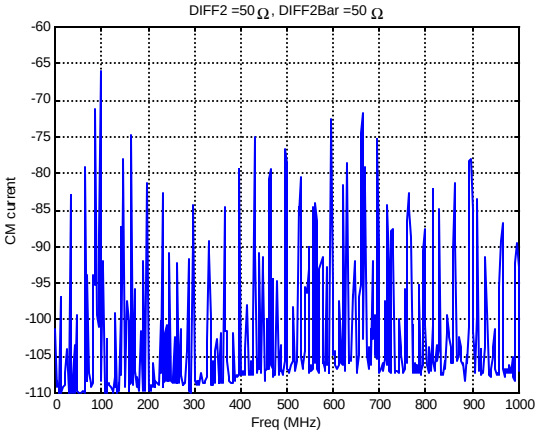
The following measurements were made to determine whether the common-mode currents were related to the differential signals or not. First, the clock driver was disabled. Both the clocks and oscillator were shut down, though the power supply was still powered on. The common-mode current on the power supply cable was measured and is shown in Fig. 8(a). The measured common-mode current with the power supply turned off is shown in Fig. 8(b). These ambient measurements confirmed that most of the noise measured in Figures 6 and 7 was coming from the board being tested.



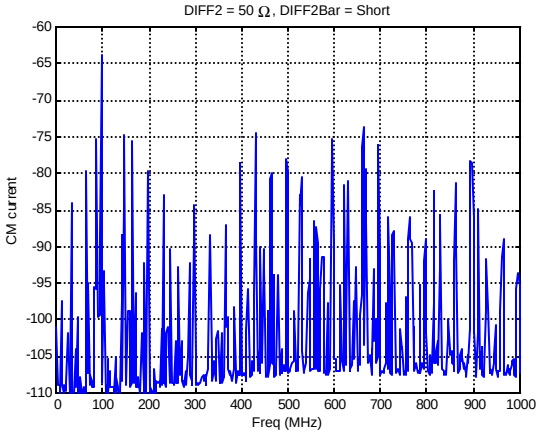
(a) Chip disabled (b) No power supply

Fig. 8. Common-mode currents on the power supply cable.

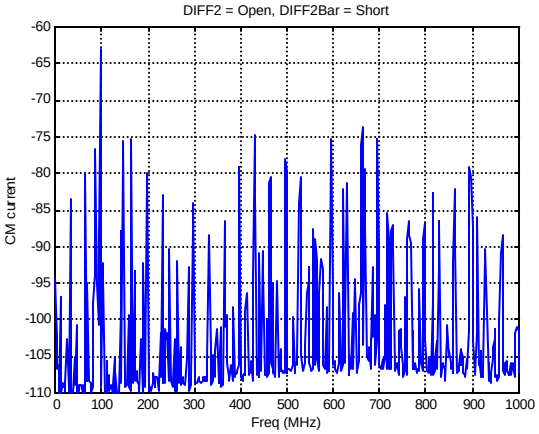
The SMA connectors were then connected to different SMA terminators in an attempt to intentionally introduce different amounts of skew. For example, one measurement was made with both sides of a differential pair connected to 50-ohm loads. They were almost balanced and the current (voltage) on each side of the differential pair was approximately equal. Then a measurement was made with one side open circuited and one side shorted. The currents (voltages) on this pair were quite different and skew was increased. Fig. 9 shows the measured common-mode current on the power supply cable with different combinations of SMA terminators. In the first four figures, only one differential pair on the board was terminated. More pairs were examined in the following two figures. When one differential pair was terminated (DIFF2 and DIFF2bar), the amount of common-mode current was essentially independent of the load imbalance. Even with two or three differential pairs unbalanced, the common-mode current remained almost the same.



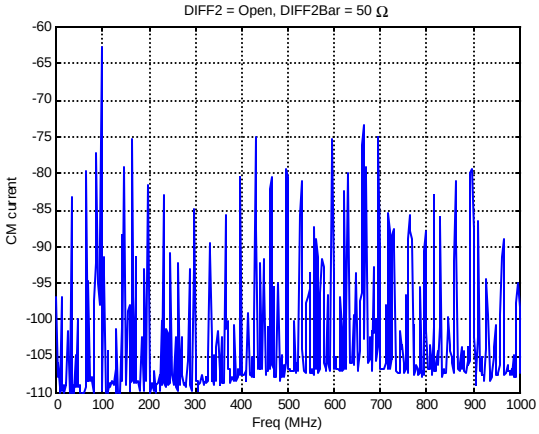
(a) DIFF2 = 50 ohms, DIFF2Bar = 50 ohms



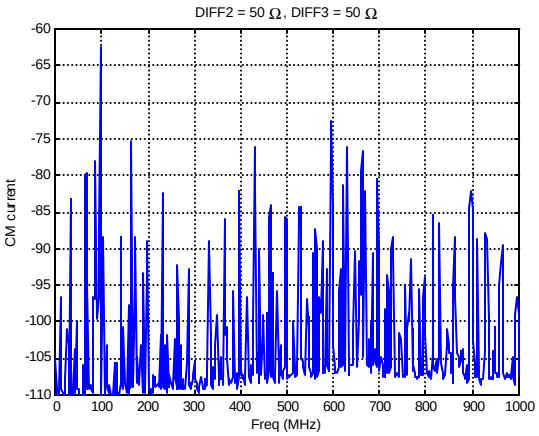
(b) DIFF2 = 50 ohms, DIFF2Bar = Short



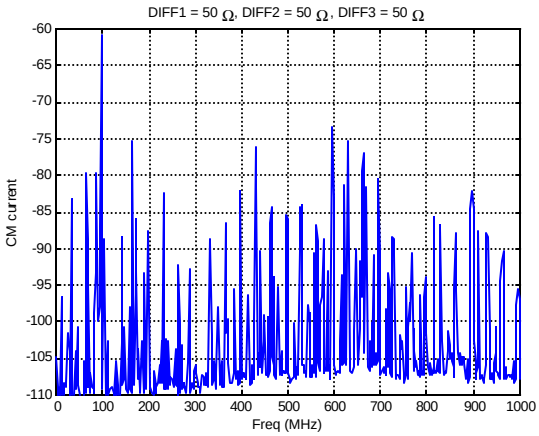
(c) DIFF2 = Open, DIFF2Bar = Short



(d) DIFF2 = Open, DIFF2Bar = 50 ohms



(e) DIFF2 = 50 ohms, DIFF3 = 50 ohms



(f) DIFF1 = DIFF2 = DIFF3 = 50 ohms

Fig. 9. Common-mode currents on the power supply cable for different loads.

5 Conclusions

We also observed that the common-mode currents induced on cables attached to the test board were nearly independent of the differential signal waveforms. It appears that, for this board, the power bus noise is a more significant source of EMI than the differential clock signals.

Although the common-mode voltage produced by the clock driver was not the primary source of induced common-mode currents on the cables, it was still measurable. For this test board with this differential clock generator, the common-mode voltage was found to have a magnitude of about 0.1 volts, independent of the clock frequency. The primary source of this common-mode voltage appears to be the imbalance between the risetime and the falltime of the signals. The risetime is about 0.8 times the falltime on both sides of the differential output. Future investigations will examine the effect of loading on the transition times of this driver.

References

[1] H. W. Johnson, *High-Speed Digital Design: A Handbook of Black Magic*, New Jersey, Prentice Hall, pp. 319-320, 1993