University of Missouri-Rolla
Electromagnetic Compatibility Laboratory

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EMC DESIGN GUIDELINES

prepared for

Boeing Commercial Avionics Systems

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EMC DESIGN GUIDELINES

1. INTRODUCTION

1.1 PURPOSE

The purpose of these electromagnetic compatibility (EMC) design guidelines is to reduce the risk of avionic line replaceable unit (LRU) noncompliance with high intensity radio frequency (HIRF) and multiple burst lightning (MBL) susceptibility requirements. These same guidelines will reduce electromagnetic emissions.

These guidelines provide design engineers with specific recommendations concerning printed circuit board (PCB) layout, metal enclosure design, and cable selection and shielding. The emphasis is on EMC design of analog and digital circuits in avionic type enclosures as used on Boeing Commercial Transport Airplanes. The guidelines will help meet the EMC requirements defined by the following documents.

- D6-16050,-2,-3,-4, Electromagnetic Interference Control Requirements.
- RTCA D0-160B, Environmental Conditions and Test Procedures for Airborne Electronic/Electrical Equipment and Instruments.
- RTCA D0-160C, Environmental Conditions and Test Procedures for Airborne Equipment.
- D6-44588, Electrical Requirements for Utilization Equipment Installed on Commercial Transport Airplanes.

1.2 CONTROLLING AUTHORITY

These guidelines were developed by Commercial Avionics Systems. Please direct any questions or recommended changes to _____.

1.3 HOW TO USE

Section 2, General EMC Principles, is a review of basic concepts related to the reduction of electrical noise emission and susceptibility. This section explains in general terms what to do and why it is important, but does not contain specific detailed recommendations. Those who are experienced with EMC design may want to skip this section.

The remaining sections cover Printed Wiring Boards, Metal Enclosures, and Cabling. Each section begins with general design guidelines that should be implemented in nearly all cases. All designers should be aware of these general guidelines. Next, specific guidelines are listed for subsets of the main topic, such as ARINC-429 signals on printed wiring boards. A designer may not need to be familiar with the specific guidelines for all subsets.

2. GENERAL EMC PRINCIPLES

Electromagnetic compatibility (EMC) means that electrical systems can function in their environment without emitting or receiving unacceptable levels of electromagnetic energy. The allowed levels of emission or susceptibility depend on the specific applications. Avionic susceptibility requirements are primarily determined by high intensity radio frequency and multiple burst lightning ambients. Every electrical noise problem consists of an interfering source, energy coupling mechanism and susceptible system. EMC design begins with a specification of the noise ambient in terms of electric and magnetic field amplitudes plus conducted common mode current levels on wiring. Next the electrical system is evaluated to determine the most likely energy coupling mechanisms. Then noise control techniques are designed into the system to counter the anticipated susceptibility or emission possibilities.

2.1 BASIC CONCEPTS

2.1.1 The deciBEL (dB)

The deciBel is formally defined as the ratio of two powers (P), but is often used as the ratio of two voltages (V) or two electromagnetic field amplitudes (E).

$$dB = 10 \log (P_2/P_1) = 20 \log (V_2/V_1) = 20 \log (E_2/E_1)$$

Common reference values are P_1 = 1 mW, V_1 = 1 μV and E_1 = 1 μV/m. This yields

$$dBmW = 10 \log (P_2/1mW);$$
$$dB\mu V = 20 \log (V_2/1\mu V);$$
$$dB\mu V/m = 20 \log (E_2/1\mu V/m).$$

Most dB ratios are arranged to yield a positive number. If a noise voltage level were reduced from 100 mV to 1 mV, the change would be referred to as a +40 dB decrease (20 log 100 mV/1 mV) rather than a -40 dB increase. If the maximum electric field emission at some frequency was +36 dBμV/m, this would correspond to

$$+36\ dB\mu V/m = 20 \log (E_2/1\mu V/m)$$

or E_2 = 63.1 μV/m. Every factor of 10 change in voltage or field amplitude causes a 20 dB change in the deciBel value.

2.1.2 Frequency, Wavelength and Standard Frequency Bands

Frequency (f) and wavelength (λ) are related by

$$f\lambda = c = 1/\sqrt{\mu\varepsilon}\ ,$$

where c equals the wave velocity and μ and ε equal the permeability and permittivity (dielectric constant) of the material. For example, if f = 100 MHz and

$$c = 1/\sqrt{\mu_o\varepsilon_o} = 3\times10^8\ m/s$$

then

$$\lambda = \frac{c}{f} = \frac{3\times10^8\ m/s}{100\ MHz} = 3\ m.$$

To calculate the wave velocity for a printed circuit board, use $\mu = \mu_o$ and $\varepsilon = \varepsilon_R\ \varepsilon_o$, where ε_R is the relative permittivity.

There are several standard frequency band designations such as HF, VHF, UHF or A, B, C, or X, Ka, Ku. An example is shown in Table 2.1.2-1

Band Designation	Frequency Range	Wavelength Range
HF	3 - 30 MHz	100 - 10 m
VHF	30 - 300 MHz	10 - 1 m
UHF	300 - 3000 MHz	1 - 0.1 m

Table 2.1.2-1 Frequency and wavelength ranges of standard bands.

The relative terms "high" and "low" frequency are often encountered. From an EMC viewpoint, "high" frequency means that the system is large compared to a wavelength or the time delay along the wiring is large compared to typical transition times. These conditions are approximated by system dimensions > wavelength/20 or propagation delays > transition time/4. For "high" frequencies, the system must be described by distributed, rather than lumped, electrical circuit parameters. Interconnecting wiring must be viewed as transmission lines requiring matched terminations and as possible undesired antennas. Openings in metal enclosures must be considered as possible electromagentic coupling apertures.

2.1.3 Current Flow Path

Current takes the path of least impedance (Z). Impedance consists of resistance (R) and reactance (X), $Z = R + jX$. Every current requires a minimum of two conductors (wires or circuit board traces), one each for output and return. Any two conductor current path can be modeled as a distributed per unit length series resistance (R), series inductance (L), and shunt capacitance (C) as shown in Figure 2.1.3-1.

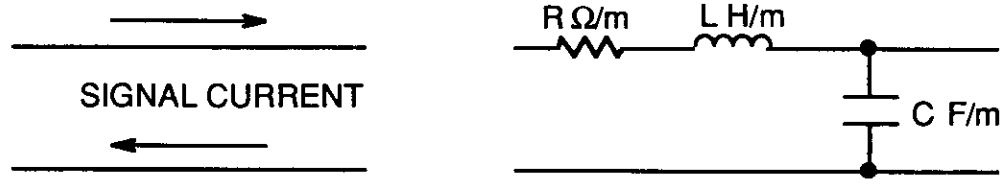


Figure 2.1.3-1 Distributed equivalent circuit for a two conductor current path.

The per unit length series impedance $R + j\omega L$ is generally more important for low load impedances ($Z_L < 100\ \Omega$) and the shunt impedance is more important for high load impedances ($Z_L > 1\ k\Omega$). For frequencies $f \geq 3$ kHz, $\omega L > R$. The current flow path on wiring and printed circuit boards is determined by minimum inductance, not minimum resistance, for $f > 3$ kHz.

Current takes the smallest loop area (least impedance) path for frequencies above 10 kHz.

For two parallel round wires of radius a and separation d, the per unit length self inductance $L \approx (\mu/\pi)\,\ell n\,(d/a)$, where μ equals the permeability of the medium surrounding the wires. The self inductance of a current loop increases with the loop area and decreases as the wire size increases.

For distributed wiring, $LC = \mu\epsilon$, where μ and ϵ are the permeability and permittivity of the material surrounding the wires. In many cases $\mu\epsilon$ = constant = LC. Hence, the capacitance and inductance must be inversely related. If two parallel wires are moved closer together, the capacitance increases and the inductance decreases. If the diameters of the two wires are increased while their center-to-center spacing is held fixed, the capacitance increases and the inductance decreases.

2.1.4 Pulse Bandwidth

A typical pulse is shown in Figure 2.1.4-1. The transition time is defined to be the time between the 10% and 90% amplitude values. If the leading and trailing edges have different transition times, then the shortest time is used to estimate the "maximum" frequency produced by the pulse.

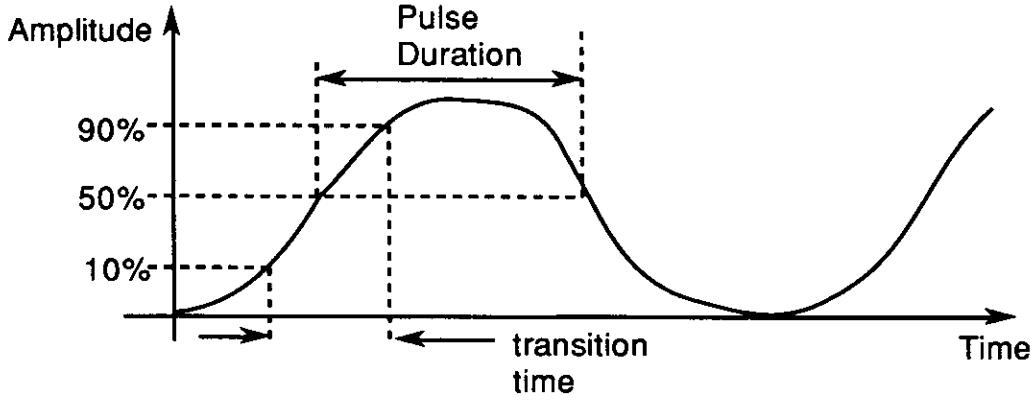


Figure 2.1.4-1 Definition of pulse duration and transition time.

Figure 2.1.4-2 shows the envelope of the maximum amplitude of the harmonic frequencies. At the frequency

$$f_{max} = \frac{1}{\pi \times \text{minimum transition time}}$$

the amplitude is more than 20 dB below the fundamental level, and beyond f_{max} the amplitude decreases at the rate of 40 dB/decade. For signals of similar amplitudes, such as two 5 V digital signals, the amplitude at f_{max} is not normally sufficient to cause mutual interference. If the two signals are largely different in amplitude, such as a 5 V digital signal and a 5 mV analog signal, then the maximum digital frequency that could cause interference would exceed f_{max}, since 5 mV is 60 dB below 5 V.

If a signal has a transition time of 1 ns, then an estimate of the maximum frequency with a significant amplitude compared to the fundamental frequency is

$$f_{max} = 1/(\pi \times 1\,\text{ns}) = 318\,\text{MHz}\,.$$

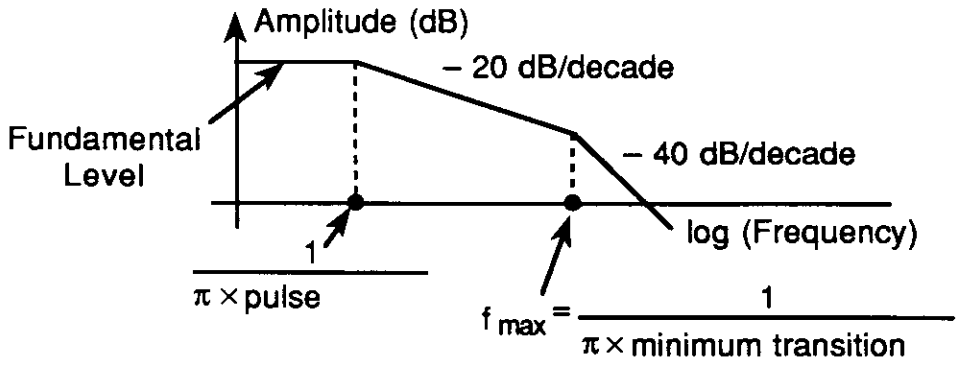


Figure 2.1.4-2 Envelope of the maximum amplitude of the harmonic frequencies produced by a periodic pulse.

2.1.5 Transmission Lines

Wiring should be treated as a transmission line whenever:

line length > wavelength/20

or

time delay along the wiring > transition time/4.

Transmission lines require both a constant characteristic impedance (Z_o) and a matched termination in order to avoid reflections. The characteristic impedance is held constant by maintaining constant conductor size and spacing. Typically Z_o > 40 Ω to avoid excessive line drive current and Z_o < 120 Ω to reduce emission or susceptibility. Coaxial cables have Z_o = 50 Ω for traditional reasons, Z_o = 75 Ω for minimum signal attenuation and Z_o = 93 Ω for reduced drive current.

Sections of lines, such as connectors, that are shorter than the minimum wavelength/20 do not require a constant impedance. The two signal conductors must be adjacent to one another to minimize cross coupling with other lines.

Figure 2.1.5-1 shows a transmission line connecting a source and load. If the power flows in only one direction, from source to load, then it is necessary to match only one end of the line, either $Z_L = Z_o$ or $Z_s = Z_o$. If power flows in both directions (bidirectional) then both ends must be matched. Balanced transmission lines, such as ARINC 429 and 629, require both a matched and balanced termination. Figure 2.1.5-2 shows several examples of balanced line matching techniques.

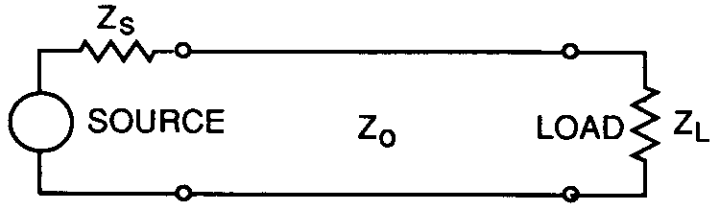


Figure 2.1.5-1 A transmission line connecting a source and load.

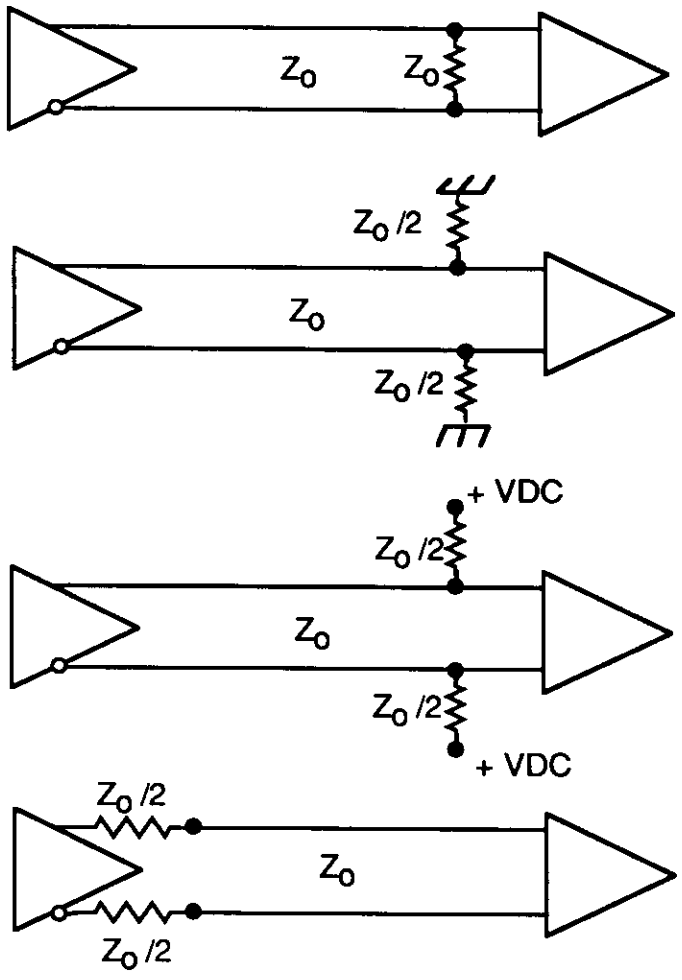


Figure 2.1.5-2 Example balanced line matching techniques.

2.1.6 Common and Differential Modes

Common mode (CM) and differential mode (DM) voltage and current definitions are shown in Figure 2.1.6-1. The DM current is the equal and opposite current. The CM current on a pair of wires or a bundle of wires is the total net current on the wires.

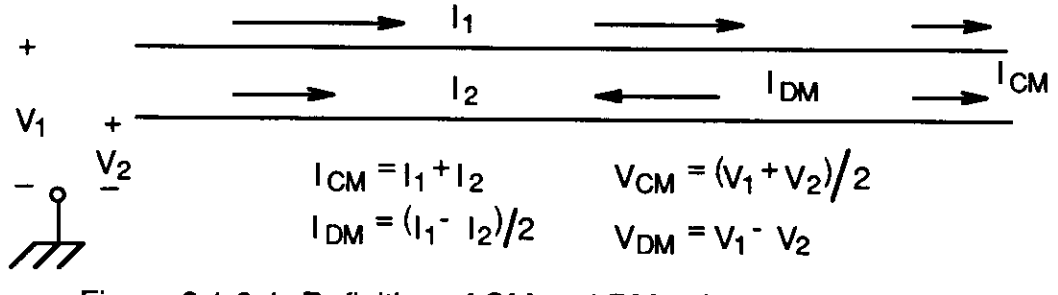


Figure 2.1.6-1 Definition of CM and DM voltages and currents.

This would be the current measured by a clamp-on current probe surrounding the entire bundle. The CM currents are usually the cause of high frequency (MHz to GHz) emission and susceptibility problems. These currents are usually neglected by most circuit analysis programs. High frequency EMC requires an understanding of CM current sources and control techniques.

2.1.7 RF Models for R, L and C

High frequency equivalent circuits for a resistor, capacitor, and inductor are shown in Figure 2.1.7-1. The lead inductance for the resistor and capacitor cannot be determined until the entire loop formed by the connecting leads is known. The capacitor acts like an inductor above the series resonant frequency $f_R \approx 1/2\pi\sqrt{LC}$ and the inductor acts like a capacitor above the parallel resonant frequency $f_R \approx 1/(2\pi\sqrt{LC})$.

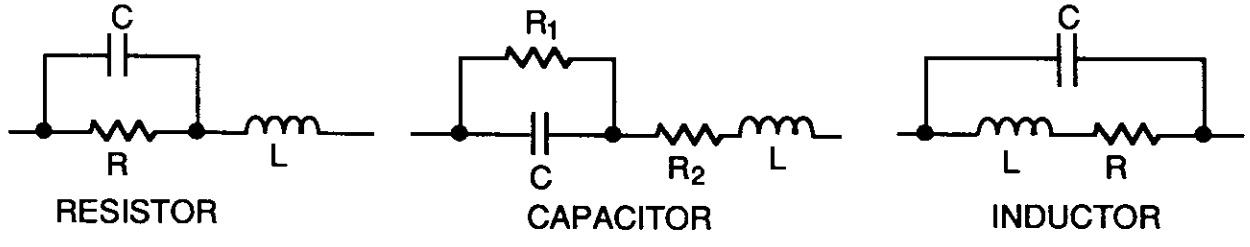


Figure 2.1.7-1 High frequency equivalent circuits for a resistor, capacitor, and inductor.

2.1.8 DC Power Distribution

Minimize DC Bus Z_o

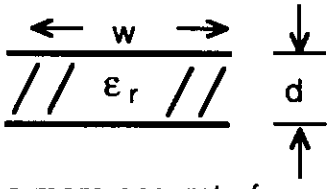
DC power bus design is the single most important factor affecting EMC. A DC distribution bus often carries high frequency currents and should be modeled as a distributed series inductance and shunt capacitance as shown in Figure 2.1.3-1. The characteristic impedance $Z_o = \sqrt{L/C}$ is an excellent figure of merit for a DC distribution bus. A large capacitance is necessary to filter noise conducted along the bus. A small inductance reduces emission and susceptibility. The ideal value is $Z_o = 0\ \Omega$. The more critical the emission threat (as indicated by shorter rise times or larger transient levels) or the susceptibility (such as mV level analog signals) the lower the required DC bus Z_o.

The characteristic impedance for flat conductors positioned one above the other is given by

$$Z_o \approx \sqrt{\frac{\mu}{\varepsilon}}\,(d/w) = \frac{377}{\sqrt{\varepsilon_r}}\,(d/w)\ \Omega,\ \text{for}\ w >> d,$$

where

ε_r = relative permittivity,
w = conductor width,
d = conductor separation.



When w ≈ d or w < d, this simple formula is not valid. Use a more accurate formula or the Greenfield simulation from Quantic.

Approximate values of Z_o for flat parallel conductors are shown in Figure 2.1.8-1.

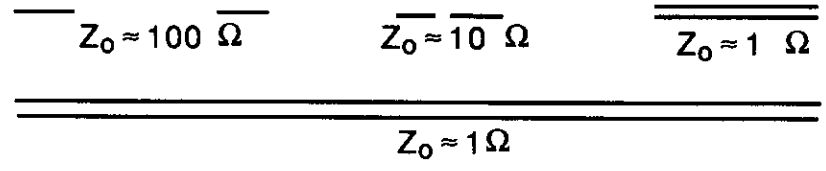


Figure 2.1.8-1 Approximate values of Z_o for flat parallel conductors.

Sizing Decoupling (Bypass) Capacitors

The simplified equivalent circuit for DC decoupling consists of a capacitor and series inductance as shown in Figure 2.1.8-2.

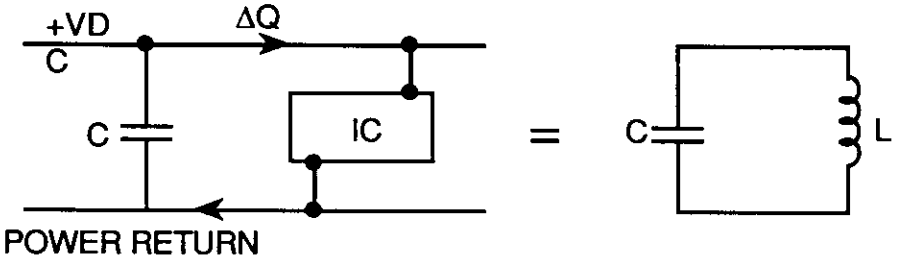


Figure 2.1.8-2 DC bus decoupling equivalent circuit.

The minimum decoupling capacitor value is determined by

$$C_{MIN} = \frac{\Delta Q}{\Delta V_{MAX}} = \frac{\int Idt}{\Delta V_{MAX}} \approx \frac{I_o \Delta t/2}{\Delta V_{MAX}}$$

where

ΔQ = transient charge required, assuming a triangular shaped current spike of peak amplitude I_o and time duration Dt,

ΔV_{MAX} = maximum acceptable change in DC voltage.

For example, if I_o = 2 mA, Δt = 10 ns, and ΔV_{MAX} = 50 mV, then C_{MIN} = 200 pF.

The maximum decoupling capacitor value is determined by the series inductance and the maximum frequency (f_{MAX}) that must be filtered by the decoupling circuit. The series resonant frequency f_R should not be significantly above f_{MAX}. A simple rule is to require

$$f_R = \frac{1}{2\pi\sqrt{LC}} \leq f_{MAX} = \frac{1}{\pi \times \text{minimum transition time}}.$$

Figure 2.1.8-3 shows the typical impedance versus frequency for a bypass capacitor with series wiring inductance. It is very critical to minimize the series inductance in order to expand the useful frequency range of the decoupling capacitor. Less capacitance with a smaller discharge loop area is much more effective than a larger capacitor and larger loop area.

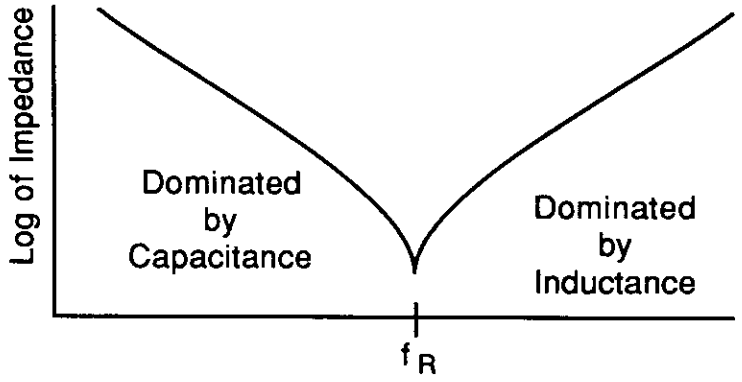


Figure 2.1.8-3 Log-Log plot of impedance versus frequency for a series capacitor and inductor.

2.2 NOISE COUPLING MECHANISMS

Electrical energy (power, signal or noise) can be transferred from place to place by only four coupling mechanisms:

1. Conductive;
2. Capacitive;
3. Inductive; and
4. Electromagnetic.

Conductive coupling occurs over two or more metal wires. Capacitive and inductive coupling represent the transfer of stored electric or magnetic energy. Electromagnetic coupling is radiated energy from the noise source. The precise distance at which the electric and magnetic fields associated with the radiated energy are greater than the fields associated with the stored (non-radiated) energy depends on the size of the noise source, but is always greater than one wavelength.

2.2.1 Conductive Coupling

Conductive or common impedance coupling requires two or more connections, usually metallic, to the noise source. Figure 2.2.1-1 shows how the DC current drawn by one circuit module can affect the DC voltage at an adjacent circuit module because of the common line impedance.

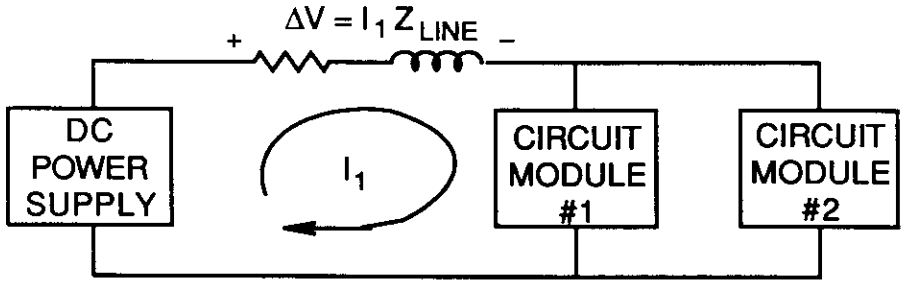


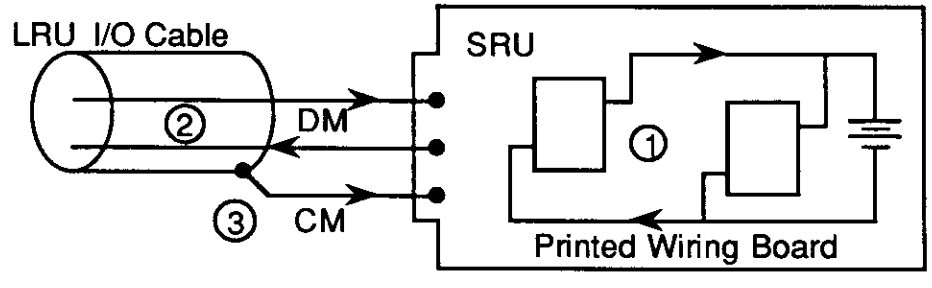
Figure 2.2.1-1 Conductively coupled noise through a common DC power line impedance.

Typical connections involving conductive coupling are:

AC or DC power;
multiple grounding or signal referencing connections;
signal lines; and
cable shields.

Figure 2.2.1-2 shows several typical examples of conductive coupling on an LRU I/O cable connected to an internal SRU.

Conductive coupling is the most frequently encountered mechanism. It is important to know whether the conductive coupling is DM or CM so that the proper type of filter can be used. Most electromagnetic radiation begins and ends as undesired CM currents on wires and metal surfaces. A clamp-on type current probe with mA sensitivity and MHz bandwidth can measure CM conducted emissions. A clamp-on bulk current injection probe can be used to test for CM conducted susceptibility.



① Transient DM conductive coupling on the DC bus between circuit modules.

② DM conductive coupling either in or out on signal lines.

③ CM conductive coupling in or out on the cable shield.

Figure 2.2.1-2 Examples of conductive coupling.

2.2.2 Capacitive Coupling

Capacitive or electric field coupling represents the transfer of electric stored energy over a distance typically less than a wavelength. The equivalent circuit for capacitive coupling is shown in Figure 2.2.2-1.

Capacitive coupling is worsened by fast switching voltages, high signal circuit impedances and large metal surface areas. To determine the equivalent impedance of the susceptible circuit to the capacitively coupled noise current, the susceptible circuit source and load impedances must be modeled as in parallel. If for example Z_S = 1 Ω and Z_L = 1 MΩ then the equivalent impedance encountered by the capacitively coupled noise current would only be 1 Ω. In this case the resulting noise voltage would probably be negligible compared to the signal voltage level. A high impedance noise source generates electric fields and a high impedance susceptible circuit responds to electric fields. For EMC purposes an impedance is rated high or low relative to 377 Ω, the intrinsic impedance of free space.

$$Z_o = \sqrt{\mu_o/\varepsilon_o} = 377\ \Omega\ .$$

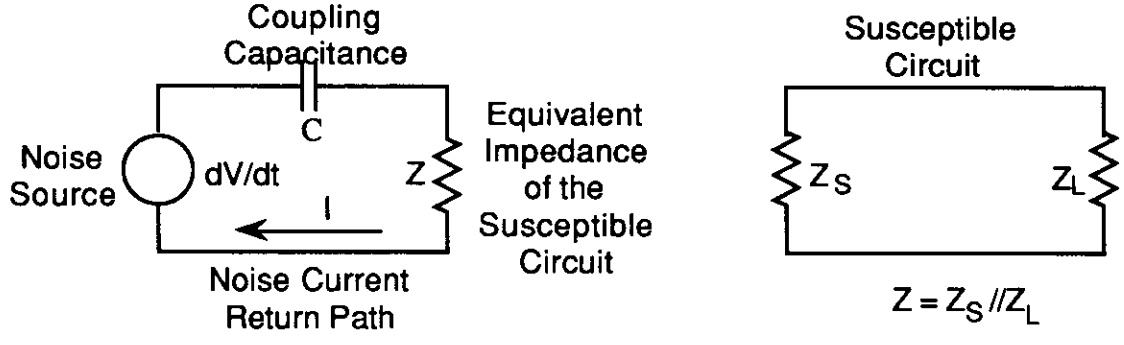


Figure 2.2.2-1 Equivalent circuit for capacitive coupling of noise.

2.2.3 Inductive Coupling

Inductive or magnetic coupling represents the transfer of magnetic stored energy over a distance typically less than a wavelength. The equivalent circuit for magnetic coupling is shown in Figure 2.2.3-1. Magnetic coupling is worsened by fast switching currents, high signal circuit load impedance (Z_L), and large loop areas. A low impedance noise source generates magnetic fields and a susceptible circuit with a low loop impedance ($Z_S + Z_L$) or a high load impedance (Z_L) responds to magnetic fields.

2.2.4 Comparing Capacitive and Inductive Coupling

The electric field generated by a noise source depends on dV/dt and the magnetic field depends on dI/dt. The ratio of these two derivatives may indicate which of these two noise coupling mechanisms is dominate. If:

$$\frac{dV/dt}{dI/dt} << 377\ \Omega,$$ magnetic coupling probably dominates;

$$\frac{dV/dt}{dI/dt} >> 377\ \Omega,$$ capacitive coupling probably dominates.

This derivative ratio only suggests a probable dominate mechanism, other factors such as mutual capacitance and mutual inductance values must also be considered.

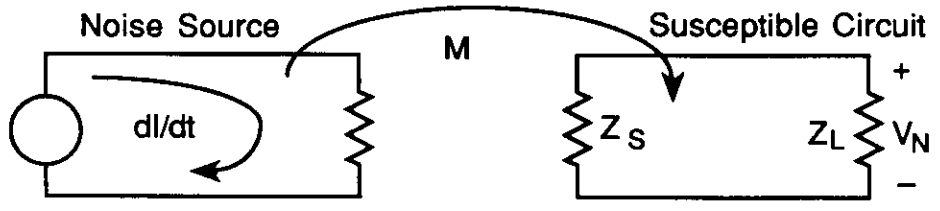


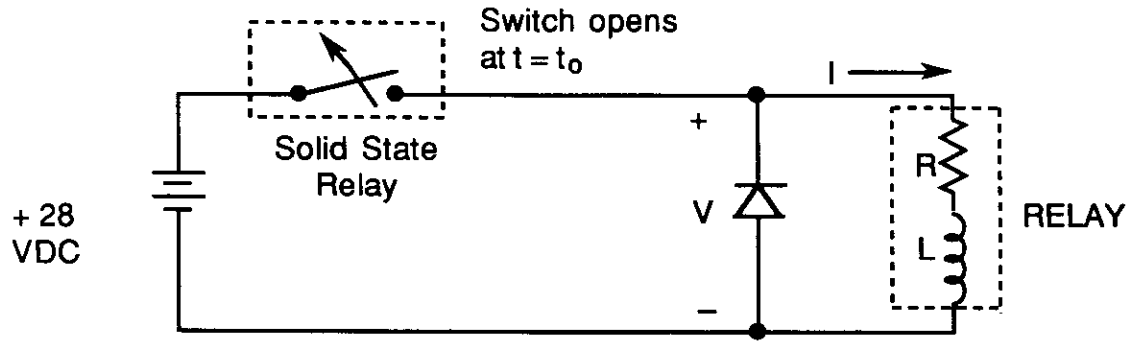
Figure 2.2.3-1 Equivalent circuit for magnetic coupling of noise.

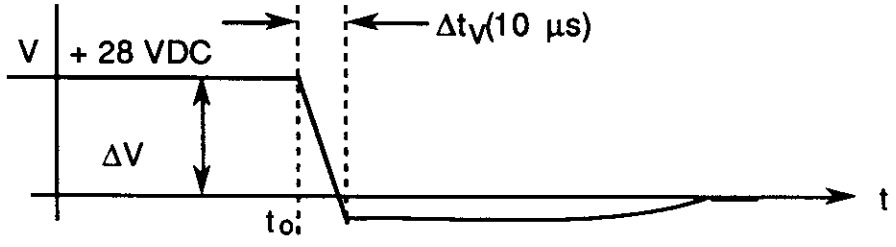
For pulse waveforms the dt represents the transition time (switching time or rise time). In most cases the transition times for the voltage and current transients are not the same. The main concern is the transient voltages and currents, not the steady state values. Example transient generators are de-energizing relay coils, electrostatic discharge, fast switching digital circuits, and arcing relay contacts. Figure 2.2.4-1 shows that a de-energized relay probably generates more capacitive than magnetic coupled noise.

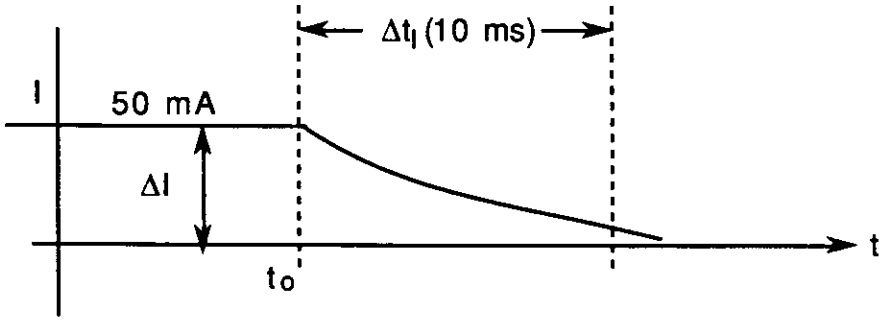
2.2.5 Electromagnetic Coupling

Electromagnetic coupling represents the transfer of radiated energy that is in the far field of the noise source. The far field begins at a distance of approximately one wavelength for a noise source with dimensions much less than a wavelength. For a noise source with dimensions greater than a wavelength, the far field distance could be several wavelengths. At distances less than a wavelength, the near field capacitive and magnetic coupling mechanisms dominate the electromagnetic coupling. Hence, electromagnetic coupling requires a distance between the noise source and the susceptible circuit that is greater than one wavelength.

Noise coupling between adjacent wires in a bundle cannot be electromagnetic coupling, while noise at 300 MHz between wires 10 m apart might be electromagnetic coupling since $d = 10\ m > \lambda = 1\ m$.







$$\frac{dV/dt}{dI/dt} \approx \frac{\Delta V/\Delta t_V}{\Delta I/\Delta t_I} \approx \frac{2\ V/1\ \mu s}{5\ mA/1\ ms} = 56\ k\Omega$$

Since 560 kΩ >> 377 Ω, then capacitive coupling is probably worse than magnetic coupling.

Figure 2.2.4-1 Comparing capacitive and magnetic coupling produced by a de-energizing relay.

2.2.6 Summary

The key features that help to identify the type of coupling produced by a noise source are shown in Table 2.2.6-1.

Noise Source Coupling Mechanism	Identifying Feature
Conductive	Two or more contacts
Capacitive	(dV/dt) / (dI/dt) >> 377 Ω
Inductive	(dV/dt) / (dI/dt) << 377 Ω
Electromagnetic	Distance > Wavelength

Table 2.2.6-1 Key features that help to identify the type of coupling produced by a noise source.

For example, noise coupling between circuit modules or traces on a printed wiring board cannot be electromagnetic radiation because the distance is not greater than one wavelength. This type of noise is either conductively coupled along the DC power bus, magnetically coupled between two loops or capacitively coupled between two "high" impedance circuits. The concepts presented in section 2.2 can help predict a noise problem before it occurs or identify the cause of an existing problem.

2.3 GROUNDING

2.3.1 Reasons for Grounding

Electrical safety, especially during lightning and power faults, is the main reason for grounding. Safety grounding is accomplished by bonding all exposed conducting surfaces together to reduce voltage differences. Safety grounding also involves providing a low impedance fault current return path to permit high current values which shorten the opening time of fuses and circuit breakers. Figure 2.3.1-1 shows an LRU chassis with a safety grounding connection to the airframe. This safety grounding wire should be as short as possible. The line, neutral and grounding conductors must be routed together.

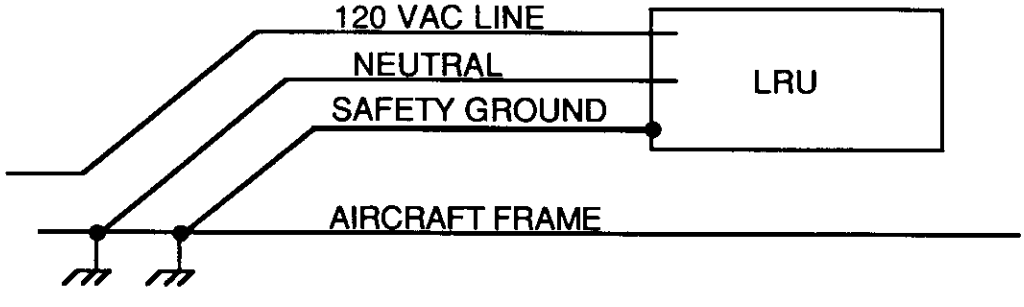


Figure 2.3.1-1 Example LRU safety grounding inside the pressure vessel.

A second reason for grounding is to provide electrical circuits with the same signal voltage reference. By reducing the CM voltage between signal reference points, both the noise and threat of damage can be reduced. If the voltage difference between signal references cannot be adequately reduced, then the interconnecting

signal lines must be metallically isolated by such devices as transformer or optical couplers.

Neither safety grounding conductors nor signal grounding conductors carry a significant amount of current under normal operating conditions. During lightning or power fault conditions safety grounding conductors may carry substantial current. A non-current carrying signal grounding conductor is not the same as a current carrying return conductor. Confusing signal grounding and signal return functions is a leading cause of noise problems. Figure 2.3.1-2 shows examples of grounding and return conductors.

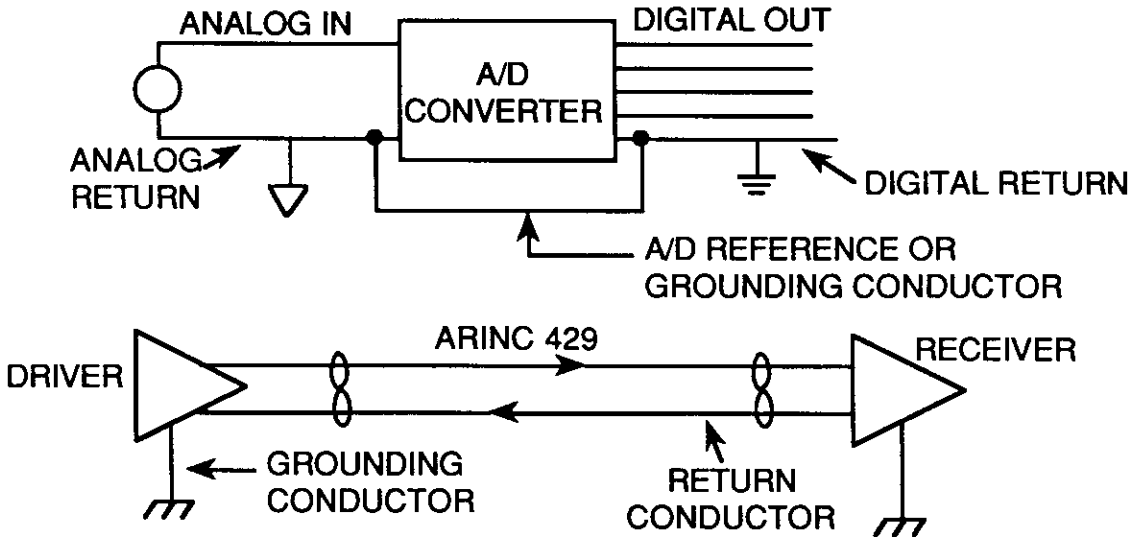


Figure 2.3.1-2 Examples of grounding and return conductors.

2.3.2 Electrical Ground Surfaces

Electrical ground consists of a good conductor with a large surface area that is sufficiently close to a system to transfer electrical energy. The ground surface should not carry significant signal current. If it does carry signal current, then the conductor is a <u>return</u> conductor and <u>not</u> a grounding conductor. The metal airframe is a current <u>return</u> for those signals flowing on the airframe, and it is also the <u>ground surface</u> for those signals not returning on the airframe.

2.3.3 Grounding and Return Symbols

All grounding symbols should be defined by a written description. The following symbols are to be used only for the purposes stated.

 Represents a connection to the metal chassis surrounding the electronic circuit or a connection to the airframe. A subscript can be used to represent a specific location on the chassis or airframe. This connection provides the grounding functions of safety and signal voltage referencing. This connection also provides the current return path for discrete signals and DC power.

 Represents a current carrying analog signal or analog DC power return connection.

 Represents a current carrying digital, discrete, or 28 VDC power return connection.

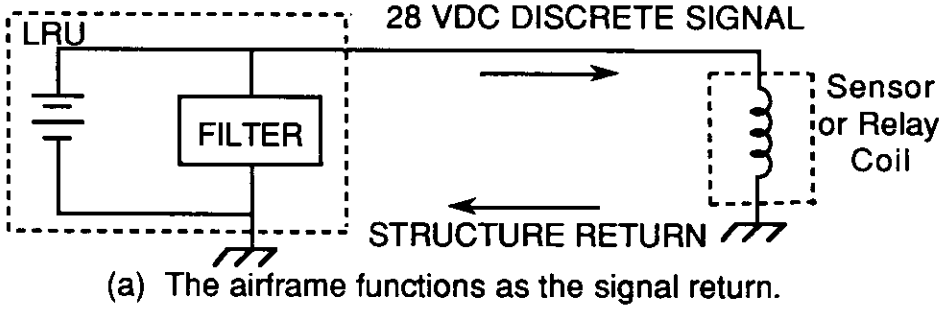
2.3.4 Signal Grounding Techniques

It is important to distinquish between a signal return function and a signal grounding function. For some signals, such as discretes, the airframe is the return path and for other signals, such as ARINC 629, the airframe is the non-signal carrying ground structure. To minimize the effects of ground voltage differences the following techniques are used:

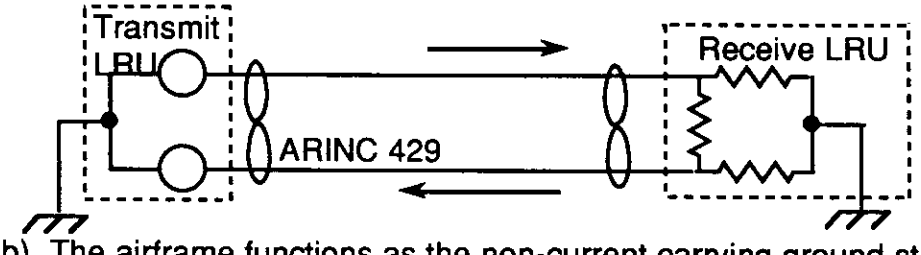
1. A low impedance ground structure such as the airframe;
2. Single point grounding, which avoids the ground voltage difference; or
3. Circuit balance, which reduces the conversion of CM ground voltage into DM signal noise.

Grounding of Signals Routed Between LRUs

Approximately DC signals, such as discretes, routed inside the pressure vessel can use the metal airframe as a return but probably requires the addition of filtering to eliminate the noise. When routed outside the pressure vessel, these signals are isolated from structure to avoid conductive contact to the voltage difference along the airframe. Wide bandwidth or low level signals are balanced to reduce the conversion of CM ground voltage into DM noise. Figure 2.3.4-1 shows these two techniques.



(a) The airframe functions as the signal return.



(b) The airframe functions as the non-current carrying ground structure.

Figure 2.3.4-1 Examples of the airframe serving as both signal return and signal ground.

Grounding of Signals Within LRUs

The signal voltage reference within an LRU is normally connected to the metal enclosure at the cable connector location to:

1. provide a discrete signal return path;
2. provide a shunting path for HIRF and ESD currents; and
3. provide a shunting path for internally generated CM currents.

The analog and digital signal references must be connected together on each wiring board that uses both signal types.

2.3.5 Ground Loops

Ground loops consist of part signal path and part ground structure in the same loop as shown in Figure 2.3.5-1. Typical examples of ground loops are:

1. A coaxial cable connected between two grounded LRUs;
2. The return plane of a backplane or motherboard connected to a metal chassis at several points;
3. The loop formed between an ARINC signal pair and the airframe.

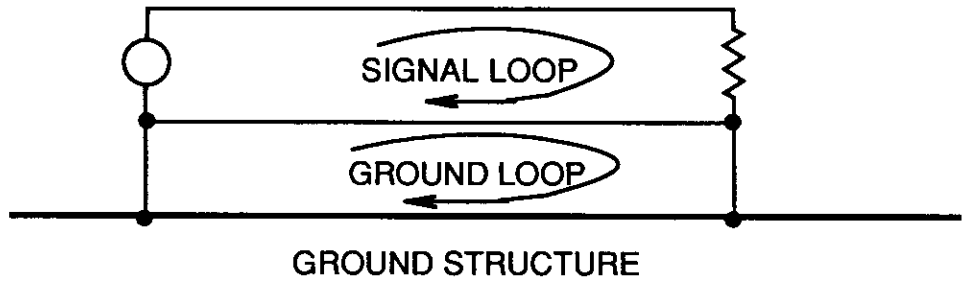


Figure 2.3.5-1 A typical ground loop.

In many cases ground loops result from necessary safety or RF noise requirements. Ground loops are more troublesome for low frequency (<1 MHz) unbalanced circuits. Ground loop noise coupling is most often conductive and occasionally magnetic. The main techniques to reduce ground loop coupling are:

1. A balanced signal circuit;
2. Single point grounding; and
3. Signal path isolation via optical or transformer coupling.

Signal balancing and transformer isolation are used in Figure 2.3.5-2 to reduce the conversion of a common mode ground voltage into differential mode signal interference.

2.4 Shielding

Shielding can be divided into two categories: that provided by the signal itself, self shielding, and that provided by added materials not associated with signal current flow. Self shielding should always be used because this technique is low cost and wide bandwidth. For severe noise environments, such as HIRF and multiple burst lightning, additional shielding may be required.

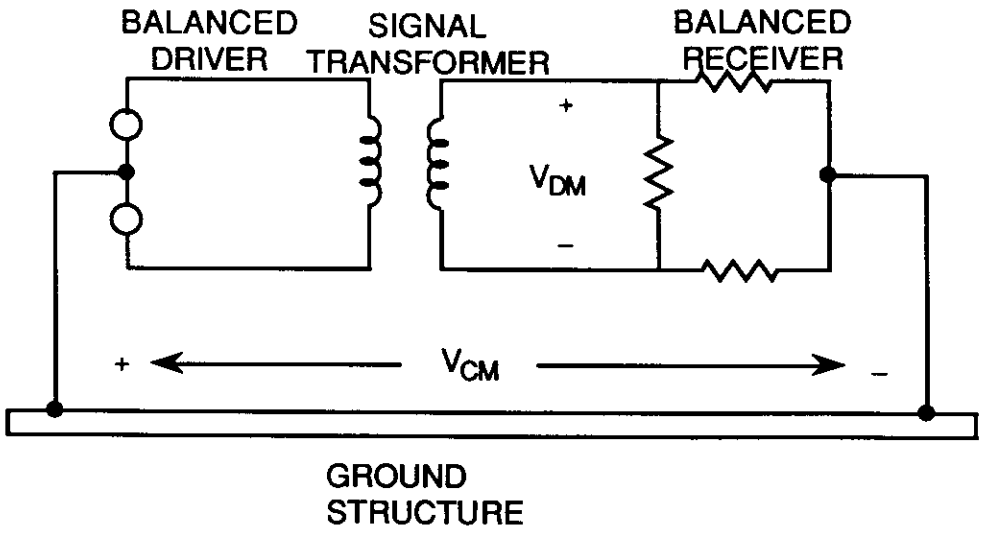


Figure 2.3.5-2 Reducing ground loop coupling, the conversion of V_{CM} into V_{DM}, by using a balanced signal circuit and transformer isolation.

2.4.1 Self Shielding

Magnetic field self shielding requires positioning the signal output and return currents such that they produce nearly zero external magnetic field. This is usually accomplished by minimizing loop area. Both magnetic field emission and susceptibility are reduced. Several examples of different degrees of magnetic self shielding are shown in Figure 2.4.1-1. The shielding is provided by the location of the currents and does not involve the use of magnetic materials.

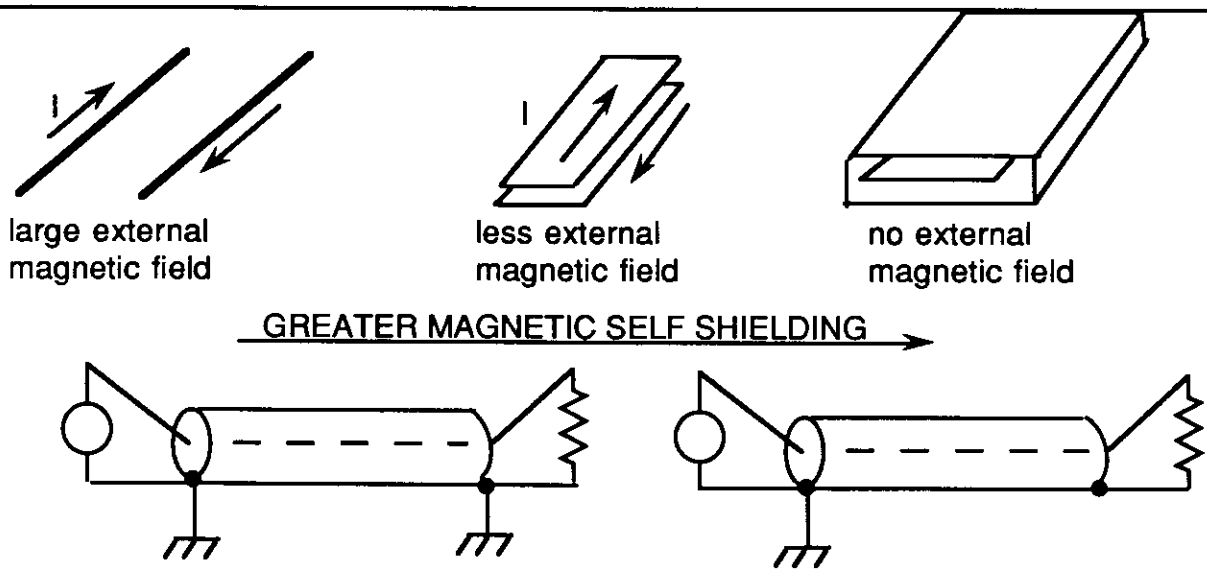


Figure 2.4.1-1 Examples of magnetic self shielding.

Electric field self shielding requires positioning the electrical charges on the signal output and return conductors such that they produce nearly zero external

electric field. If possible, operate the outermost conducting surface of a component at the signal reference voltage. Figure 2.4.1-2 shows several examples.

Magnetic and electric self shielding at low frequencies usually results in improved electromagnetic self shielding at higher frequencies.

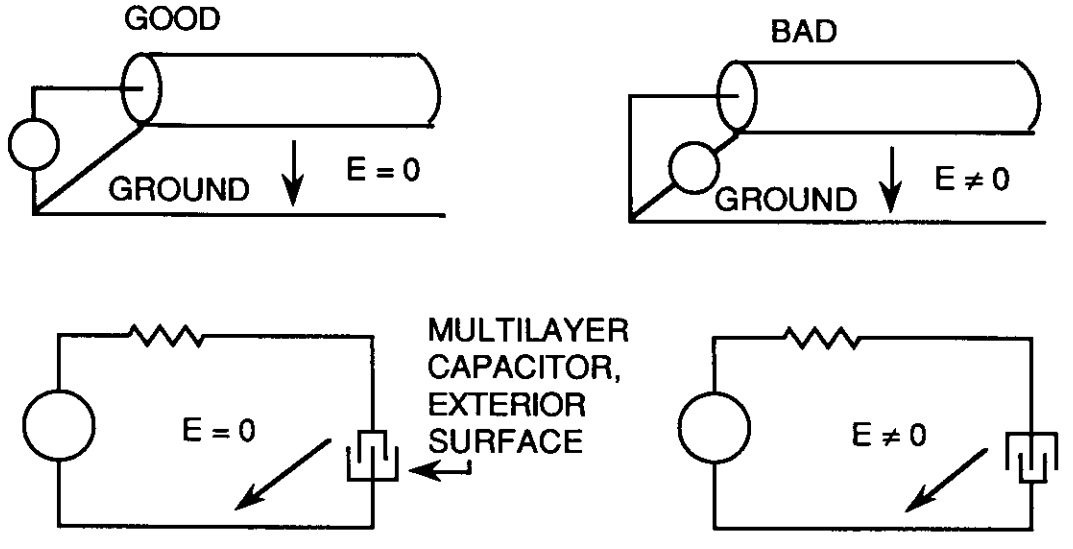
2.4.2 Additional Shielding Techniques

Shielding is used to reduce either magnetic, capacitive or electromagnetic coupling through the air or dielectric between circuits. Since there are three coupling mechansims, there are three different shielding strategies. The amount of shielding provided by an enclosure depends on the enclosure material, the geometry of openings, and the noise coupling mechanism. The shielding effectiveness in dB is defined as

$$S_{dB} = 20\log\left(\frac{\text{Electric or Magnetic Field Without the Shield}}{\text{Electric or Magnetic Field With the Shield}}\right).$$

The shielding results from a combination of absorption loss A and reflection loss R.

$$S_{dB} = A_{dB} + R_{dB}$$



Connect the outside foil of tubular capacitors to the signal reference to provide electric field self shielding.

Figure 2.4.1-2 Good and bad examples of electric field self shielding.

Magnetic Shielding

Magnetic shielding at frequencies below 10 kHz requires a high permeability material to divert the magnetic flux away from the area being protected. High permeability materials are heavy, costly, saturable (nonlinear) and frequency dependent. Magnetic shielding above 10 kHz requires only a good conductor positioned perpendicular to the magnetic flux. Eddy currents are produced that generate a magnetic flux to oppose the change in the original flux.

Neither magnetic shielding technique requires an electrical contact to the shield. However, any magnetic shield which is also a good conductor requires an electrical connection to avoid causing excessive capacitive coupling. The preferred defense against magnetic fields is proper signal current positioning, self shielding (see Figure 2.4.1-1).

Capacitive Shielding

Capacitive shielding requires the proper location and connection of a good conductor. The location allows the shield to intercept the capacitively coupled noise current before it reaches the protected circuit. The shield connection allows the noise current to return to its source. Normally capacitive shields are connected only once at the point where the current being protected is grounded. Figure 2.4.2-1 shows a capacitive shielding example.

A capacitive shield only needs to be a good conductor. The shield can have openings as long as these openings are in an area where the electric field is known to be negligible. A shield covering 98% of the length of a cable may be an effective capacitive shield yet a useless electromagnetic shield.

Electromagnetic Shielding

Shielding of a far field plane electromagnetic wave is provided by a good conductor completely surrounding the area to be protected. The shielding effectiveness is a combination of the reflection and absorption losses. For a solid conductor the absorption loss alone is 8.7 dB per skin depth. The skin depth for a good conductor is

$$\delta = 1/\sqrt{\pi\mu\sigma f},$$

where: δ = skin depth (m) ;
μ = conductor permeability (H/m);
σ = conductivity (S/m); and
f = noise frequency (Hz).

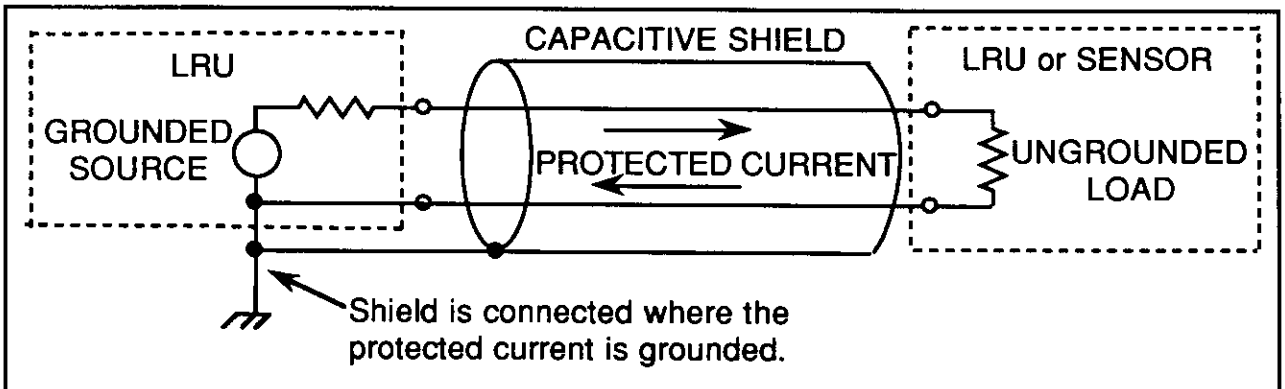


Figure 2.4.2-1 A capacitive shielding example.

Some typical values for the skin depth in copper are

Frequency	100 Hz	1 MHz	100 MHz
Skin Depth	0.66 cm	66 μm	6.6 μm

Values for the conductivity relative to copper and permeability relative to vacuum of several metals are listed in Table 2.4.2-1. The permeability of magnetic materials decreases with increasing frequency. In the MHz to GHz frequency range it is best to assume that all conductors are essentially nonmagnetic.

Material	Conductivity relative to copper, s_r	Permeability relative to vacuum, m_r
Silver	1.05	1
Cooper, annealed	1.0	1
Gold	0.7	1
Aluminum, soft	0.61	1
Brass	0.26	1
Nickel @ 1 kHz	0.20	100
Steel, @ 1 kHz	0.10	1000
Mμmetal @ 1 kHz	0.03	11,000
Mμmetal @ 10 kHz	0.03	3,000
$\sigma_r = \sigma/\sigma(\text{copper})$; $\sigma(\text{copper}) = 5.8 \times 10^7$ S/m $\mu_r = \mu/\mu_o$; $\mu_o = 4\pi \times 10^{-7}$ H/m		

Table 2.4.2-1 Relative conductivity and permeability of various metals.

Inadequate shielding effectiveness at high frequencies usually results from enclosure openings (holes and seams) or conductors penetrating the enclosure (connectors, metal shafts, etc.) To produce an "electromagnetically tight" enclosure requires careful design of openings and cable shield terminations.

Zero electromagnetic shielding should be assumed for enclosures with openings whose linear dimensions exceed one half of a wavelength. The objective is to minimize the area and length of any opening. A large number of small circular openings are preferred over one elongated slot of the same total area. The quantitative prediction of aperture coupling is complicated and cannot be described in this brief overview. A general guideline is to keep the linear dimension of openings less than wavelength/20.

For a cable shield and metal enclosure to form an electromagnetically tight seal above 10 MHz, the shield must bond 360° to the enclosure. This is usually accompolished with a metal connector shell. The connector shell must have 360° bonding to the enclosure. For shielding at frequencies below 10 MHz, pigtail connections with an effective length less than about 2 inches can be used. The positioning of the pigtail as shown in Figure 2.4.2-2 to minimize inductance (loop area) results in an effective length less than 2 inches but an actual wire length greater than 2 inches to ease assembly and repair. Tie wrapping the excess pigtail length against the cable shield must be specified on the cable drawing.

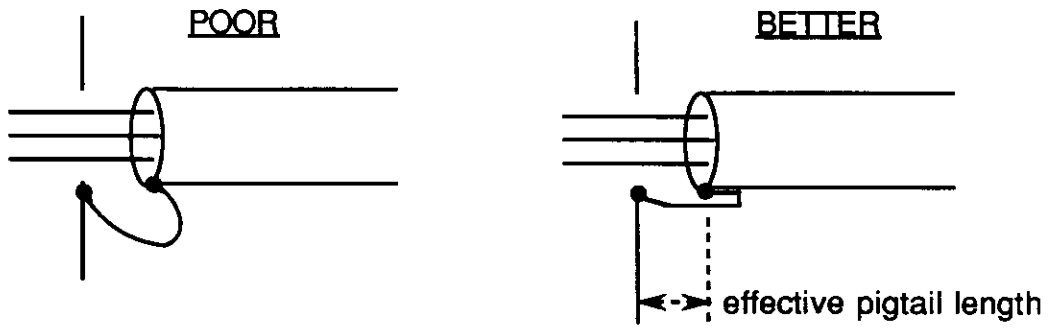


Figure 2.4.2-2 Preferred position and effective length of a shield pigtail.

If an insulated conductor passes through an enclosure opening, then zero electromagnetic shielding should be assumed. If the conductor connects internally to the enclosure then all frequencies, even DC, may pass into or out of the enclosure.

2.5 FILTERING

Filtering is the only solution technique for conductive (common impedance) coupled noise. An electrical filter is a device that can separate electrical energy based on some selection criteria. Typical filter types are

- Frequency selective (low pass)
- Mode selective (CM rejection)
- Amplitude selective (surge suppressor).

Figure 2.5-1 shows these different selective criteria in an AC line filter. If the frequency range, mode (common or differential) and amplitude of the conductive noise are known, then an appropriate filter can be designed.

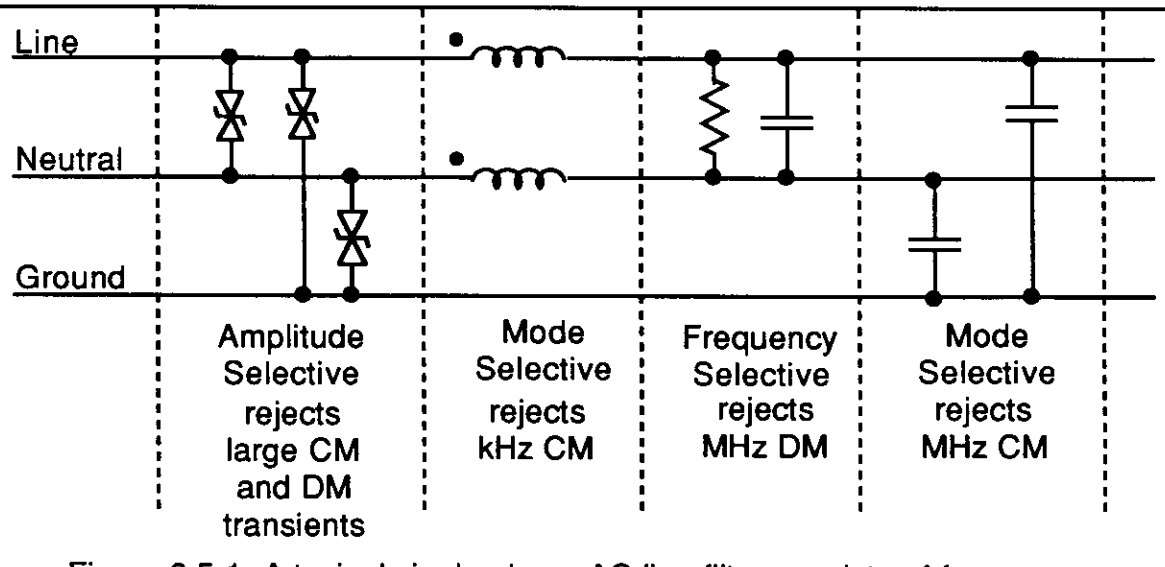
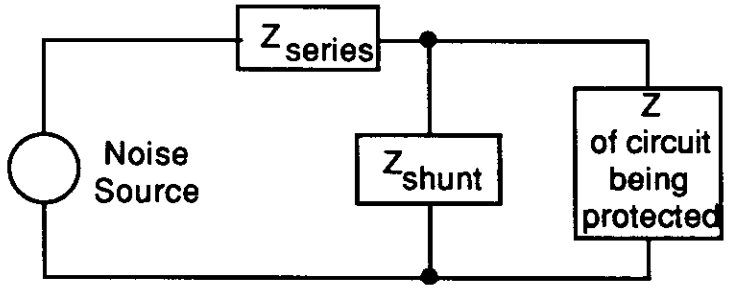


Figure 2.5-1 A typical single phase AC line filter consists of frequency, mode and amplitude selective sections.

The impedance of the circuit being protected determines whether a series or shunt filter is used, as shown in Figure 2.5-2. If the signal circuit impedance >> 377 Ω, then a shunt (usually capacitve) filter element is preferred. For an impedance << 377 Ω a series R-L filter is preferred.



If Z >> 377 Ω, use $Z_{shunt} < 0.1$ Z.

If Z << 377 Ω, use $Z_{series} > 10$ Z.

Figure 2.5-2 The signal circuit impedance determines whether a series or shunt filter is used.

2.5.1 Balancing (Common Mode Filtering)

A circuit must be balanced to reduce the conversion of common mode energy into differential mode energy. Voltage differentials along the airframe due to HIRF and MBL are examples of CM noise sources. A circuit is balanced when the current output and return paths are electrically identical. An example of a balanced circuit is shown in Figure 2.5.1-1.

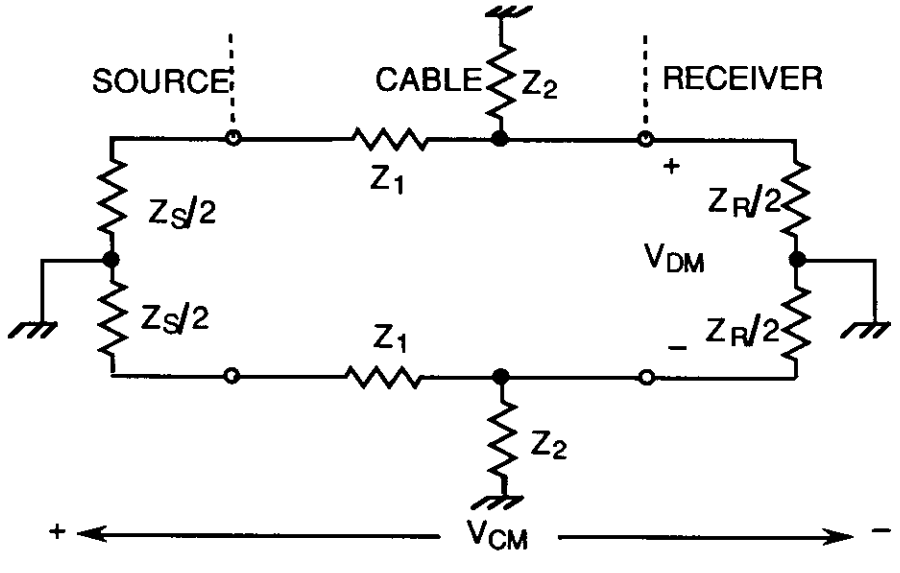


Figure 2.5.1-1 An example of an impedance balanced circuit.

Balance requires that the series impedances (Z_1) along the output and return paths be equal and that the shunt impedances (Z_2) be equal. The signal source and receiver impedances must also be balanced relative to the signal grounding point. The impedance balance must be maintained for the signal source, interconnecting cable, and receiver circuit. Z_2 normally represents a stray shunt capacitance from each signal line to ground. To make these two capacitors equal requires that each signal wire have the same diameter, length and position.

An example of an unbalanced circuit is shown in Figure 2.5.1-2. Neither the source impedance Z_S nor the receiver impedance Z_R are balanced relative to signal ground. The coaxial cable does not have equal series resistances and equal shunt capacitances to ground for each wire.

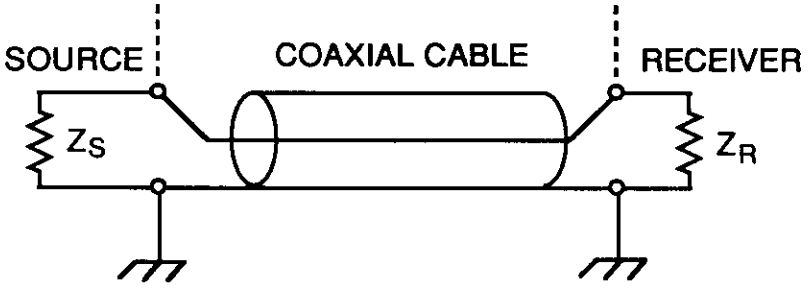


Figure 2.5.1-2 An example of an impedance unbalanced circuit.

The degree of balance is measured by the common mode rejection ratio (CMRR).

$$CMRR\ (dB) = 20 \log (V_{CM}/V_{DM})$$

If any one part of the circuit is significantly unbalanced, then the common mode rejection ratio will be drastically reduced. For cabling longer than one meter, the capacitive shunt balance in the cable usually limits the system common mode rejection. Twisted shielded pair cable provides a much better balance than coaxial cable or single wires with the airframe structure as return. Wide bandwidth signals, such as ARINC 429 and 629, use a balanced circuit to reject CM from the airframe. Narrow bandwidth circuits, such as discretes, can use an unbalanced structure return because the CM noise that is converted to DM is removed by frequency filtering.

2.5.2 Bypassing (Frequency Filtering)

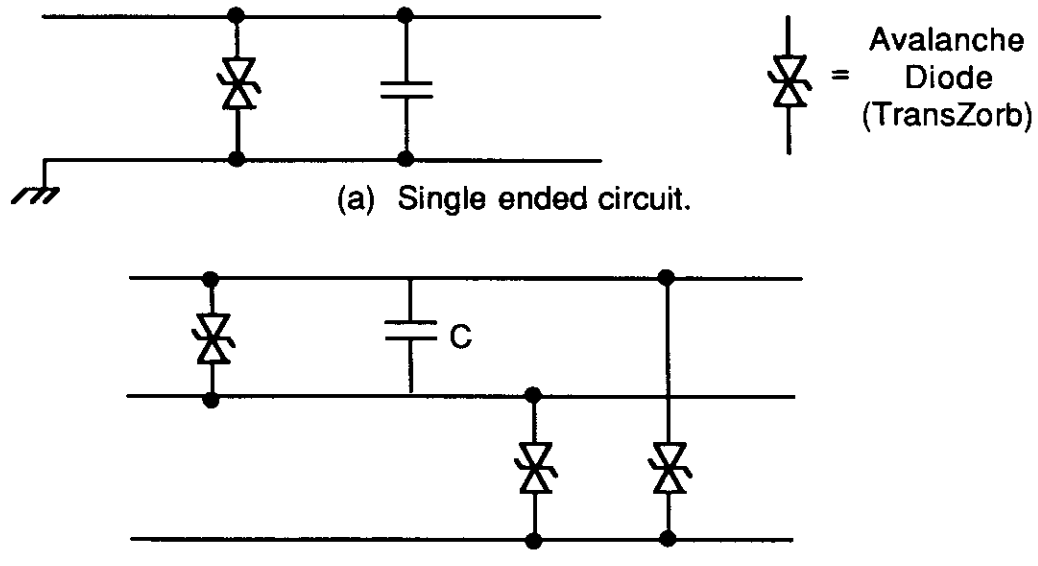
The purpose of bypassing is to provide high frequency CM and DM filtering. The decoupling of the DC power bus for integrated circuits is a specific example that was described in 2.1.8. All AC power imputs to LRUs and DC power inputs to SRUs require shunt capacitive bypassing.

2.5.3 Transient Suppression (Amplitude Filtering)

Transient suppression is a combination of amplitude, frequency and mode selective filtering. The main objective is to limit the amplitude of any unwanted CM or DM voltages. There are three transient protection devices: gas tube, metal oxide varistor and avalanche diode. The gas tube (spark gap) has a relatively slow

response time of ~ 1 μs, but can handle kWs of peak power with only a few pF of shunt capacitance. The metal oxide varistor (MOV) has a fast response ~ 1 ns and high peak power rating, but has a clamping voltage that tends to decrease with repeated transients. The avalanche diode has a fast response of ~ 1 ns and constant clamping voltage, but a low peak power rating and high shunt capacitance.

The metal oxide varistor is normally used on high energy circuits such as AC power, DC power or inductively switched loads. The standard arrangements for protecting single ended and balanced lines are shown in Figure 2.5.3-1. The avalanche diode, such as General Semiconductor's TransZorb, is used on low energy signal circuits such as ARINC, discrete and analog signals and 0-10 W DC power supplies. A low capacitance version of the avalanche diode must be used for signal frequencies above 1 MHz.



(a) Single ended circuit.

(b) Balanced circuit.

Figure 2.5.3-1 Transient protection for single ended and balanced circuits using varistors.

2.6 EMC PROBLEM INDICATORS

Excessive bandwidth - Use the slowest rise time possible and limit the bandwidth of all input and output lines.

Excessive wiring inductance - Minimize loop areas, especially on printed wiring boards.

Undesired antennas - If two metal surfaces, such as an LRU chassis and a cable shield, are not effectively bonded together at high frequency then a "dipole" antenna may exist.

Ungrounded metal - Metal surfaces that are electrically floating may cause a safety hazard and may increase capacitive and electromagnetic noise coupling.

Common mode current - The presence of common mode current, especially on intercon-necting cables, indicates a possible emission or susceptibility problem.

Pulse ringing - Usually indicates excessive wiring inductance.

Pulse rounding - Usually indicates excessive wiring or load capacitance.

Wiring length > wavelength/20 - Indicates that a controlled impedance and a matched termination are required.

Single point ground - This is not a proper grounding strategy for circuits operating at MHz and higher frequencies.

Signal load impedance >> 377 Ω - Suggests a sensitivity to both capacitively and magnetically coupled noise.

Unterminated signal lines - Can cause capacitive coupling if connected to a high impedance load.

Switch mode power supplies - Often produce conducted common mode and magnetically coupled noise.

2.7 GENERAL SUSCEPTIBILITY AND EMISSION REQUIREMENTS

In the past, radiated susceptibility tests were conducted at about 10 V/m up to 1 GHz. Current susceptibility test levels are dictated by Multiple Burst Lightning (MBL) and High Intensity Radio Frequency (HIRF) interference. Present radiated susceptibility tests are conducted at 200 V/m up to 18 GHz. Both the field strength and frequency range have increased by more than a factor of ten over past requirements.

	Radiated Susceptibility Test Levels
Past	~ 10 V/m up to 1 GHz
Present	~ 200 V/m up to 18 GHz

The detailed requirements and test procedures are found in D6-16050-4, Electromagnetic Interference Control Requirements. A brief listing of the types of tests follow in sections 2.7.1 and 2.7.2.

2.7.1 Types of Susceptibility Tests

1. Electrostatic discharge
2. Audio frequency susceptibility:
   a. AC and DC power line conducted susceptibility to 150 kHz.
   b. Electric field coupling to wiring to 15 kHz.
   c. Magnetic field coupling to wiring to 15 kHz.

   d. Magnetic field coupling to equipment at 400 Hz.
3. Radio frequency (RF) susceptibility:
   a. Conducted RF susceptibility, 10 kHz - 400 MHz (common mode current injection).
   b. Radiated RF susceptibility, 2 MHz to 18 GHz: 200 V/m amplitude modulated, 600 V/m pulsed.
4. Power line spike susceptibility.

2.7.2 Types of Emission Tests

1. Interference voltages on signal lines.
2. Short duration interference.
3. Audio frequency conducted emissions, 20 Hz to 150 kHz.
4. RF conducted emissions, 150 kHz to 30 MHz.
5. RF radiated emissions, 150 kHz to 6 GHz.

2.8 GLOSSARY

Balanced — A transmission line is balanced if both the signal and signal return conductors have the same impedance to ground.

Common-mode — The component of current on a transmission line that flows in one direction only and does not use any of the transmission line conductors as a return path.

Crosstalk — Crosstalk occurs when signals in one circuit unintentionally induce voltages or currents in a different circuit.

Decoupling capacitor — A capacitor placed between a DC voltage point and ground that is used to provide a local source of charge for devices with varying current requirements.

Differential-mode — The component of current on a two wire transmission line that flows in one direction on one wire and the opposite direction on the other wire.

EMC — Electromagnetic compatibility

EMI — Electromagnetic interference

ESD — Electrostatic discharge

HIRF — High Intensity Radiated Field

Return plane — A zero volt plane in a multilayer board (sometimes referred to as a ground plane).

Transient — A sudden change or spike in a voltage and/or current waveform.

3. PRINTED WIRING BOARDS

3.1 GENERAL WIRING BOARD DESIGN GUIDELINES

Avionic systems are unlikely to meet HIRF and other EMC requirements unless careful attention is paid to component selection, placement, and trace routing on every printed wiring board. Every active circuit on a printed wiring board is both an emitter and receiver of electromagnetic energy. The goal of the board designer is to design functional circuits that:

1. do not radiate excessively, and
2. are not adversely affected by the energy they receive.

Generally speaking, a circuit radiation source has two parts, a signal source and an "antenna" (see Figure 3.1-1). A circuit that is sensitive to external fields can be viewed as consisting of a "receiver" and an "antenna". In both cases, the "antenna" may be considered to consist of those parts of the circuit (or other circuits) that help to couple electromagnetic field energy to and from the circuit.

Radiation problems can often be eliminated by reducing the signal strength of the source whereas susceptibility problems are sometimes fixed by increasing the signal strength of the receiver circuit. These are conflicting requirements that must be resolved by weighing the likelihood of both types of failure. On the other hand, steps taken to minimize a circuit's ability to behave like an efficient "antenna", usually reduce the likelihood of both radiation and susceptibility problems.
Generally, long trace lengths and large loop areas make better "antennas". The following general guidelines are designed to ensure that excessive trace lengths and loop areas are avoided.

- ☐ Use surface mount components wherever possible.

- ☐ Route all signal return lines adjacent to corresponding signal lines.

High-speed, high-power, high-duty-cycle signals (e.g. clock lines) are more likely to present a radiation problem. High-impedance, high-gain components (e.g. operational amplifiers) are more likely to present a susceptibility problem. Power and I/O lines are most likely to be efficient "antennas" since they are not confined to the board.

- ☐ When laying out a printed wiring board, first priority should be given to using a solid, continuous return plane.

- ☐ Next, place DC power on non-overlapping planes.

- ☐ Then I/O lines should be routed (generally, I/O lines should be routed individually rather than left to the autorouter), followed by local or very short traces and high-speed and/or susceptible circuit traces. Low-speed circuits that are not particularly susceptible should be given the lowest priority.

- ☐ Clock oscillators are preferred to crystal/amplifier combinations. The oscillator housing should be connected to the return plane.

- ☐ Traces at the input of high-gain amplifiers are critical. The loop area formed by these traces must be kept to an absolute minimum.

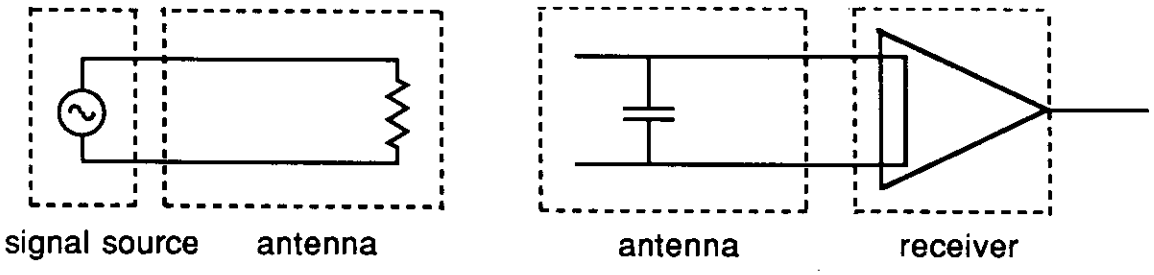


Figure 3.1-1 Circuits emit and receive EM fields.

3.1.1 Grounding Strategy

Proper grounding is perhaps the single most effective method for minimizing electromagnetic radiation and susceptibility problems. Fixing an EMC problem that is due to improper grounding with filters or shields can be frustrating and expensive. The importance of developing an effective grounding strategy at the beginning of the SRU design *and following it* cannot be over-emphasized.

The ground structure of an electronic system serves three primary purposes:

- safety ground
- reference ground
- return path for unbalanced signal and low-voltage power currents.

In order to provide an adequate safety ground, the ground structure must be able to conduct relatively large amounts of low-frequency current without developing a significant potential between any two grounded points. In this way, if a fault occurs and a high-voltage wire comes in contact with a grounded surface, the grounded surface will not become charged to a dangerous level. Safety ground is a non-current carrying ground by definition, but a safety ground structure must be capable of carrying currents high enough to blow a fuse or trip a breaker when a fault occurs.

Another purpose of the ground structure is to provide a common reference potential for the system. Referencing different circuits or subassemblies to the same potential helps to eliminate electromagnetic radiation and susceptibility problems. Unintentional potential differences can interfere with circuit operation, damage circuits, and cause EMI or safety problems. Reference grounds are not current carrying grounds by design, but they must be able to carry moderate amounts of "unintentional" current without developing a significant point-to-point potential over a wide frequency range. A low inductance is necessary to minimize ground voltage differences.

Unbalanced signal and low-voltage power sources often use part of the ground structure as a return path for signal currents. When this occurs, it is very important that the impedance of the grounding structure (at signal or power frequencies) be as low

as possible. Otherwise, the potential that develops across the ground impedance due to these intentional currents, could interfere with the safety and reference functions of the ground structure.

3.1.1.1 Grounding Strategy for LRUs

A diagram outlining the grounding strategy for cardfiles and LRUs is shown in Figure 3.1.1-1. The ground connection between the air frame and chassis is a safety ground, a reference ground, and a discrete signal return. Safety ground will normally be provided by a single heavy wire. Depending on the number of discrete signals and sensitivity of these signals to noise, additional grounds may be required.

The connection between the chassis and the backplane is a high-frequency reference ground and a discrete signal return. Cable shields are terminated on the chassis, but the signals on those cables are referenced through the backplane to the cards. It is important that a reasonably good high-frequency connection be made between the backplane ground and the chassis.

Cards are grounded to the backplane through connector pins. Ground pins in the connector serve as discrete signal returns and high-frequency reference grounds.

- ☐ The number of pins designated as 'ground' in a connector should exceed the number of power pins. Ideally, one ground pin should be provided for every signal pin. At the very least, the ratio of ground pins to non-ground pins should be no less than 1:8.

- ☐ All ground pins and any spare connector pins should provide a simple, short connection between the card ground plane and the backplane ground.

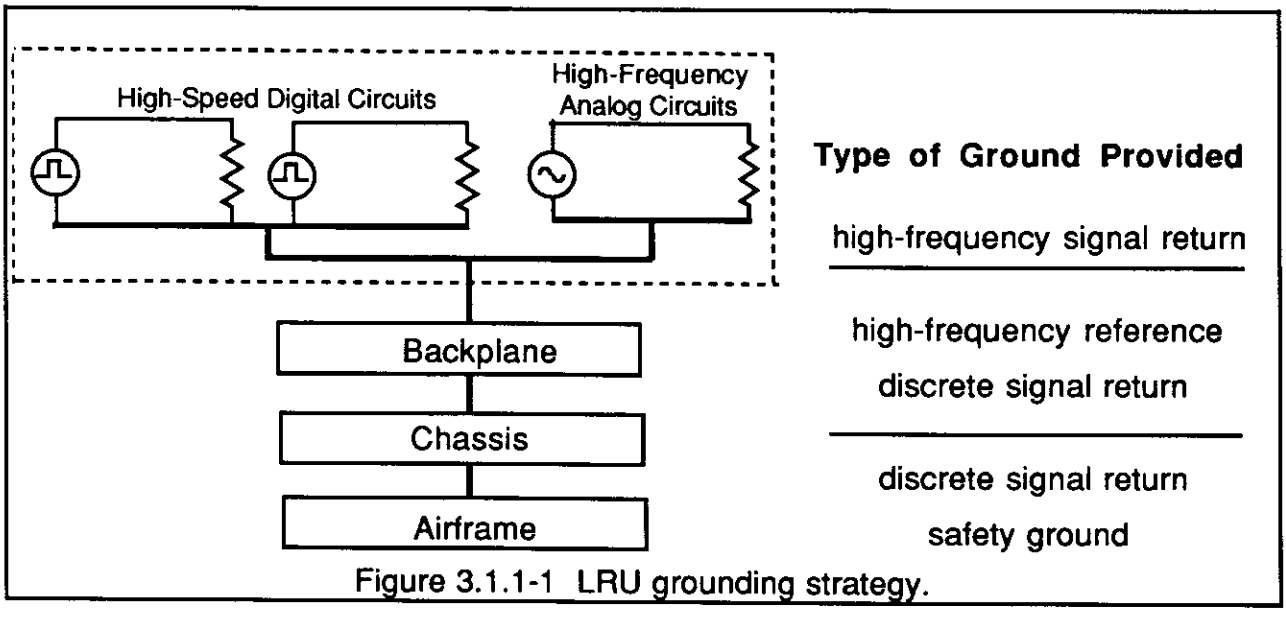


Figure 3.1.1-1 LRU grounding strategy.

3.1.1.2 Ground on SRUs

Every circuit card should have only one primary ground plane. This ground plane serves the following purposes:

- reference ground
- discrete signal return
- analog signal return
- digital signal return.

In order to effectively perform all of these functions simultaneously, it is very important to pay particular attention to the card layout. By carefully positioning circuits on the card, different areas of the ground plane can serve different purposes as shown in Figure 3.1.1-2.

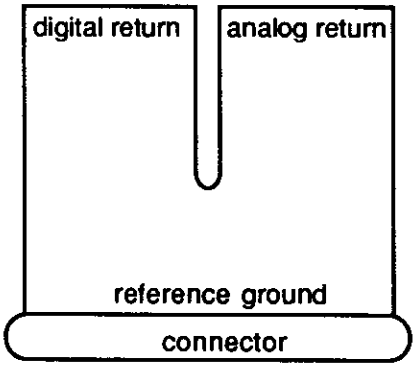


Figure 3.1.1-2 Groundplane with analog and digital regions.

- ☐ It is important to maintain a single continuous ground plane. Be sure that via holes or other discontinuities in the ground plane do not effectively isolate significant areas of the plane. Currents flowing in the ground plane must be able to flow unimpeded.

- ☐ If necessary, thin slots may be used to prevent digital return currents from interfering with analog signals, but the slots should always run mostly perpendicular to the connector and the distance between the connector and the slot should exceed the length of the slot.

- ☐ The region of ground near the connector is a high-frequency reference for currents that do not I/O the board. Care should be taken to ensure that high-frequency digital or analog signal return currents, that do not I/O the board, do not flow in this region of the ground plane.

- ☐ High-frequency currents that must I/O the board should be balanced, if possible, like ARINC-629.

- ☐ Unbalanced high-frequency currents that must I/O the board must remain within their own DC voltage region. For example, a digital signal operating from +5 VDC must not pass through a ±15 VDC or +28 VDC region.

3.1.2 Function Placement

Components and circuit modules must be grouped together based on whether they operate from ±15 VDC, +5 VDC or +28 VDC. The ±15 VDC is for analog (including audio) signals and the ±15 VDC portion of the ARINC level shifting circuits. The +28 VDC is for the DC power supply source and the +28 VDC portion of the discrete level shifting circuits. The +5 VDC is for digital signals only. Those portions of ARINC and discrete signal circuits that operate from +5 VDC are digital signals.

Since there are three basic DC supply sources, there are three distinctive signal types:

1. ±15 VDC powers "analog" signals;
2. +28 VDC powers "discrete" signals; and
3. +5 VDC powers "digital" signals.

A printed circuit board or backplane must be divided laterally into areas that require specific DC supply voltages. It is preferred that the three DC supplies (±15, +5, +28) be separated into non-overlapping areas as much as possible.

The ±15 VDC power planes must not overlap the +5 VDC power plane. In a multilayer configuration (see the 10 layer example in section 3.1.3) the ±15 VDC and +5 VDC are assigned the same two layers, thus preventing any overlap. This means that any circuit module that uses both ±15 VDC and +5 VDC must be positioned to straddle the boundary between these two areas. Analog to digital converters, the ARINC 629 serial interface module, and the ARINC 429 level shifting circuit are examples of circuits that must "straddle" the DC power boundaries.

- ☐ The DC power planes must not overlap one another.

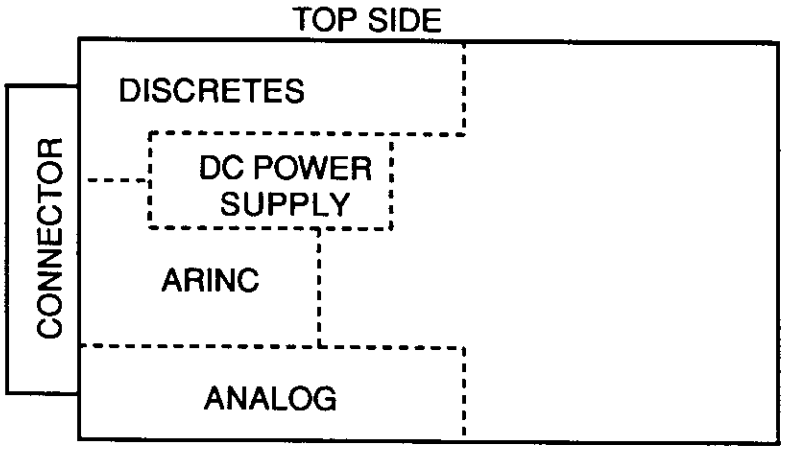
Figure 3.1.2-1 shows that function placement is dictated by the DC voltage used by that function. The DC power supply section is positioned toward the top of the board because of heat flow, yet in a position such that overlapping of the +28, ±15, and +5 VDC planes is eliminated. The ARINC circuit area includes two DC voltages because some ARINC components operate from the "analog" ±15 VDC supply and other components operate from the "digital" +5 VDC supply. For similar reasons, the discrete circuit area includes +28 VDC and +5 VDC in separate regions. The size and shape of the three DC voltage areas must be adjusted to accommodate the unique set of functions for each board design.

Figure 3.1.2-2 shows a second example of function segregation based on the DC voltage used by each circuit module. The connector is assumed to be located near the center of the board. The lateral segregation must meet these requirements:

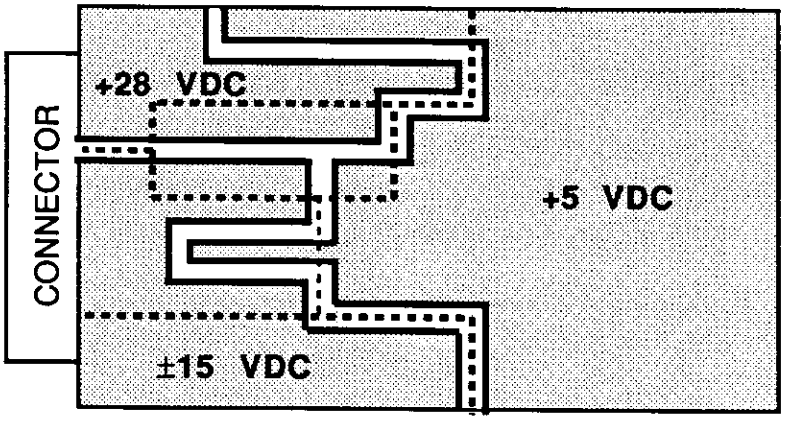
1. Provide direct access to the connector for analog, ARINC and discrete I/O. If I/O access is required to the digital (+5 VDC) area for test purposes, this access could be provided through the + 28 VDC area.

2. Provide an adequate boundary length between the DC voltage areas for interfacing circuits such as A/D converters (±15 VDC to +5 VDC), ARINC-429

level shifting (±15 VDC to +5 VDC) and discrete level shifting (+28 VDC to +5 VDC).



a) Lateral segregation by signal type.



b) Lateral segregation by DC voltage. Circuits requiring two DC voltages must straddle the gap between those areas.

Figure 3.1.2-1 Lateral segregation of circuits based on the DC voltage used.

General Function Placement Guidelines

- ☐ Keep all functional connectors on one end of the board. The test connectors can be on the opposite end of the board.
- ☐ Keep all high frequency circuits that do not I/O the board away from the connector.
- ☐ Keep high current and transient current (dI/dt) devices near their source of power.

- ☐ Avoid placing magnetic components close together. Maintain a separation at least twice the largest dimension of either component.

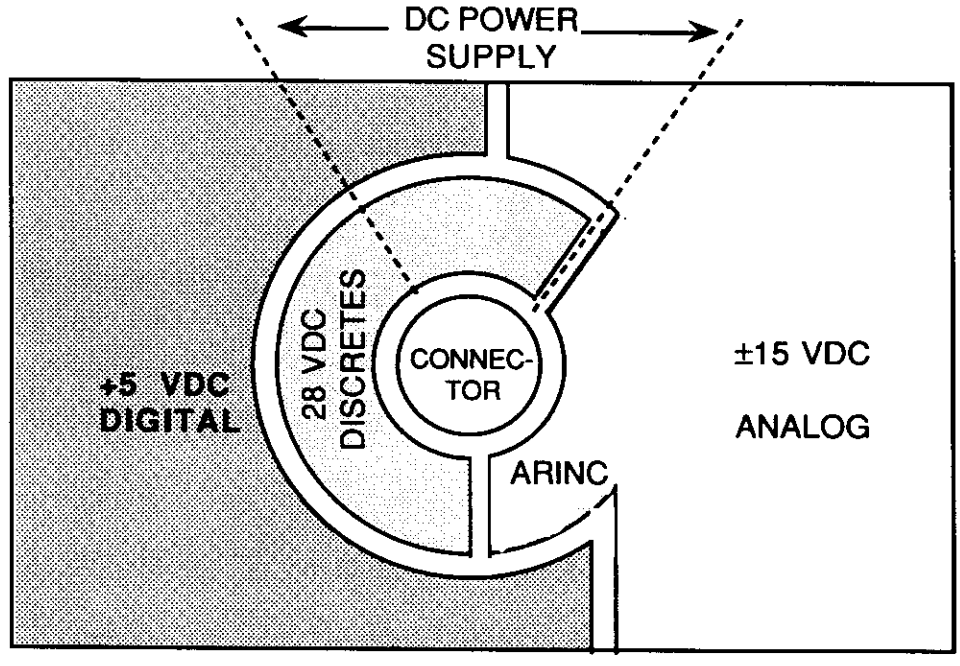


Figure 3.1.2-2 PCB lateral segregation of circuits based on the DC voltage used and a centrally mounted connector.

- ☐ Consider eliminating the power and return planes beneath inductors to reduce the shunting capacitance. If this is done, be certain that no traces cross this area because they would not have a low inductance return path.

- ☐ Centrally locate clock oscillators to minimize trace lengths.

- ☐ Do not route traces on the layer directly beneath circuit modules with fine pitched leads. Lead spacings less than about 30 mils do not allow sufficient space for a trace.

3.1.3 Standard Layering Configuration

On a circuit card it is necessary to classify signals based on the DC voltage required:

1. Analog uses ±15 VDC;
2. Digital uses +5 VDC; and
3. Discrete uses +28 VDC.

Some signals, such as ARINC 429 or 629, consist of a digital part powered by +5 VDC and an analog part powered by ±15 VDC. Even though the analog part of an ARINC

signal has only three distinct levels (high, low and null), since it is powered by ±15 VDC this signal should be considered as a high level, broad band analog signal.

Within each DC voltage area the signals must be separated based on frequency (or data rate) and amplitude (or level). The signal derivatives dV/dt or dI/dt conveniently combine both amplitude and frequency information. For sinusoids, the time derivative is equivalent to the product of signal frequency and amplitude. Signals whose derivatives or frequency x amplitude products differ by more than a factor of ten should be separated laterally from one another by at least 2 cm.

High rate or high frequency signals consists of clocks, microcore interconnections, data buses, ARINC, and analog RF signals. Low rate or low frequency signals consist of discrete signals that change state less than once a minute, analog audio signals and test signals.

- ☐ Use power and return planes for isolation between high rate and low rate signals.
- ☐ High rate signals should be between power and/or return planes.
- ☐ No signal layer should be more than two layers from a power or return plane.
- ☐ Minimize the use of gaps in the return plane.
- ☐ Cross-hatching with a grid size smaller than 1 mm is acceptable in place of a solid plane.
- ☐ The DC power planes should not overlap.

3.1.3.1 Standard 10 Layer Circuit Card

The standard layer assignments are shown in Figure 3.1.3.1-1.

- ☐ The RETURN PLANE uses layers 3 and 8. No signals may be routed on these two layers.
- ☐ The DC POWER uses layers 4 and 7. No signals may be routed on these two layers.
- ☐ If –15 VDC is not used, the +15 VDC should be assigned to layer 7 as well as layer 4.
- ☐ Low rate or low frequency signals use layers 1 and 2 or 9 and 10. These signals typically run in orthogonal directions on adjacent layers. A particularly short run high frequency signal may occasionally use one of these four layers.
- ☐ High rate or high frequency signals use layers 5 and 6. Signal directions on layer 5 are generally orthogonal to those on layer 6.

Layer Number	Active Component Side
1 2	} Low rate or low frequency signals
3 4	RETURN PLANE DC POWER PLANES
5 6	} High rate or high frequency signals
7 8	DC POWER PLANES RETURN PLANE
9 10	} Low rate or low frequency signals
	Passive Surface Mount Component Side

Figure 3.1.3.1-1 Standard assignment for a 10 layer circuit card.

The same basic layer assignments are used within each of the three laterally segregated signal areas -- digital, analog and discrete -- as shown in Figure 3.1.3.1-2.

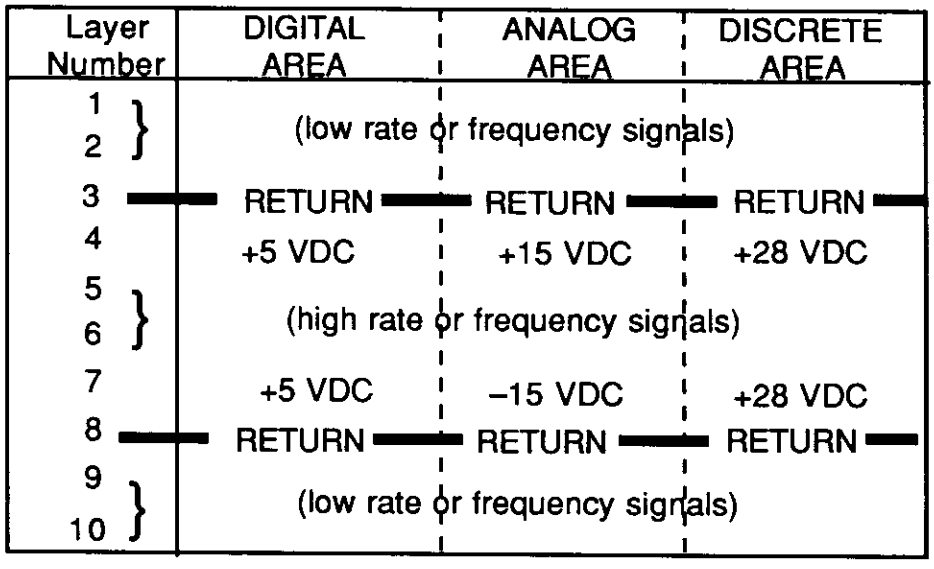
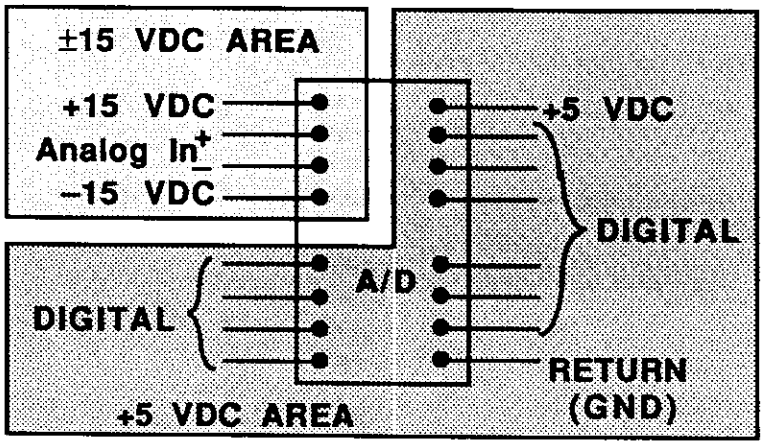


Figure 3.1.3.1-2 Layer assignments within the digital, analog and discrete signal areas.

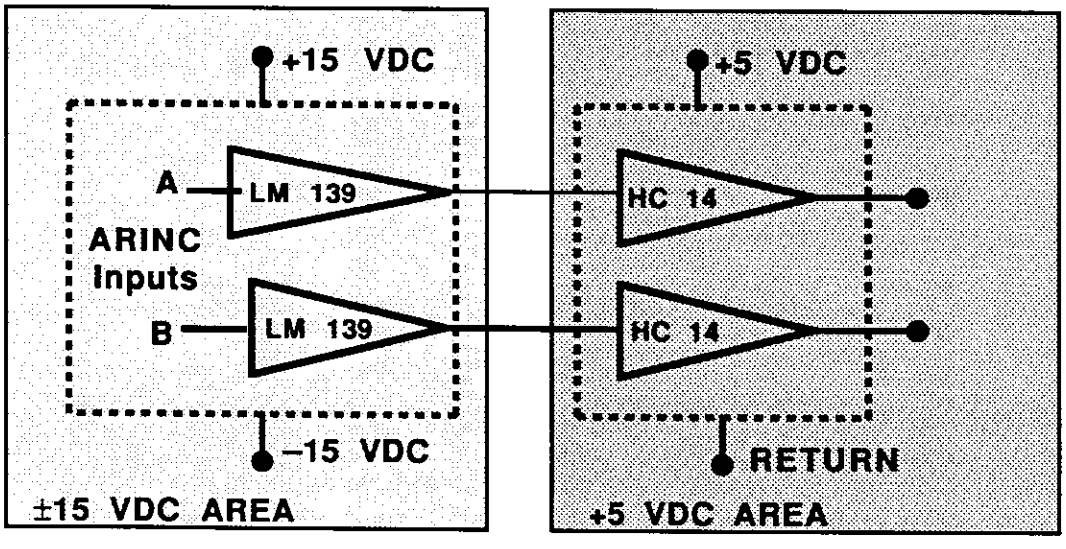
Figure 3.1.3.1-3 shows two examples of how circuits that must interconnect between two different DC voltages can be laterally segregated into separate non-overlapping DC voltage areas. The shape of the boundary between the two DC

voltage areas is dictated in the case of a circuit module by the pin assignments or in the case of a circuit made of individual components by the placement of the components. Figure 3.1.3.1-4 shows how the poor pin assignments for the ARINC 629 Serial Interface Module can complicate the lateral segregation of the ±15 VDC and +5 VDC areas.



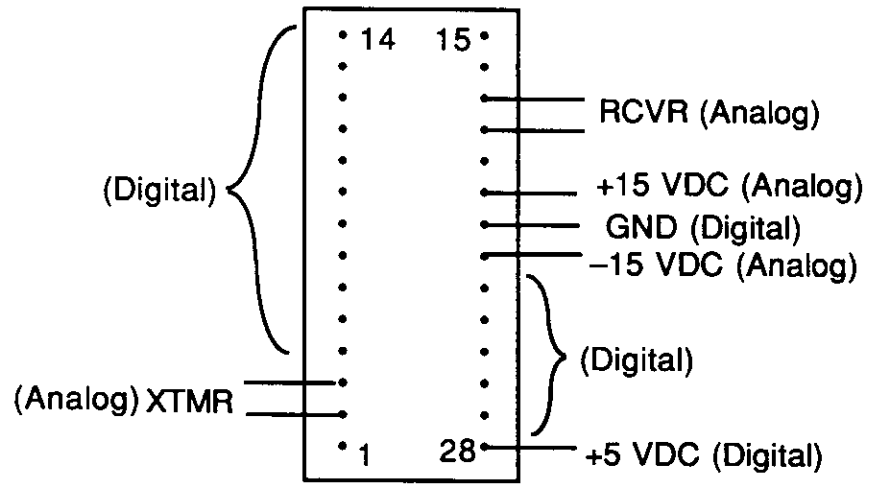
(a) Lateral segregation of the ±15 VDC and +5 VDC areas in the region near an anlog to digital converter.

A gap exists in the DC power plane,
but there is no gap in the return plane.

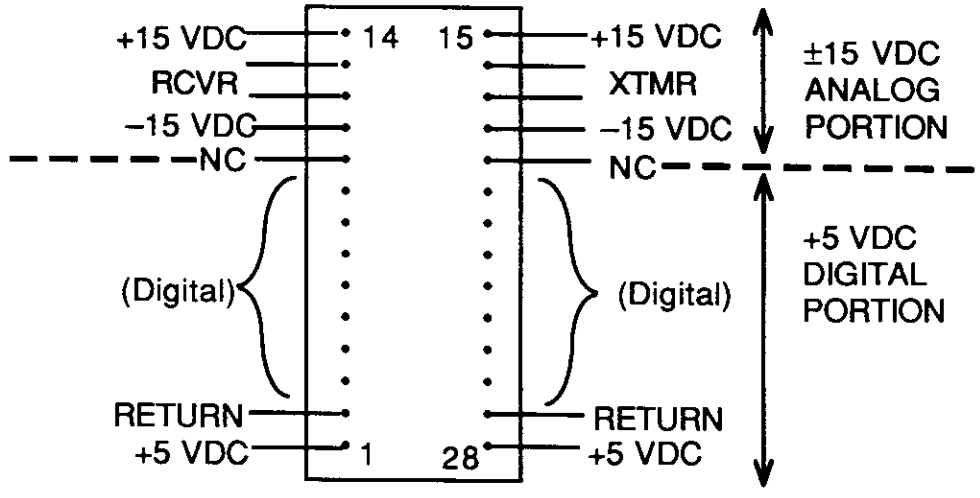


(b) A simplified diagram of the ARINC 429 receiver level shifting circuit showing the clear division between the ±15 VDC (analog) and +5 VDC (digital) portions.

Figure 3.1.3.1-3 Examples of circuits that must straddle two DC voltage areas.



(a) The actual pin assignments for the ARINC 629 Serial Interface Module showing the poor lateral segregation of analog and digital functions. How can the ±15 VDC and +5 VDC areas be separated?



(b) A better segregation of the ARINC 629 SIM pins into analog and digital functions.

Figure 3.1.3.1-4 Poor circuit module pin assignments can greatly complicate the lateral segregation of DC voltage areas.

3.1.4 Trace layout

As Section 3.1 pointed out, circuit board traces are often the "antennas" that facilitate the coupling between currents and fields. There are four basic concepts that form the basis for an effective trace layout.

1. Design the traces to be very inefficient "antennas."
2. Keep "transmitting" traces away from "receiving" traces.

3. Don't allow the trace layout to violate the grounding strategy discussed in Section 3.1.1.
4. Assign the highest routing priority to the most critical traces.

The following guidelines support one or more of these concepts. These guidelines apply to both backplanes and circuit cards. Since the return plane is the highest priority trace, guidelines pertaining to the return plane are listed first.

- ☐ Avoid placing gaps in the return planes. If a gap is absolutely required to keep digital noise from interfering with analog circuits, place it far from the connector and minimize its length.

- ☐ Return planes must be solid in the region near the connector.

- ☐ Don't permit via pads to overlap and form a gap or slit in the return plane.

- ☐ When there is more than one return plane, all via connections to return should connect to both planes.

Power planes and traces are the second priority. The following guidelines pertain to power routing.

- ☐ Confine power to dedicated planes. Keep signal and return traces off the power layers and avoid routing power traces on non-power layers.

- ☐ When there are multiple voltages on the same power layer, maintain a low-inductance (i.e. wide trace) path from all points on the plane to the power supply.

The following guidelines apply to all signal traces. Remember to assign the highest priority to I/O traces, high-frequency traces, and traces in susceptible circuits.

- ☐ Wider traces have lower inductance and are usually preferred for high-speed signals.

- ☐ The spacing between any trace and the board edge should be greater than the height of the trace above the return plane. (If all the traces are routed within the defined board area, this is taken care of automatically.)

- ☐ No traces should be allowed to cross a gap in the return plane except balanced A/D connections.

- ☐ Keep the highest speed traces short and on one layer. When there is a tradeoff between minimizing the length of a trace and keeping it on one layer, priority should be given to minimizing the length.

- ☐ Whenever there is a tradeoff between minimizing signal path loop area or trace length, minimize the loop area.

- ☐ If a "guard trace" is used, it must be connected to the return plane on both ends.

- ☐ The highest frequency signal lines should be kept inside the outermost power or return planes.

- ☐ If a signal path is greater than $\lambda/20$ at the *highest frequency of concern* (see section 2.1.5), it should be treated as a transmission line. A constant characteristic impedance should be maintained and the load impedance should be matched to the line.

- ☐ Arinc line pairs should always be balanced with uniform characteristic impedance.

- ☐ Balanced line pairs should be routed together on the same layer maintaining a constant separation.

- ☐ Balanced line pairs should always be routed on a layer adjacent to power or return planes although it is permissible to jump from one layer to another even if the two layers are adjacent to different power or return planes.

- ☐ It is best to laterally segregate traces to minimize crosstalk.

- ☐ Routing traces on adjacent layers at right angles to each other permits more efficient routing and minimizes crosstalk.

- ☐ Fill empty areas on a layer with metal either by widening traces or adding a patch of metal connected to the return plane. Do not permit floating areas of metal to exist. Tie unused metal areas to the return plane.

- ☐ Try to avoid running signal traces in the region directly beneath the power supply.

3.1.5 I/O Pin Assignment

A key point to keep in mind when making I/O pin assignments is that generally the card layout should dictate how pins are assigned. It is not usually a good idea to alter the card layout just to match a preconceived connector pin assignment. Therefore,

- ☐ Maintain flexibility with I/O pin assignments. Don't lock in on a pin assignment until the basic card layout has been determined.

- ☐ Coordinate pin assignments with function locations on the card.

- ☐ If the connection is between two cards (e.g. a SRU and a backplane), the layout of the two cards must be coordinated. Pins must be assigned with the layout of both cards in mind.

Once the general functional placement of power and signal pins has been determined, the following guidelines can be applied to obtain the best possible connector pin assignment.

- ☐ Locate signal returns on pins closest to their corresponding signal pins.
- ☐ Separate high-level output and low-level input pins.
- ☐ Return or power pins can be used to help isolate signals.
- ☐ Any extra pins in the connector should be used for return or DC power.

Sometimes the pin assignments have been fixed and they are not subject to change by the circuit designer. In these situations,

- ☐ Consider I/O pin assignments when routing power planes and placing components.
- ☐ Use power and return planes to isolate lines that need isolation but can't be separated laterally.

3.1.6 I/O Filtering and Surge Protection

3.1.6.1 Filtering

I/O lines often require filtering in order to keep external noise currents from getting into a system or to keep internal noise from getting out. Referring to the "antenna" analogy of Section 3.1, I/O lines are often a link between the most efficient antennas (i.e. the external cables) and the potential "sources" and "receivers" in the LRU. Even relatively insensitive, low-frequency I/O lines (e.g. discretes) may require filtering, since these lines may inadvertently couple to sensitive or high-speed circuits in the system.

- ☐ Position all I/O filters within the connector or as close to the connector as possible. Don't allow noise to bypass the filter components by coupling to unrelated traces between the filter and the connector.

EMC filters are generally first or second-order, low-pass filters (often with built-in loss). Higher-order filters, bandpass filters, and notch filters may be used in special circumstances, but in general they should be avoided. Filter components may contribute to unwanted coupling or transient oscillations (ringing). Therefore, a basic rule of EMC filtering is,

- ☐ Keep the filter simple. Use a single capacitor to filter high impedance (> 1 kΩ) circuits or a ferrite bead to filter low impedance (< 100 Ω) circuits.

Sometimes, a single capacitor may resonate with the trace inductance making it necessary to add additional resistance. A resistor can be placed in the signal path or it can be added in series with the capacitor as shown in Figure 3.1.6.1-1. The choice

will depend on the desired frequency response. Ferrites have a significant amount of loss at high frequencies and usually do not require additional resistance.

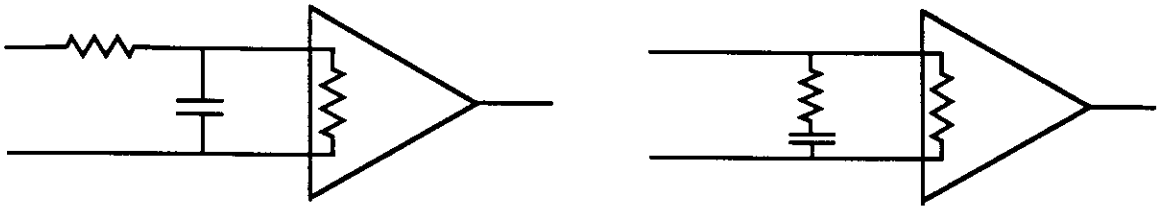


Figure 3.1.6.1-1 Two possible RC filter configurations.

- Pi or T-filters (Figure 3.1.6.1-2) can be used when the impedance of the circuit is unknown or uncontrolled.

- Use ferrites, rather than inductors when constructing a Pi or T-filter. Ferrites have a more stable high frequency impedance.

Sometimes it may not be clear during a product's design stage whether or not filtering is required.

- It is a good idea to provide pads and vias for filter components even if it is not certain that they will be needed. Filters cannot be readily added to a surface mount card that doesn't have a place for them. On the other hand, it is easy to bypass them during testing and remove them in a later design iteration if they are not needed.

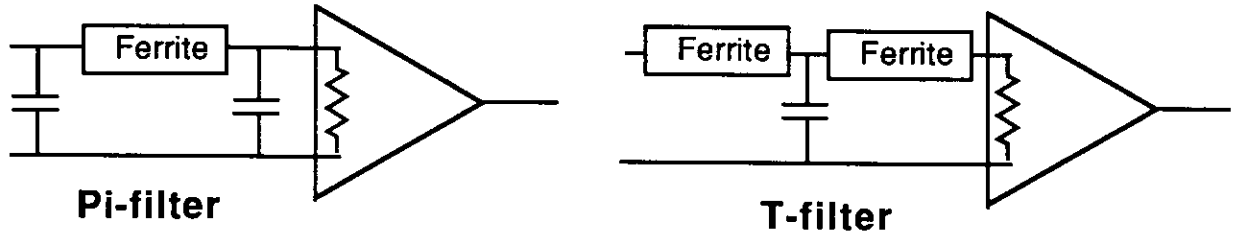


Figure 3.1.6.1-2 Pi and T-filters.

3.1.6.2 Surge Protection

Filtering alone may not protect a circuit from large transients that may be coupled to the I/O lines due to lightning, electrostatic discharge (ESD), or power surges. Surge protection is accomplished using devices that limit the maximum voltage that can be dropped across them. For example, Figure 3.1.6.2-1 illustrates how a pair of diodes might be used to limit an amplifier's input voltage.

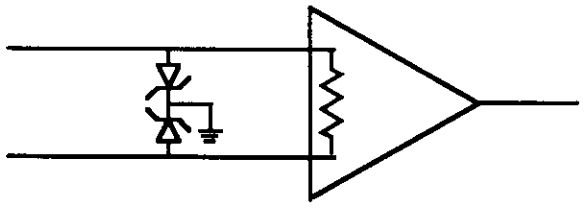


Figure 3.1.6.2-1 Using diodes for surge protection.

Diodes, metal oxide varistors, and gas-discharge tubes can be used to provide different levels of surge protection. Table 3.1.6.2-1 lists properties of each of these surge protection devices.

3.1.7 DC Power Bypassing

The purpose of bypass (decoupling) capacitors on a PCB is to provide the switching currents when integrated circuit devices change state.

- ☐ All bypass capacitors will be surface mount devices.
- ☐ Place all bypass capacitors directly beneath and on the opposite side of the board from the integrated circuit being decoupled. Orient the surface mounted capacitor such that the solder pads are not shadowed by the capacitor body as the PCB is passed through the solder process.

Type	Polarity	Failure Mode	Condition when activated	Response Time (sec)	Capacitance (farads)	Voltage Range
Diodes or Transorbs	unipolar	short	clamped	10^{-9}	10^{-7} - 10^{-10}	4 - 200
Metal Oxide Varistors	bipolar	degraded then short	clamped	10^{-9}	10^{-8} - 10^{-10}	33 - 1400
Gas Discharge	bipolar	open	short	10^{-6}	10^{-11} - 10^{-12}	100 - 10^{4}

Table 3.1.6.2-1: Comparison of transient protection devices.

- ☐ Use the widest, shortest traces possible between the capacitor mounting pads and the vias to the power and return planes.
- ☐ For 5 VDC and ±15 VDC operation use the following SMD ceramic chip capacitors:

CAPACITOR	BOEING P/N
0.001 μF	900 - 14050 - 10295
0.1μF	900 - 14051 - 10495

- ☐ Use the bypassing recommended in Table 3.1.7-1.

IC Family (Type)	SOIC Size (Pins)	Bypassing Required
HCMOS, ACT or TTL	16 - 20	One 0.001 µF capacitor at each device plus a centrally located 0.1µF capacitor for each group of 15 0.001 µF capacitors.
HCMOS, ACT or TTL	24 - 40	One 0.001 µF and one 0.1 µF capacitor at each device.
µP, Static RAM, EEPROM NOURAM, EPLD PALs		One 0.001 µF and one 0.1 µF capacitor at each device.
ASICs or Discretes	40	One 0.001 µF capacitor for each power input pin and one centrally located 0.1 µF capacitor.

Table 3.1.7-1 Bypassing requirements for specific circuits.

3.1.8 AC Power Inputs

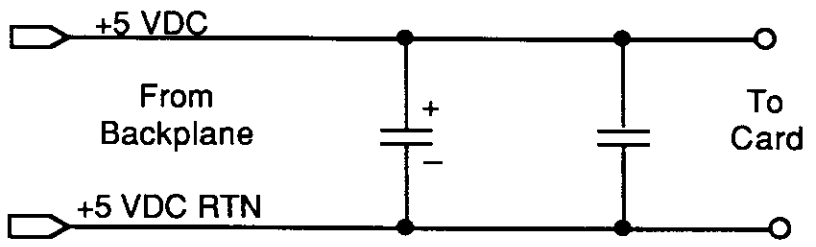
- ☐ All AC power inputs must be transformer coupled, except for those inputs that are only passed through or switched by the SRU.
- ☐ If a shielded transformer is used, the shield must be connected by a separate trace to the SRU enclosure.
- ☐ The AC power neutral must be kept isolated from the PCB return plane.

3.2 SPECIFIC WIRING BOARD DESIGN GUIDELINES

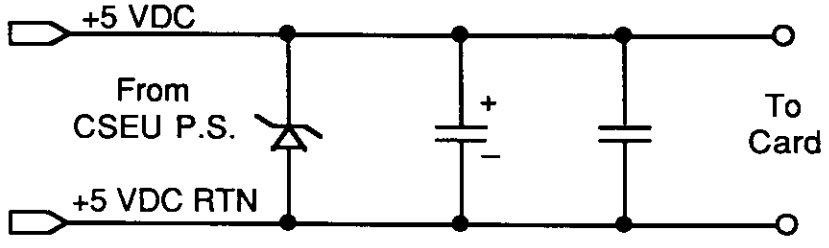
3.2.1 DC Power Supplies

3.2.1.1 Standard DC Power Input Filters

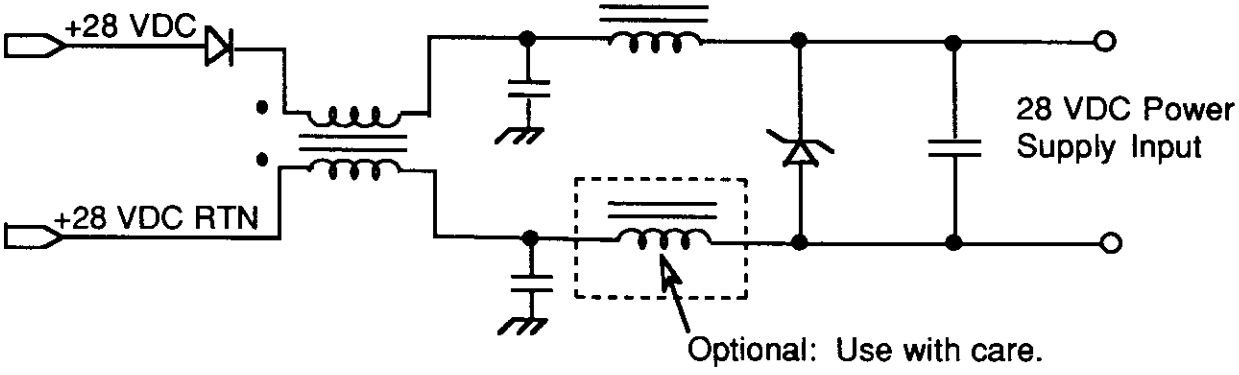
Figure 3.2.1.1-1 shows the standard filter configurations for +5 VDC and +28 VDC inputs to circuit cards.



(a) +5 VDC intrabox connection via backplane.



(b) +5 VDC interbox connection via airplane wiring.



(c) + 28 VDC input.

Figure 3.2.1.1-1 The standard filter configurations for +5 VDC and +28 VDC inputs to circuit cards.

3.2.2 AC Power Supplies

3.2.2.1 Standard 115 VAC Input Filter

Figure 3.2.2.1-1 shows the standard filter configuration for 115 VAC inputs to circuit cards.

3.2.3 Discretes

☐ Use the SIP for transient protection and level shifting.

- ☐ Position the SIP across the boundary between the 28 VDC and 5 VDC power planes.

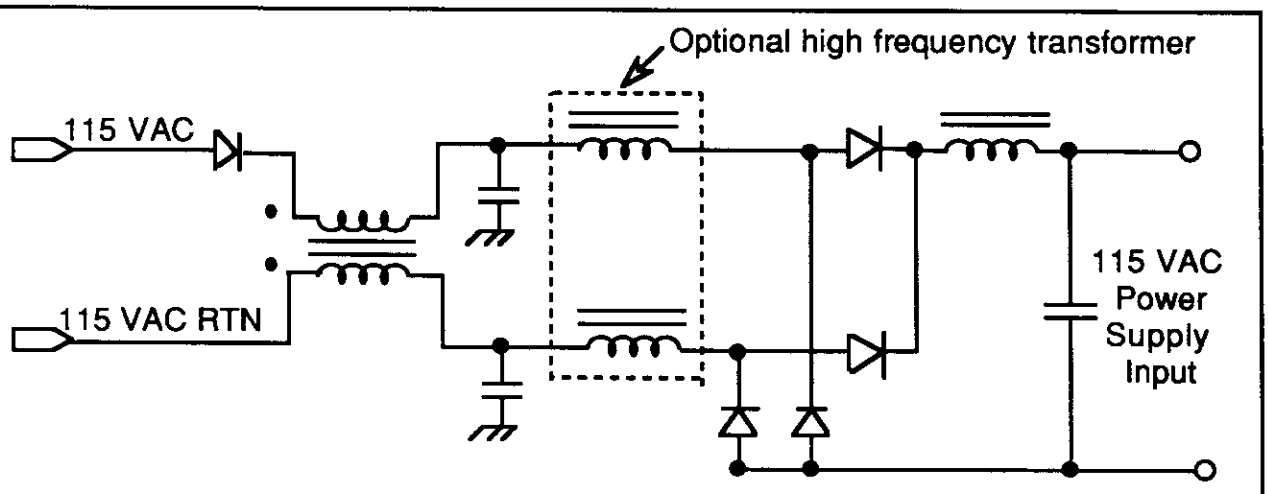


Figure 3.2.2.1-1 The standard filter configuration for 115 VAC inputs to circuit cards.

3.2.4 Analog Circuit Modules

3.2.5 Digital Circuit Modules

3.2.6 Balanced Signals

3.2.6.1 ARINC - 429

- ☐ Because the level shifting circuit consists of discrete components, the layout is very critical in order to minimize loop areas.
- ☐ The level shifting circuit must be divided into two sections, one operating from ±15 VDC and the other from +5 VDC.
- ☐ Route the transmit and receive signals as a balanced pair between power or return planes.

3.2.6.2 ARINC - 629

- ☐ Place the Serial Interface Module (SIM) across the boundary between the ±15 VDC and +5 VDC regions.
- ☐ Route the transmit and receive signals as a balanced pair between power or return planes.

3.2.6.3 RS - 485

3.2.7 Test Functions

4.0 METAL ENCLOSURES

4.1 GENERAL METAL ENCLOSURE DESIGN GUIDELINES

Metal enclosures contribute to the electromagnetic compatibility of an LRU in two ways:

1. A metal enclosure provides a common reference potential for the entire LRU.

2. Metal enclosures can shield sensitive circuits from external electromagnetic fields.

The importance of the first item above cannot be overstated. In order to couple electromagnetic energy into or out of a circuit, certain elements of a system must function as an "antenna." Every antenna requires at least two significant conducting surfaces that are at different potentials as illustrated in Figure 4.1-1. A metal enclosure is a convenient means of ensuring that all conductive surfaces of significance are held to the same potential. By eliminating the most efficient antennas in a system, many radiation and susceptibility problems can be avoided.
In order to ensure that a metal enclosure can provide an adequate reference, it is important to observe the following guidelines:

Relatively efficient antenna

Relatively inefficient antenna
(bulk of conductor is held to one potential)

Figure 4.1-1 There are two halves to every antenna.

☐ Under no circumstances, should an enclosure be used as a power or signal return path.

☐ High-speed signal lines should be routed close to their own return and kept away from the enclosure surfaces.

☐ The enclosure must provide a low RF impedance between any two points on its surface.

Cracks, seams, and apertures in the enclosure impede normal current flow. This not only increases the RF impedance, but it also reduces the shielding effectiveness of the enclosure. A metal enclosure shields circuits from external fields by reflecting and absorbing electromagnetic energy. In order to provide effective shielding, it is important that RF currents are able to flow freely on the surface of the enclosure.

4.1.1 Enclosure Grounding

Ideally the enclosures of all LRU's would be bonded to the airframe with a good, low-impedance, RF connection. This would prevent the LRU from obtaining a potential significantly different from that of the nearby airframe.

Since it is not always possible to achieve a low-impedance RF bond between the airframe and the LRU enclosure, cables running between the LRU and points on the airframe may be relatively efficient RF antennas. For this reason, we must assume that a significant amount of common-mode current will exist on the I/O cables (see Figure 4.1.1-1).

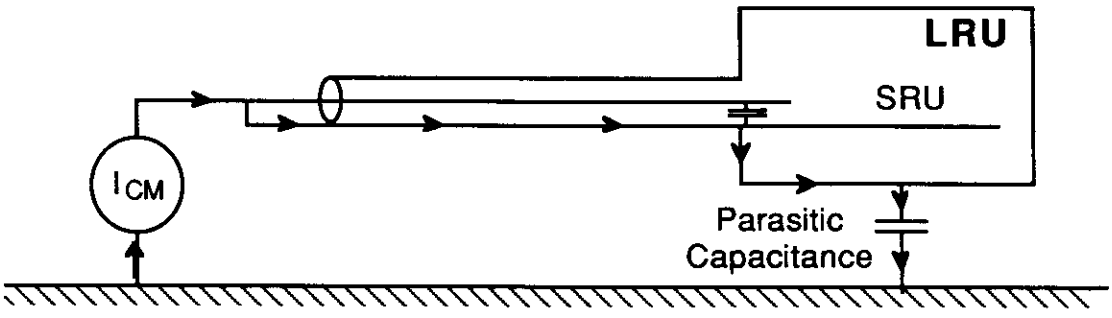


Figure 4.1.1-1 Shunt common mode currents to the enclosure.

In order to prevent common mode current on the cables from flowing through the interior of an LRU,

- ☐ All cable shields should be bonded to the exterior of the LRU at the connector.
- ☐ Backplanes or cards attached directly to an I/O cable should have their ground planes bonded to the enclosure at the connector.
- ☐ All connectors should be located on one side of the LRU.

The greater the number of I/O cables, the more important it is to provide a low-impedance connection between the enclosure and the airframe. For this reason,

- ☐ Cardfiles should be bolted to the airframe at multiple points and care should be taken to ensure that a low-impedance bond has been attained.

4.1.2 Apertures

Apertures in a metal enclosure impede the flow of high frequency currents and allow fields to penetrate through the enclosure. Although apertures are a necessity in most LRU's for cooling, I/O, or display purposes, it is desirable from an EMC standpoint to keep the number and size of apertures to a minimum. Where apertures are unavoidable, the following guidelines apply.

- ☐ Minimize the maximum linear dimension of an aperture. Round or square holes are better than slots because they have the smallest maximum linear dimension for a given area.

- ☐ When a relatively large aperture area is required for cooling, use a screen or mesh behind the apertures to help surface currents flow through the area as if the aperture wasn't there.

- ☐ Position the apertures to minimize the impedance to the flow of surface currents (see Figure 4.1.2-1).

- ☐ Keep apertures away from I/O and ground connections and other areas where surface current densities on the enclosure are likely to be highest.

Figure 4.1.2-1 Apertures should not impede current flow.

4.1.3 Seams

When two parts of an enclosure are fastened together, perfect electrical contact is usually not achieved over the entire length of the seam. Current flow is diverted in the vicinity of the seam and, in effect, the seam may behave like a long thin aperture. Because their maximum linear dimension is large, seams usually present a much more significant breach in the enclosure's shielding effectiveness than other apertures.

There are several reasons that two metal surfaces in physical contact with one another may not make good electrical contact (see Figure 4.1.3-1).

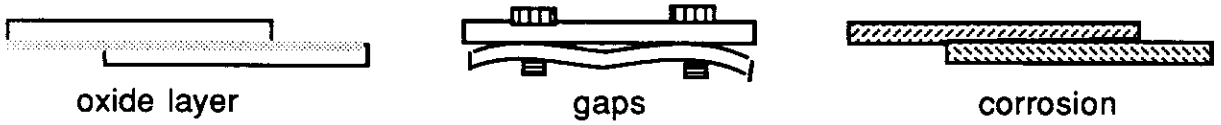


Figure 4.1.3-1 Electrical gaps in metal-to-metal seams.

- ☐ Oxides or other non-conductive contaminant may be present on the surface of the conductors.

- ☐ The conductors may not be perfectly flat.

- A galvanic reaction caused by current flowing between dissimilar metals may cause the interface to become corroded and nonconductive over time.

The following guidelines are meant to ensure that good electrical contact is maintained across enclosure seams.

- Conductive gaskets may be used to electrically seal gaps in seams due to non-flat surfaces. Some conductive gaskets have metal fibers designed to pierce through thin layers of oxide or other surface contaminants.

- Copper finger stock serves the same function as conductive gaskets. Finger stock is preferred when the seam connection is made and unmade often (e.g. door seams).

- When conductive gaskets are not used, it is a good idea to provide a significant amount of overlap as shown in Figure 4.1.3-2. This provides a good RF connection due to the capacitive coupling between the conductors even if perfect conductive coupling is not achieved.

Figure 4.1.3-2 Overlapping seams.

- It is best to avoid using different metals in the enclosure design. However, whenever two dissimilar metals are joined, care should be taken to ensure that they are close to each other in the galvanic series (Table 4.1.3-1). The farther apart metals are in the galvanic series, the greater the potential for corrosion formation at the interface.

Anodic End - most easily corroded					
Group	1.	Magnesium	**Group**	13.	Nickel (active)
I	2.	Zinc	**IV**	14.	Brass
	3.	Galvanized Steel		15.	Copper
Group	4.	Aluminum		16.	Copper-Nickel alloy
II	5.	Cadmium		17.	Monel
	6.	Galvanized Iron		18.	Silver solder
Group	7.	Carbon Steel		19.	Nickel (passive)
III	8.	Iron		20.	Stainless steel (passive)
	9.	Stainless Steel (active)	**Group**	21	Silver
	10.	Lead-Tin Solder	**V**	22.	Graphite
	11.	Lead		23.	Gold
	12.	Tin		24.	Platinum
			Cathodic End - least corroded		

Table 4.1.3-1 Galvanic series.

4.1.4 Plastic Enclosures

The following design guidelines apply to enclosures made of plastic materials.

- ☐ Conductive plastics (carbon or fiber filled) should be avoided. They do not have adequate surface conductivity.
- ☐ Conductive paint should also be avoided, because it is easily rubbed off. This makes it ineffective as a shielding material and the conductive flakes or powder can adversely affect circuit operation.
- ☐ Vacuum deposition techniques suffer from the same flaking problems as conductive paints.
- ☐ When plastic enclosures are used, they should be plated (preferably with an electroless nickel process).

4.1.5 Electromagnetically Sealed Enclosures

In order to take full advantage of the shielding that metal enclosures can provide, it is essential that careful attention be paid to each and every I/O cable. As Figure 4.1.5-1 illustrates, just one unfiltered wire penetrating the enclosure can reduce the shielding effectiveness to 0 dB or less. A sealed enclosure must filter every I/O wire. Preferably the filtering is done at the connector so that noise currents on the wire can be shunted to the external surface of the enclosure.

- ☐ All unshielded cables must be filtered at the point where they enter an electromagnetically sealed enclosure.
- ☐ Long shielded cables may not require filtering, since any common mode currents within the cable may be sufficiently attenuated by the time they reach the enclosure.

Power connections tend to have particularly high noise currents and often they require substantial filtering. Components of the filter are often large due to their voltage and current handling requirements. One common method of providing for large filter components without compromising the effectiveness of the sealed box is to provide a secondary enclosure exclusively for the filter components as shown in Figure 4.1.5-2.

4.2 SPECIFIC METAL ENCLOSURE DESIGN GUIDELINES

4.2.1 Cardfiles

- ☐ Cardfiles are sealed enclosures. Careful attention must be paid to the apertures and seams and every wire penetrating the enclosure must be filtered at the connector.

- ☐ The back planes in a cardfile must be bonded to the cardfile enclosure at points at least once every 4 inches around their perimeter.
- ☐ The cardfile chassis must be bolted to the airframe at multiple points and care should be taken to ensure that a low-impedance bond has been obtained.

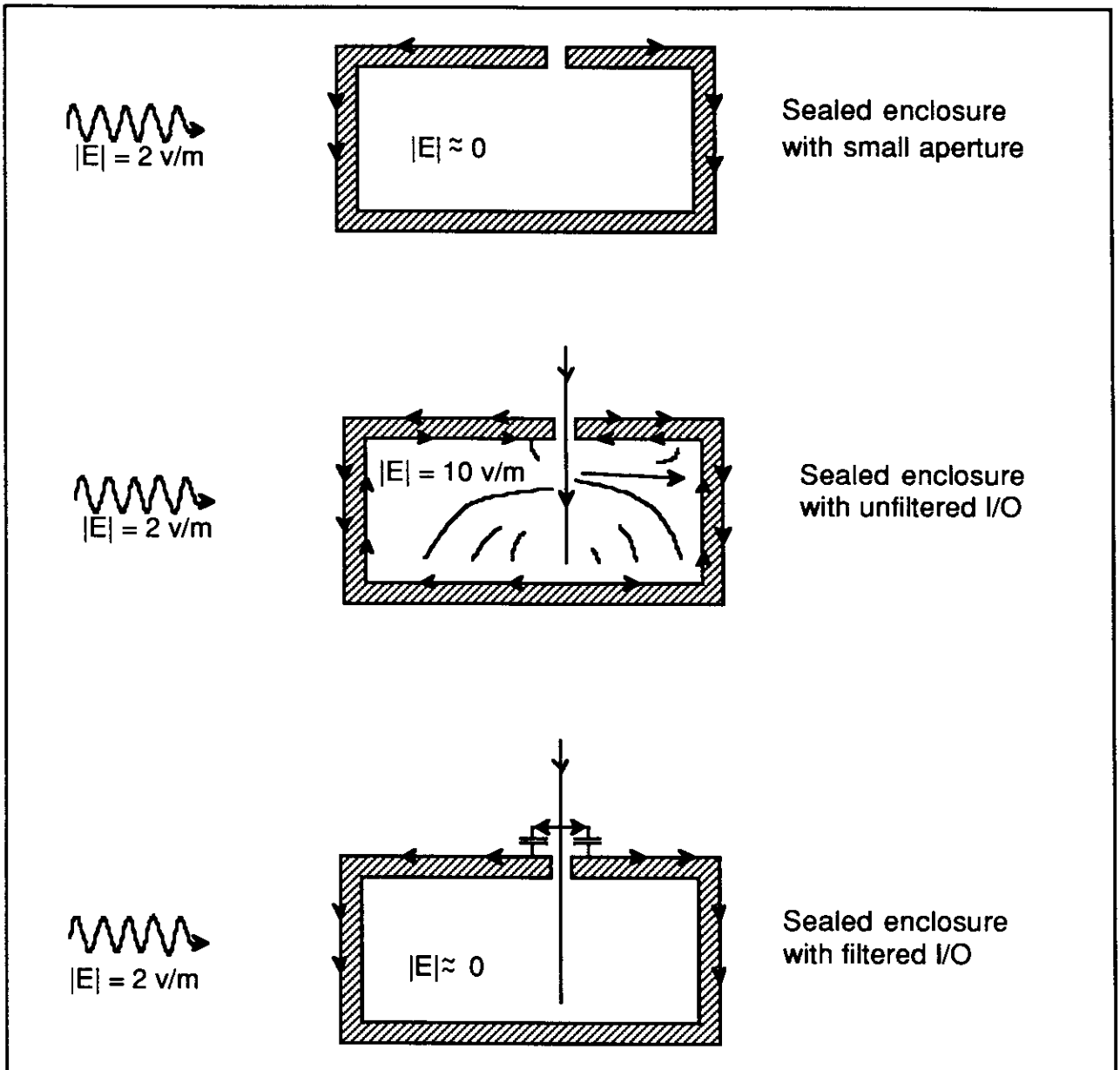


Figure 4.1.5-1 Wires penetrating sealed enclosures.

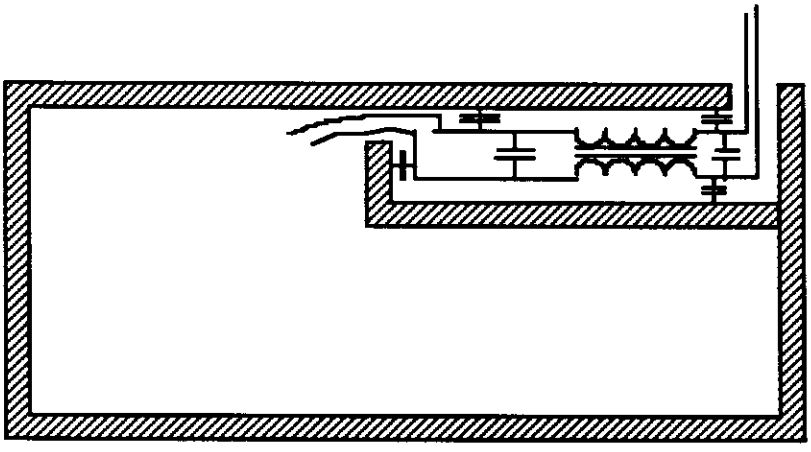


Figure 4.1.5-2 Power filtering in a sealed enclosure.

5. CABLING

This chapter is concerned with cabling outside of metal enclosures, such as between LRUs or between an LRU and a sensor, relay or actuator. All cabling is assumed to be inside the pressure vessel (PV) unless specifically stated to be outside the PV.

5.1 GENERAL CABLING DESIGN GUIDELINES

- ☐ Cabling must be considered as a possible wire (electric field) or loop (magnetic field) transmitting or receiving antenna.

- ☐ Control noise by filtering at the ends of a cable rather than using a cable with additional wires or shielding. Filtering is less weight and cost than shielding.

- ☐ Group cables by compatible signal and power types, such as:
  AC power, DC power and discrete signals;
  Balanced digital signals (ARINC 429/629, RS 485);
  Analog, audio and RF signals.

- ☐ Outside the pressure vessel (PV), all cabling (signal and power) must be a twisted pair, shielded and ungrounded. The shield must make a 360° contact to the pressure vessel connector. Any signals or power that use structure return inside the PV must be grounded at the PV connector.

- ☐ When magnetic protection is critical use a twisted pair for each signal current with a minimum of one twist per inch for wires smaller than #18 AWG.

5.1.1 Function and Connection of Cable Shields

Below 1 MHz the primary function of a cable shield is to reduce capacitive noise coupling. Above 10 MHz the primary function is to reduce electromagnetic emission or susceptibility. The shield transfer impedance can be used to compare the effectiveness of various shield types. The lower the transfer impedance the more effective the shield.

- ☐ Lightning dictates the connection of shields outside the PV and HIRF dictates the connection inside the PV. Outside the PV a cable shield must be connected only at the PV connector to avoid conducted lightning transients.

- ☐ Braid, braid plus foil and double braid shields are acceptable. Metallized polyester film shields or foil shields without a drain wire can not be used. Foil shields with a drain wire are not acceptable for electromagnetic (MHz) shielding but can be used for capacitive (kHz) shielding.

- ☐ The connection of the shield is as important as the type of shield material. In general, a 360° connection of the shield is best and should be used whenever possible.

- ☐ Shielding intended to reduce capacitively coupled noise at frequencies below 1 MHz can use a pigtail connection less than 2 inches long. These shields can be spliced together. The capacitive shield should be grounded on the same end of the cable where the signal is grounded.

- ☐ Shielding intended to reduce electromagnetically coupled noise at frequencies above 10 MHz must use a 360° peripheral connection at each end of the cable. No pigtails and no splicing are permitted.

- ☐ The shield metal and connector or enclosure metal must be electrochemically compatible to reduce corrosion (See Table 4.1.3-1).

- ☐ Don't use a cable shield as the return path for a balanced signal. Don't confuse the functions of shielding and signal return.

- ☐ Cable shields have no effect on magnetic fields at frequencies less than 10 kHz.

- ☐ A properly connected single braided shield can provide approximately 40 dB of shielding compared to an unshielded wire at frequencies less than 100 MHz.

- ☐ Use a silver coated copper braid. Do not use bare copper or tin coated braids because oxidation causes a loss of shielding effectiveness.

- ☐ A foil plus braid combination provides an effective electromagnetic or capacitive shield that can carry significant noise current and is flexible and strong.

5.1.2 Individual Wires

- ☐ All signals routed on an individual wire use the airframe structure as the return path.

- ☐ Outside the PV, each signal must have a dedicated return path. No signal can be routed on an individual wire with a structure return.

- ☐ No ARINC, audio or analog signals can use individual wires. They must all use a balanced twisted pair.

- ☐ The only signals that can use individual wires with a structure return are low frequency discretes, 400 Hz AC power and 28 VDC power.

- ☐ All individual wires routed within 1 meter of the flight deck windows will have a single braided shield with pigtail connections less than 2" at the disconnects and less than 4" at the LRU connector.

5.1.3 Balanced Twisted Shielded Pairs

- ☐ Balanced twisted shielded pair cabling is required for all ARINC, audio and analog signals.

- ☐ Balanced signal pairs must carry equal and opposite currents.

- ☐ The wire pairs must be twisted at a rate > 1 twist/inch for wire sizes smaller than #18 AWG. The twisting reduces differential mode magnetic coupling from lightning and crosstalk.

- ☐ The wire pairs must be balanced to increase the common mode rejection of lightning transients. Balance requires that the two wires have the same diameter and length. Shielding helps to improve the capacitive shunt balance.

- ☐ Balanced cables longer than 1 m carrying signal frequencies > 10 MHz require a constant characteristic impedance and matched termination to reduce reflections. These cables must be shielded to maintain a constant impedance and reduce electromagnetic susceptibility to HIRF. Typical twisted shielded pairs have $Z_0 \approx 100\ \Omega$.

5.1.4 Coaxial Cables

- ☐ Coaxial cables are unbalanced and should not be used for signal frequencies below 50 MHz.

- ☐ The outer conductor of a coaxial cable must have a 360° peripheral connection at each end. These connections provide electromagnetic shielding and the signal return path.

- ☐ Coaxial cables have a more constant characteristic impedance than twisted pairs and should be used for frequencies above 50 MHz.

- ☐ A coaxial connector should not be isolated or floating from a metal enclosure because of safety and electromagnetic susceptibility problems.

5.1.5 Bulkhead Mounted Connectors

- ☐ Recommendations for connectors mounted to metal LRU or card file enclosures are contained in 4.1.1.

- ☐ Bulkhead connectors must be electrically bonded to the airframe. Do not use electrically floating connectors.

- ☐ The outermost shield on the cable bundle must bond to the connector back shell. The type of connection, 360° or pigtail, is determined by the type of signals (see 5.1.2 and 5.1.3). If the cable contains any internal shields that

are electrically isolated from the outer shield, then these internal shields should be brought through the connector on individual pins.

- ☐ Balanced signal pairs must be assigned to adjacent connector pins.

- ☐ Assign connector pins by grouping compatible signals together, such as
  Group 1: AC power, DC power and discretes
  Group 2: Balanced digital signals (ARINC)
  Group 3: Analog, audio and RF signals.

5.2 SPECIFIC CABLING DESIGN GUIDELINES

5.2.1 Power

Be wary of the increasing amount of switch mode AC/DC and DC/DC converter harmonic current flowing through the airframe. This current may eventually reach a level that justifies the use of AC power neutral and/or 28 VDC return conductors in order to reduce noise coupling from the airframe.

- ☐ AC power, DC power and discretes may be routed together, as long as all separation requirements have been met.

5.2.1.1 Single Phase AC Power

The single phase 120 VAC 400 Hz power uses the airframe as the power neutral. The following guidelines apply to the AC power connection between a LRU and the airframe.

- ☐ The line, neutral and grounding conductors must be of equal wire size. The wire size is dictated by the load current requirement. All three conductors must be within 2" of one another. Connect the neutral and grounding conductors to the airframe at points less than 6" apart.

- ☐ Connect the safety grounding conductor just inside the metal LRU or card file enclosure and within 2" of the connector.

- ☐ Be wary of the harmonic currents drawn by AC to DC switch mode power converters. These currents can cause conductive and magnetic noise coupling.

5.2.1.2 Three Phase AC Power

The three phase 120 VAC 400 Hz power uses the airframe as the power neutral.

A balanced three phase load means equal sinusoidal currents per phase resulting in zero neutral current. Nonlinear switch mode AC to DC power converters produce significant nonsinusoidal (harmonic) current that can cause a neutral

(airframe) current larger than the phase current. These large airframe currents can exist even when the power load is equally divided between the phases.

5.2.1.3 28 VDC Power

The 28 VDC wiring uses the airframe as the current return path. This method reduces wire weight but allows significant noise coupling that must be removed by filtering at each LRU. In this case filtering is preferred over the use of additional wiring.

- ☐ Be wary of the harmonic currents drawn by DC to DC switch mode power converters.

5.2.2 Discretes

Discrete signals exist in one of three states:

OPEN - A high impedance to ground, typically > 70 kΩ;

GND - A "low" DC voltage to ground, typically < 5 V; and

HIGH - A "high" DC voltage to ground, typically > 9 V.

There are four combinations of these three states consisting of inactive/active pairs:

OPEN/GND

OPEN/HIGH

HIGH/GND

GND/HIGH

The high impedance OPEN state is most susceptible to capacitively coupled noise and may require a shielded cable in high electric field environments. The low impedance GND and HIGH states are most susceptible to magnetically coupled noise and may require a twisted pair cable.

- ☐ Inside the PV and greater than one meter from the flight deck windows, all discrete signals may be routed on individual wires and use the airframe structure as the current return path.

- ☐ Within one meter of the flight deck windows, HIGH/GND and GND/HIGH discretes will be routed on twisted pairs. OPEN/GND and OPEN/HIGH discretes will be routed on twisted shielded pairs. The shields will be connected to the airframe within one meter of the windows using pigtails less than 4 inches long.

- ☐ Outside the PV all discrete signals will be routed on twisted pairs and ungrounded. These signals will convert to a structure return at the first

bulkhead connector inside the PV. Some discretes outside the PV may also require shielding.

- ☐ Discrete signals may be routed with DC and AC power.

5.2.3 ARINC and RS Signals

5.2.3.1 ARINC - 429

- ☐ Route on a balanced twisted shielded pair.
- ☐ A single shield is sufficient with pigtail connections less than two inches long between the shield and each connector. The shield must be connected to the chassis on each end of the cable.

5.2.3.2 ARINC - 629 Stubs

- ☐ Route on a balanced twisted shielded pair with a constant $Z_0 = 100\ \Omega$.
- ☐ Use a double shield, such as a braid over a foil. Connect the shield with a 360° contact at each connector. Maintain continuity between all shield segments. Do not use any pigtails.

5.2.3.3 RS - 485

- ☐ Route on a balanced twisted shielded pair.
- ☐ A single shield is sufficient with pigtail connections less than 2 inches long between the shield and each connector. The shield must be connected to the chassis on each end of the cable.

5.2.4 Analog Signals

5.2.4.1 Audio

- ☐ Route on a twisted pair.
- ☐ Use a differential line driver and receiver.
- ☐ If a shield is used on the twisted pair, ground the shield only on that end of the cable where the signal is grounded.

5.2.4.2 RF

- ☐ Route unbalanced (single ended) RF signals on a coaxial cable. Connect the outer conductor (shield) with a 360° contact at each connector.
- ☐ Route balanced RF signals on a twisted shielded pair. Connect the shield with a 360° contact at each connector.

5.2.4.3 400 Hz AC Signals

- ☐ Route on a twisted shielded pair.
- ☐ A single shield is sufficient with pigtail connections less than 2 inches long between the shield and each connector.