University of Missouri-Rolla

Electromagnetic Compatibility Laboratory

Title: **A Printed Circuit Board's Response to Decoupling Capacitors**

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A Printed Circuit Board's Response to Decoupling Capacitors

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(Report Submitted by
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- *March 27, 1992*
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Abstract:

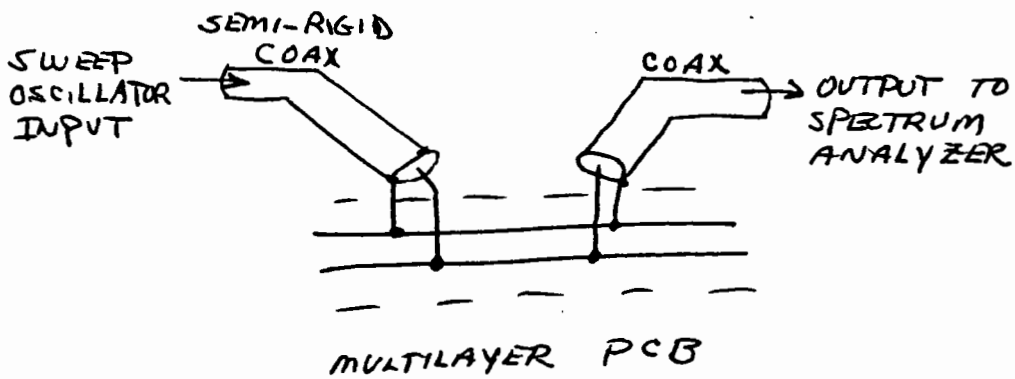
A typical printed circuit board was studied and observed under various capacitive load conditions. Decoupling capacitors are often used to inprove the performance of printed circuit boards by supplying local sources of charge to compensate for high transient currents. This procedure was investigated to note the dependance on location, lead length, quantity, and values of these decoupling capacitors. It was hypothesized that given the construction of modern pc boards and the frequencies at which they are operated, the decoupling capacitors may not be necessary, or at least do not require the high numbers of capacitors or the restrictions of location that are currently imposed in industry due to the inherent properties of the board.

Table of Contents:

Introduction:

The effects of decoupling capacitors on printed circuit boards were studied for limitations on four parameters: location, lead length, quantity, and capacitive value. A sweep oscillator was used as the input to the experimental system. The response was viewed on the spectrum analyzer, which showed a characteristic curve which was proportional to the impedance of the board. This curve was studied under various load conditions which were representative of variations on the parameters that restrict the use of decoupling capacitors.

The intent of the theory and experimental data was to show that due to the multi-plane construction of modern printed circuit boards a change in board construction may be possible. If decoupling capacitors are indeed necessary, then a few capacitors of higher value located arbitrarily on the board can replace the many low value capacitors mounted purposely near integrated circuit chips, as is common in practice today.



Theory/Background:

One of the concerns governing the use of integrated circuits on printed circuitboards has been that the transient currents associated with polarity changes on a chip can not be supplied in the time needed. Predominantly, this is corrected by placing capacitors near the chip. This is intended to provide a source of local charge, while keeping the voltage drop at this location due to the transient at a minimum. The capacitor is placed as close as possible to the chip also to lower the inductance which can slow the response since the current is not allowed to change instantaneously across an inductor. Recent trends seem to have been moving toward multi-layer boards which should not have the problems accompanied with charge location or the inductance found with currents in traces.

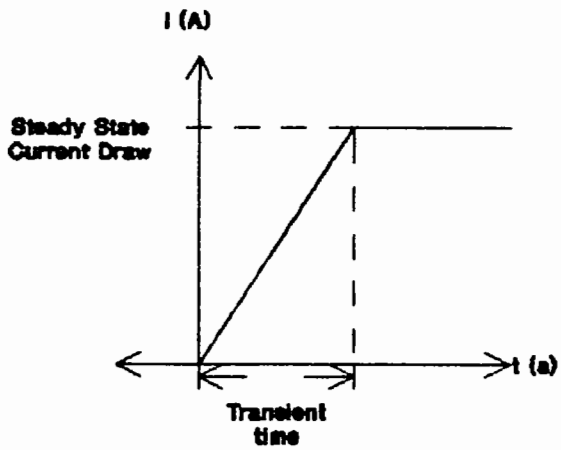


Figure 1: *Transient Response*

Figure 1 shows a possible transient current response. Considering the extra charge required to be the area under the curve during the transient time would yield

$$\int i\,dt = (dQ/dt)*t/2 = Q$$

Setting a maximum voltage fluctuation at dV yields the required capacitance

$$C = Q/dV$$

For the parallel plate setup of figure 2, the capacitance can be related as

$$C = eA/D$$

which implies

$$Q/dV = eA/D \text{ or } A = QD/dVe$$

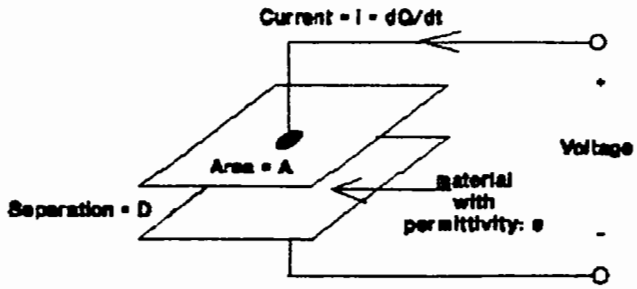


Figure 2: *Parallel Plate Capacitor*

The permittivity, *e*, is inherent to the center material. Distance, voltage deviation, and charge are determined by the setup. Therefore the area required by parallel plates to provide the necessary capacitance can be calculated. A typical calculation could be

$$dV = .1\ V$$

$$I = 50mA$$

$$t = 10ns \quad \text{which implies } C = 2500pF$$

$$e = e_o * e_r = e_o * 4.7 \qquad (e_o = 8.85E\text{-}12)$$

$$D = 6\ mils$$

which would require an area of $A = 14.2\ in^2$

So it would seem a heavily populated board with one power plane and one ground plane would not be able to supply the current, although a board with only a few scattered chips should not require any extra mounted capacitors.

Besides costly construction, the large number of small capacitors often have another drawback. When the small capacitors fail, they become shorts which can damage the board beyond repair. The larger capacitors have the benifit of going to open upon failure. This should increase the longevity of the board as well as heighten dependability.

Another aspect of the parallel plane PC board setup is that the plates allowforvery little magnetic flux, so the inductance should be negligible.

C = AN INDIVIDUAL DECOUPLING CAPACITOR

C_o = CAPACITANCE of POWER & RETURN PLANES

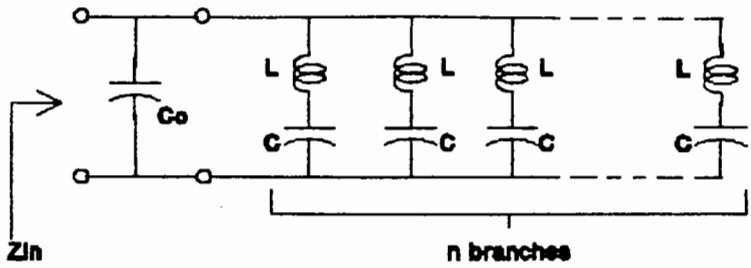


Figure 3: *Equivalent Circuit*

The low inductance and the fact that the board is small with respect to wavelength should allow for the charge to be drawn from anywhere on the board without requiring the decoupling capacitors to be mounted purposely close to the chip.

The mounted capacitors have a short lead (TRACE) length which therefore have a noticeable inductance at high frequencies. If all capacitors are considered equal and the lead lengths are equal the equivalent circuit should be that of figure 3, where Co is the board capacitance. The effect of parallel inductances is lessened while the parallel capacitances result in an increase. The equivalent circuit should look like figure 4. So if the number of capacitors were to be decreased without adding induction problems, the lead lengths would have to be shortened to *reduce* the actual inductance.

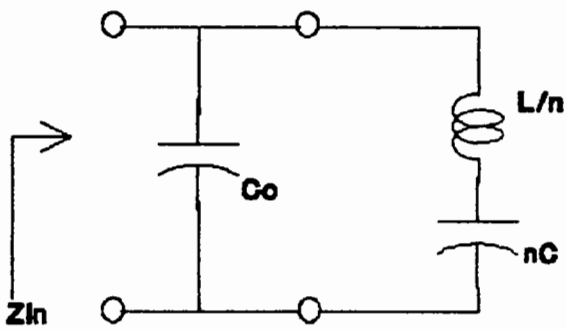


Figure 4: *Reduced Circuit*

By evaluating different resonant frequencies in the frequency response the various roles of induction and capacitor size may be of use. It is recalled that the zero caused by the series resonance is related by

$$w_s = 1/(LC)^{1/2}$$

The poles set up by the parallel components can be related by

$w_p = (1 + nC/Co)^{1/2}/(LC)^{1/2}$

or $f_p = f_s*(1 + nC/Co)^{1/2}$

Figure 5 shows the impedance versus frequency for the board with capacitors and the bare board. The magnitudes are found to be equal at

$w_a = (1 + nC/2Co)^{1/2}/(LC)^{1/2}$

or $f_a = f_s*(1 + nC/2Co)^{1/2}$

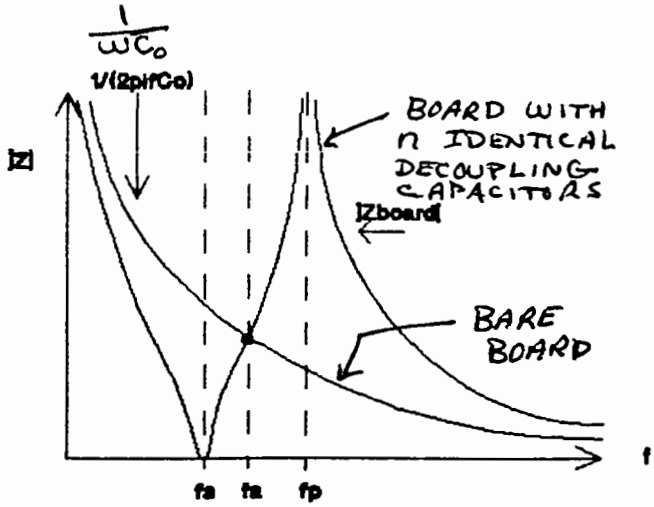


Figure 5: *Impedance*

These equations should prove useful in interpreting impedance responses of the printed circuit board. Pages A-1.1 to A-1.3 in appendix 1 show that the inductance seems to dominate the location of the pole and zero for a hooked up (DECOUPLING) capacitor, and the actual capacitance determines the distance between the zero and pole.

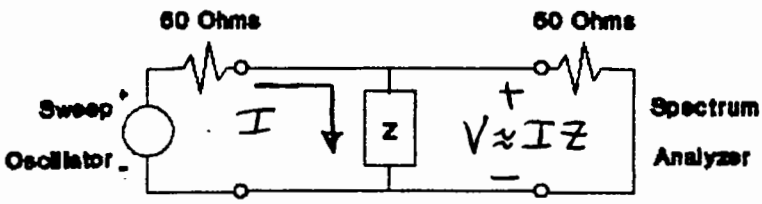


Figure 6: *Test Circuit*

The primary test setup is seen in figure 6. The board impedance is so small at the higher frequencies that the current should flow primarily through the board and therefore the sweep oscillator will see 50 ohms in series with a very small impedance. The result is that the current should stay constant over the sweep range and the spectrum analyzer should measure the voltage differences over a range of frequencies across the board which now are directly proportional to the impedance.

Results/Analysis:

The spectrum analyzer produced plots which represent a basic form of the impedance. Page 4 from Appendix A-1 shows the input impedance form for the bare board with approximately a 1 in^2 hole in the middle. This plot shows approximately the expected response for a LUMPED capacitor up to a frequency of 200Mhz. Beyond this frequency, the board shows transmission line characteristics, which include seing the edge of the board as an short or open circuit at quarter or half-wavelength intervals, respectively. For example, the input terminal was approximately 4-1/4 inches from the edge of the board. Using this value as a quarter wavelength, the corresponding frequency should be about 320Mhz, assuming an $e_r = 4.7$. This frequency corresponds almost exactly to a frequency, f_3, on the graph ON PAGE A1.4.

Reducing the range of frequencies to 200Mhz and below allowed the board to be viewed where the transmission line affects are not relevant. Placing a 0.01μF capacitor at several different locations resulted in A-1.5. The capacitor used for each location was the same but the differences in each curve corresponded predictably to lead length involved with the particular connection, according to the background theory. Visual inspection of the locations verified that indeed the leftmost curve corresponded to the longest lead lengths and therefore the highest inductance.

Theoretically, the more capacitors involved, the lower the inductance, and the respective curve should shift to the right of the spectrum. The results in A-1.6 confirm this view. When several capacitors are added across the board, the resulting curve is shifted to the right. Using a single capacitor as a reference shows the validity of the inductor theory. Since

inductors add inversely in parallel and the single inductor was placed at a location common to both setups, the multiple capacitor setup must have a lower inductance. Assuming therefore that the differences in impedance curves is due to inductance, the location of the decoupling capacitors is irrelevant as far as proximity to load is concerned.

By placing shorts at various locations a worst case load can be simulated. The results should show a zero at low frequencies, and then the typical capacitor and inductor relationships at higher frequencies. The high number of connections between the power and ground planes should reduce the total inductance significantly, thus forcing the resonant frequencies to the right of the spectrum. The resistive load should also "soften" the resonant peaks since actual zeros and infinities cannot be reached. This is precisely what was found when plotted, as seen in A-1.7.

The first experimental board had a small hole in the center but when a complete board was obtained, the response was nearly identical as observed when comparing A-1.5 to A-1.8.

The plot on page A-1.9 shows a comparison between a completely populated board and the experimental worst case load board. Over the lower range the impedance of the populated board indeed stayed flatter and lower than the worst case setup. The differences at the higher end can be attributed to the location of the terminals on the populated board as previously discussed.

To further prove the relation between inductance and the resulting impedance curve, two different capacitors (observed separately) with variable lead lengths were applied to the board at a single location. The figures of A-1.10 and A-1.11 show the results of this test. They clearly show that the lower the inductance, the further to the right of the

spectrum the curve was shifted. Therefore if the inductance is to be lowered (thereby increasing current response time) the capacitor leads to the power and ground planes must be shortened.

In an attempt to gain further insight into the impedance characteristices of the printed circuit board, the S-parameter test set was used. The input impedance corresponded to the S_{21} scattering parameter. This discussion should be pre-empted by noting that the S-parameter test set results in an unstable curve, which makes reading with accuracy difficult.

The wide range response of both the fully loaded and mock loaded boards found on page A-1.12 correspond quite well to the results obtained from the spectrum analyzer. The high range of the S-parameter tests show the intense transmission line effects at higher frequencies.

Page A-1.13 compares the wide band responses with and without the shorts. At lower ends the impedance peaks are noticably "softened" by the addition of the shorts but at higher frequencies the two curves start to coincide as transmission line effects take over.

The end result showed that if lead lengths are small so that inductance is negligible then a few capacitors could be used of a higher value at arbitrary locations chosen at the board designers discretion.

Conclusion:

The role of decoupling capacitors on printed circuit boards was evaluated for dependency on four parameters: location, lead length, quantity and capacitive value. The response of the pc board was studied theoretically and experimentally under various load conditions. It was determined that although under most circumstances it would not be practicle to remove all decoupling capacitors from the board, the restrictions typically placed on the implementation of these capacitors could be greatly relaxed.

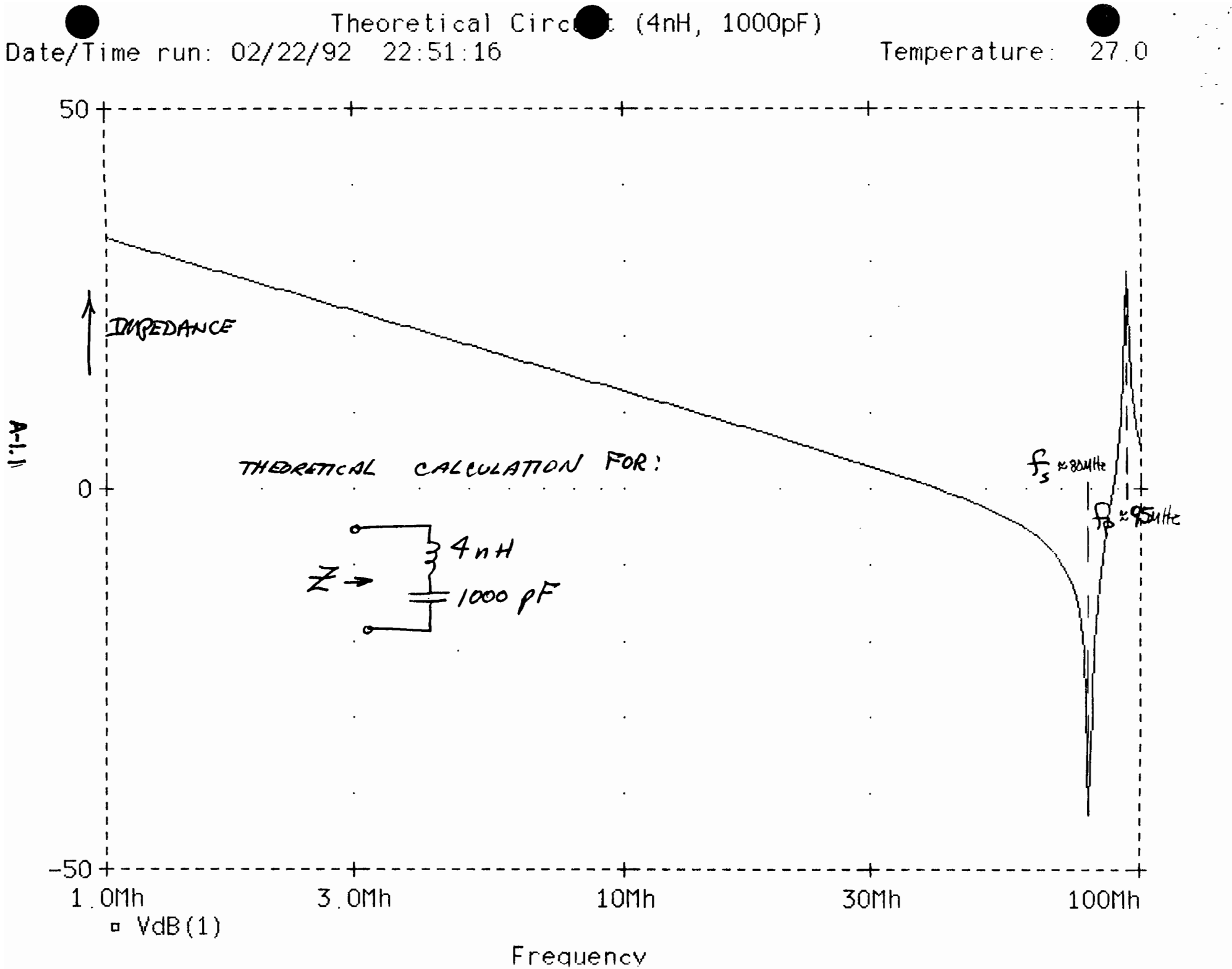
Since the inductance of the board was neglible, and the distances associated with it were small compared to normal operation wavelengths, the location of the capacitors not a factor of the board's ablility to respond. Since the location is not a factor, fewer capacitors of greater value can be substituted for the present practice of many small capacitors at discrete locations.

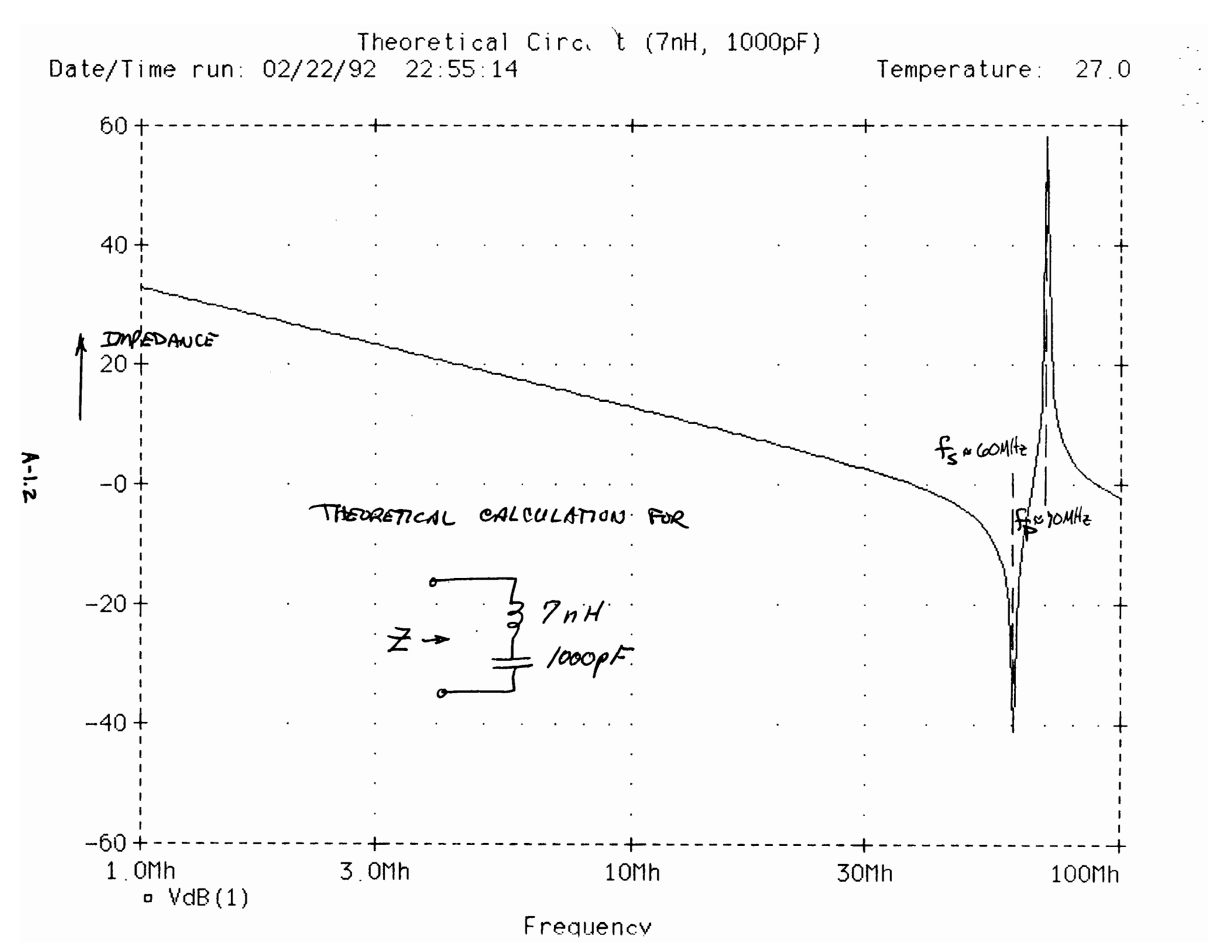
The inductance associated with the lead length of a capacitor is inversely proportional to the number of capacitors used. By reducing the quantity, the inductive problem becomes significant. This can be corrected by creating lead lengths that are as short as possible, preferably on top of the vias, so as to provide the smallest loop for magnetic flux.

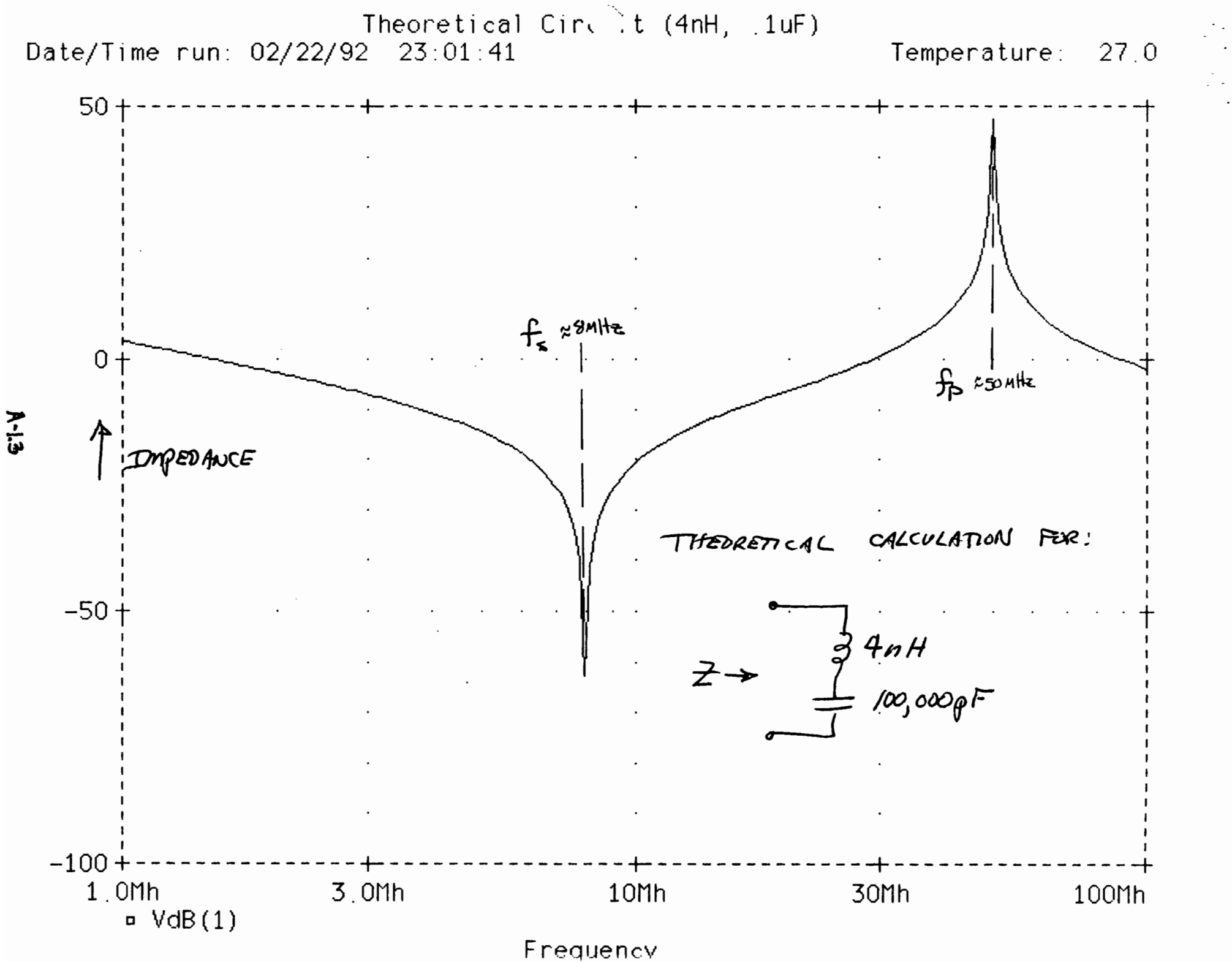
The small capacitors that are typically mounted next to the IC chips are small enought that when they fail they become shorts, often damaging the board beyond repair. The larger capacitors have the added bonus of typically going to opens upon failure thus allowing the board to be easily repaired. The overall effect is longer life and greater reliability of the printed circuit board.

In conclusion, the cost of construction, the difficulties of manufacturing, and the failure rate of such boards should all decline if such measures were taken.

Appendix 1: Graphs


Theoretical Circuit (4nH, 1000pF)
Date/Time run: 02/22/92 22:51:16
Temperature: 27.0
50
0
-50
IMPEDANCE
A-1.1
THEORETICAL CALCULATION FOR:
Z
4nH
1000 pF
$f_s \approx 80$MHz
$f_p \approx 95$MHz
1.0Mh
3.0Mh
10Mh
30Mh
100Mh
VdB(1)
Frequency

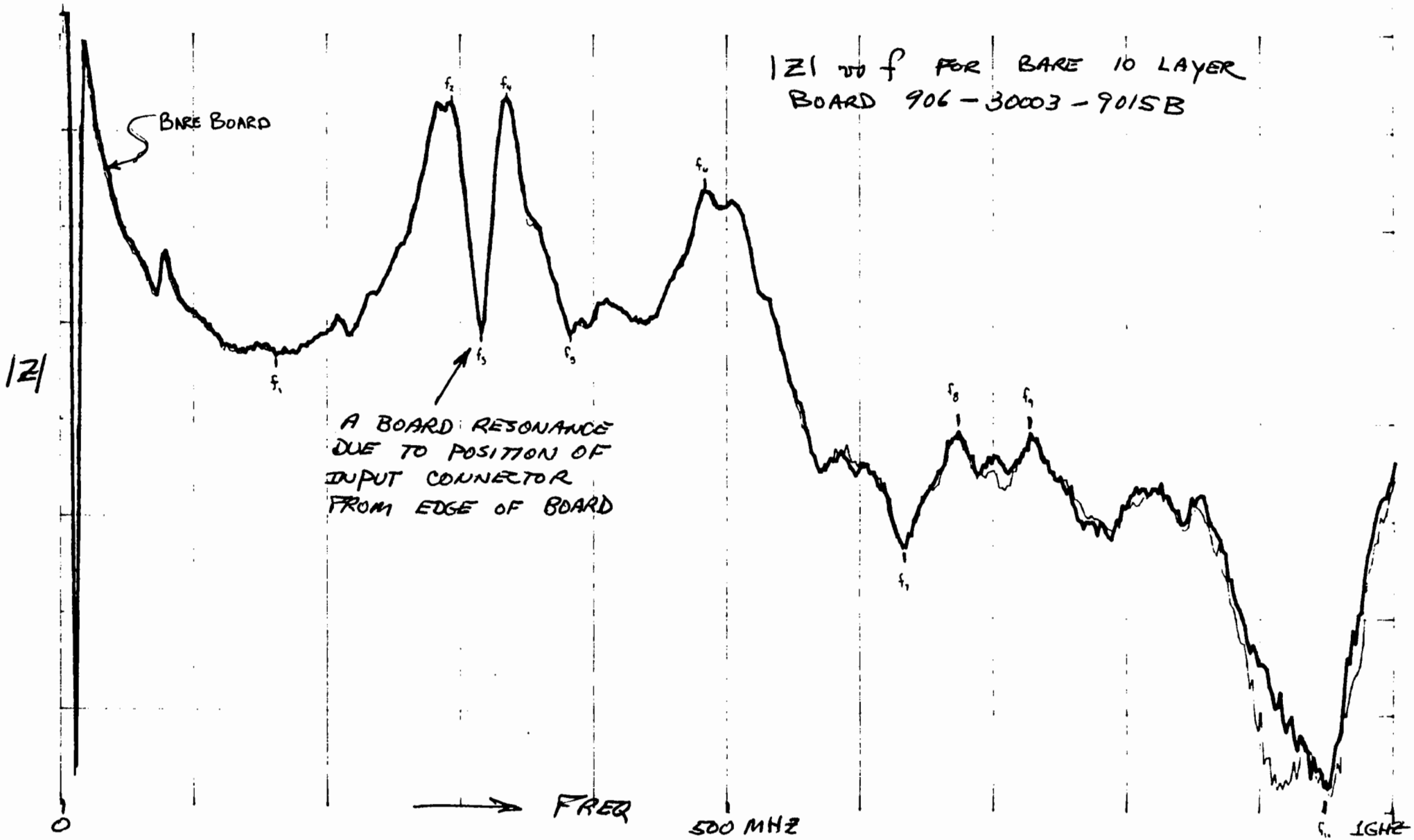

Theoretical Circ t (7nH, 1000pF)
Date/Time run: 02/22/92 22:55:14
Temperature: 27.0
60
40
20
-0
-20
-40
-60
IMPEDANCE
A-1.2
THEORETICAL CALCULATION FOR
Z
7nH
1000pF
$f_s \approx 60MHz$
$f_p \approx 70MHz$
1.0Mh
3.0Mh
10Mh
30Mh
100Mh
VdB(1)
Frequency


Theoretical Circuit (4nH, .1uF)
Date/Time run: 02/22/92 23:01:41
Temperature: 27.0
50
0
-50
-100
1.0Mh
3.0Mh
10Mh
30Mh
100Mh
VdB(1)
Frequency
A-13
IMPEDANCE
$f_s \approx 8$MHz
$f_p \approx 50$MHz
THEORETICAL CALCULATION FOR:
Z
4nH
100,000pF

3/10/92

CTR 499.9 MHz SPAN 100 MHz/ RES BW 3 MHz VF OFF

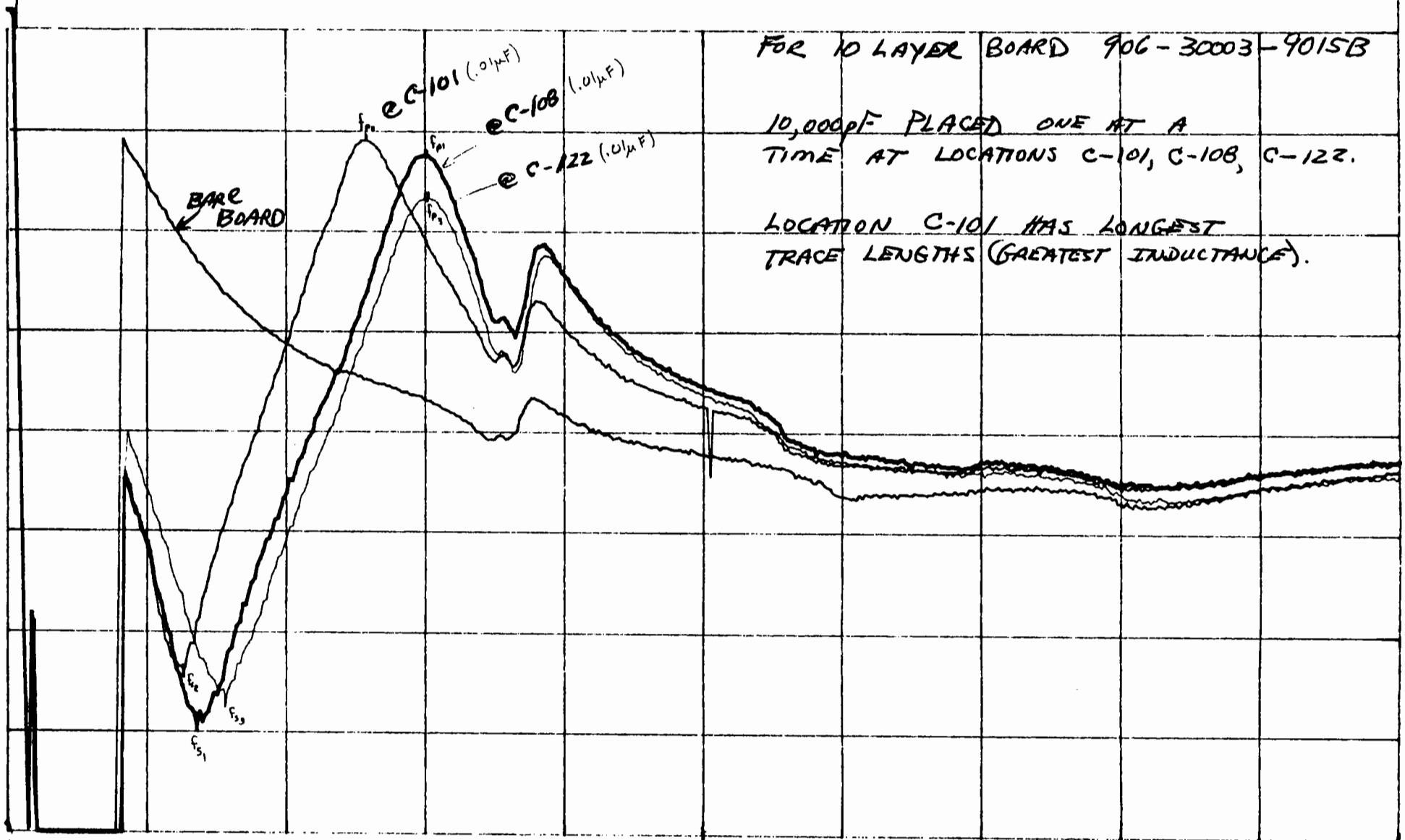
REF -5 dBm 5 dB/ ATTEN 30 dB SWP 1 sec/



3/10/92

CTR 100.0 MHz SPAN 20 MHz/ RES BW 300 kHz VF OFF

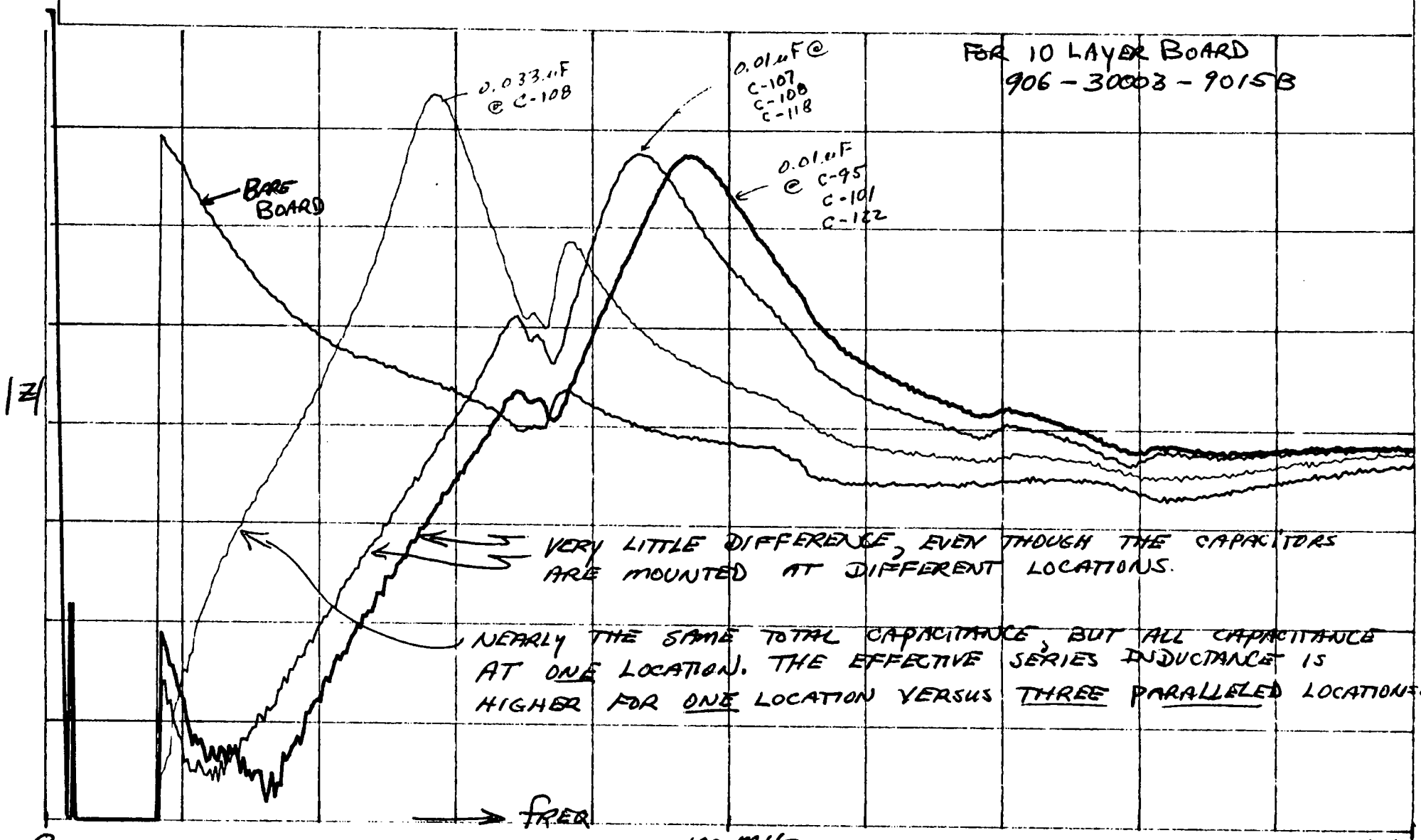
REF 0 dBm 5 dB/ ATTEN 30 dB SWP 1 sec/



3/10/92

CTR 100.1 MHz SPAN 20 MHz/ RES BW 300 kHz VF OFF

REF 0 dBm 5 dB/ ATTEN 30 dB SWP 1 sec/



VERY LITTLE DIFFERENCE, EVEN THOUGH THE CAPACITORS ARE MOUNTED AT DIFFERENT LOCATIONS.

NEARLY THE SAME TOTAL CAPACITANCE, BUT ALL CAPACITANCE AT ONE LOCATION. THE EFFECTIVE SERIES INDUCTANCE IS HIGHER FOR ONE LOCATION VERSUS THREE PARALLELED LOCATIONS.

A-1.6

Shorts at C-95, C-107, C-141, C-122, C-153
1000 pF at C-108, C-101, C-123, C-121, C-152

3/10/92

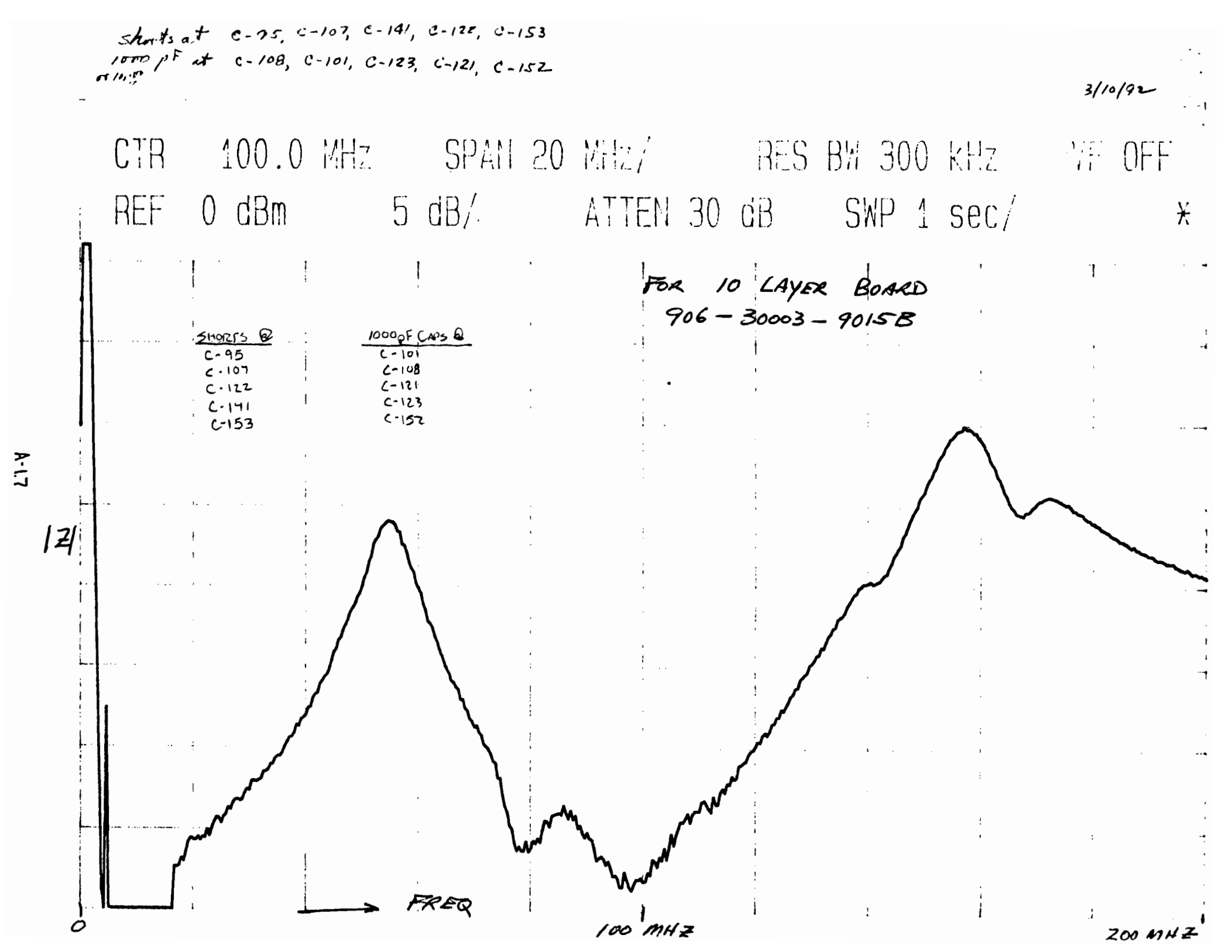
CTR 100.0 MHz SPAN 20 MHz/ RES BW 300 kHz VF OFF

REF 0 dBm 5 dB/ ATTEN 30 dB SWP 1 sec/ *

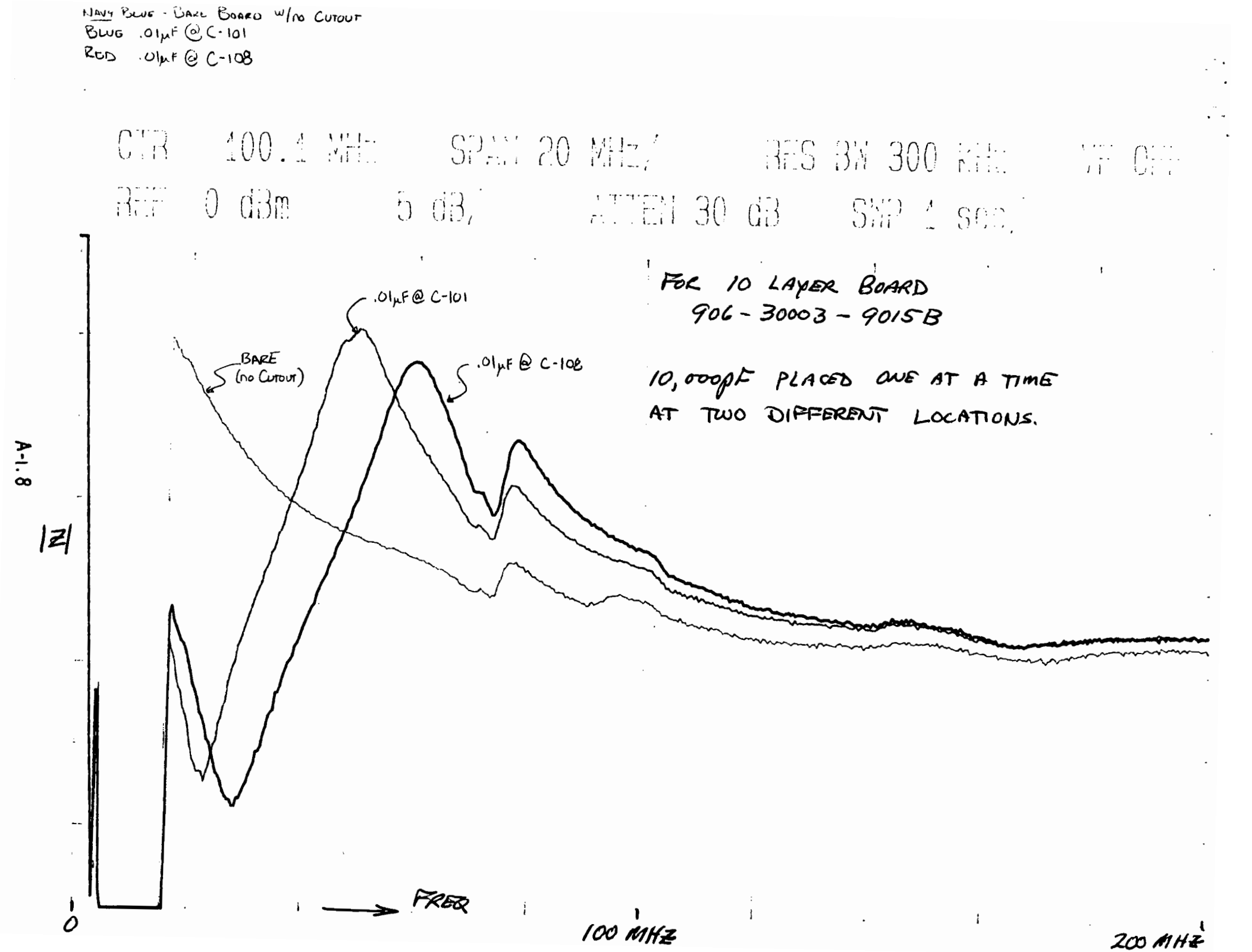
FOR 10 LAYER BOARD
906-30003-9015B

SHORTS @
C-95
C-107
C-122
C-141
C-153

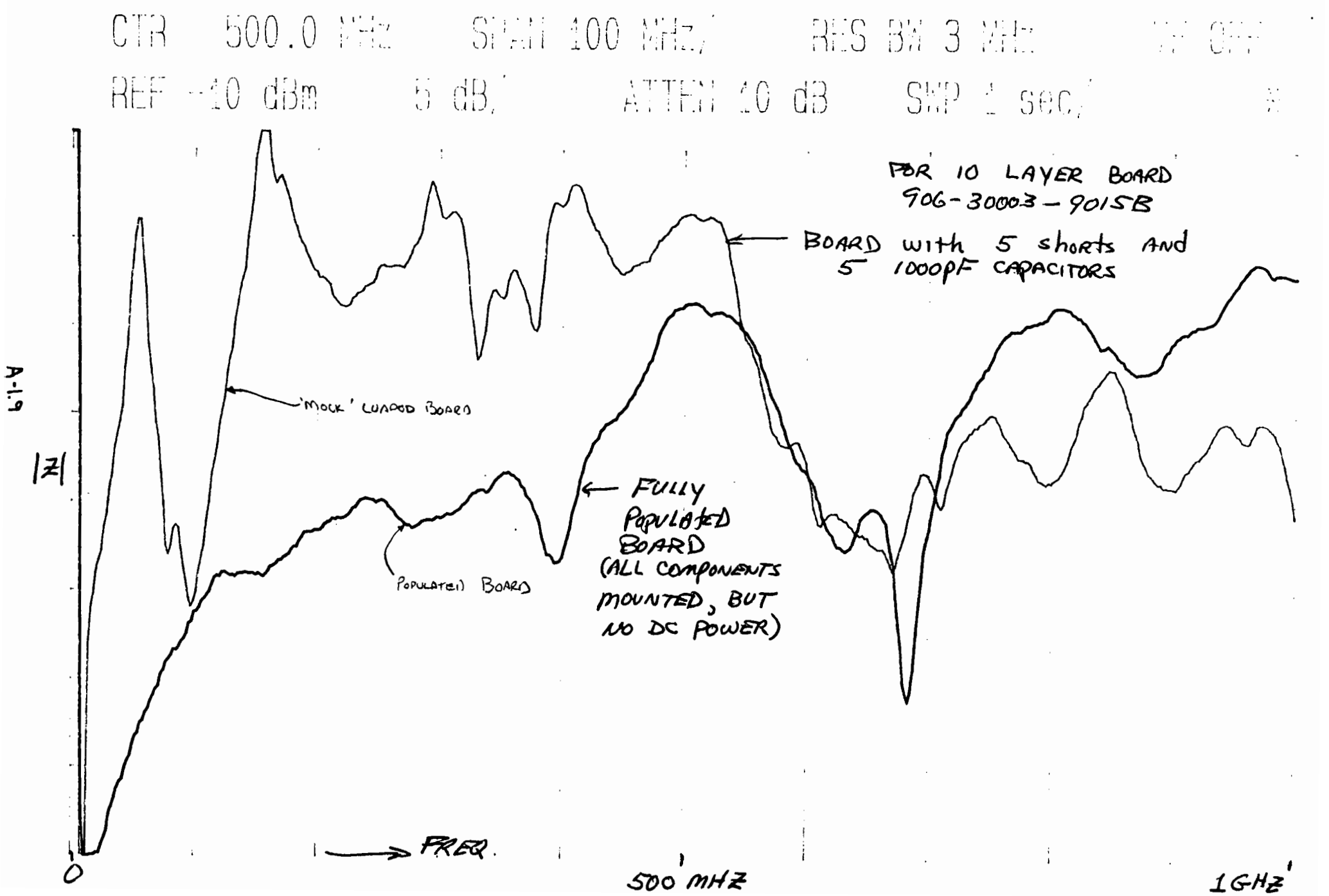
1000pF CAPS @
C-101
C-108
C-121
C-123
C-152



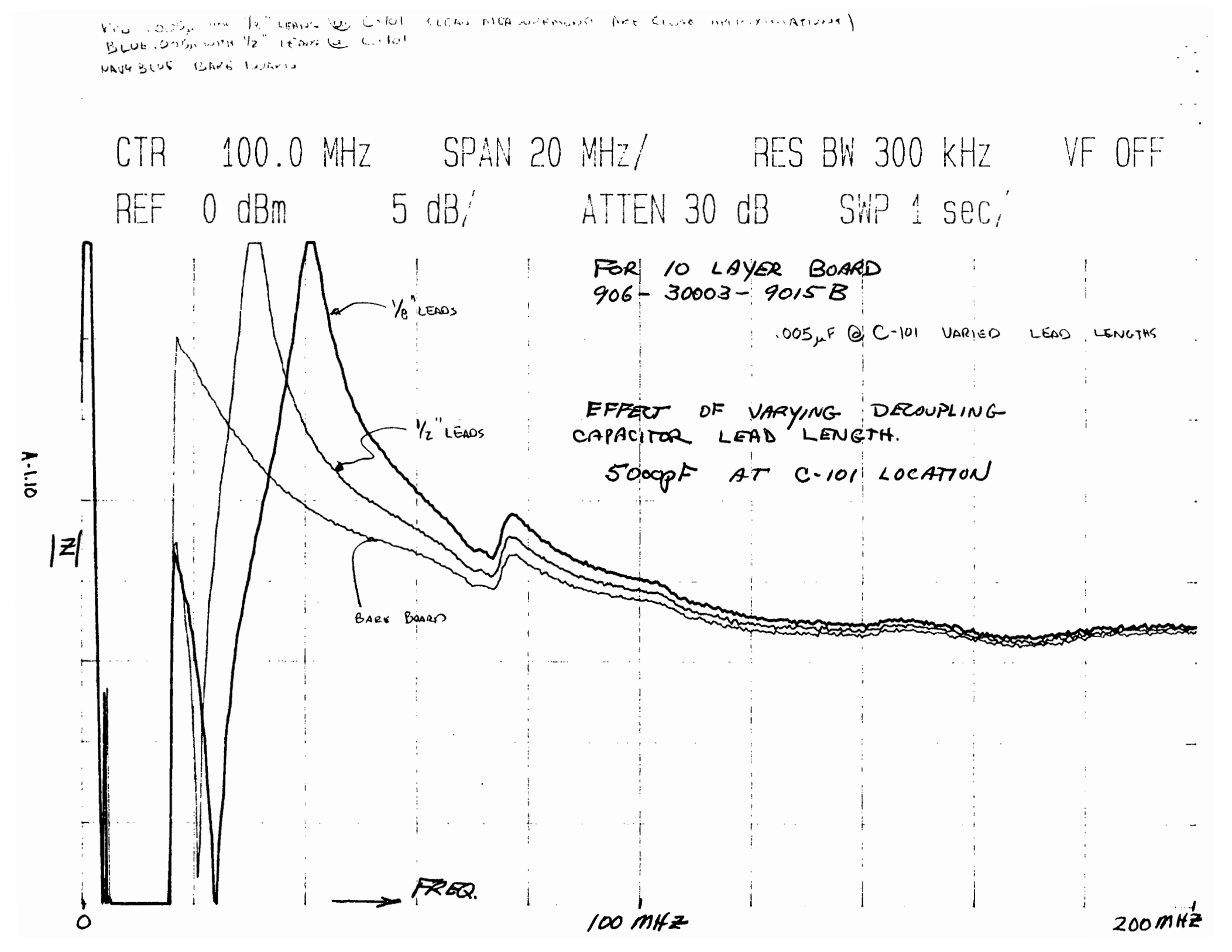
NAVY BLUE - BARE BOARD W/NO CUTOUT
BLUE .01μF @ C-101
RED .01μF @ C-108



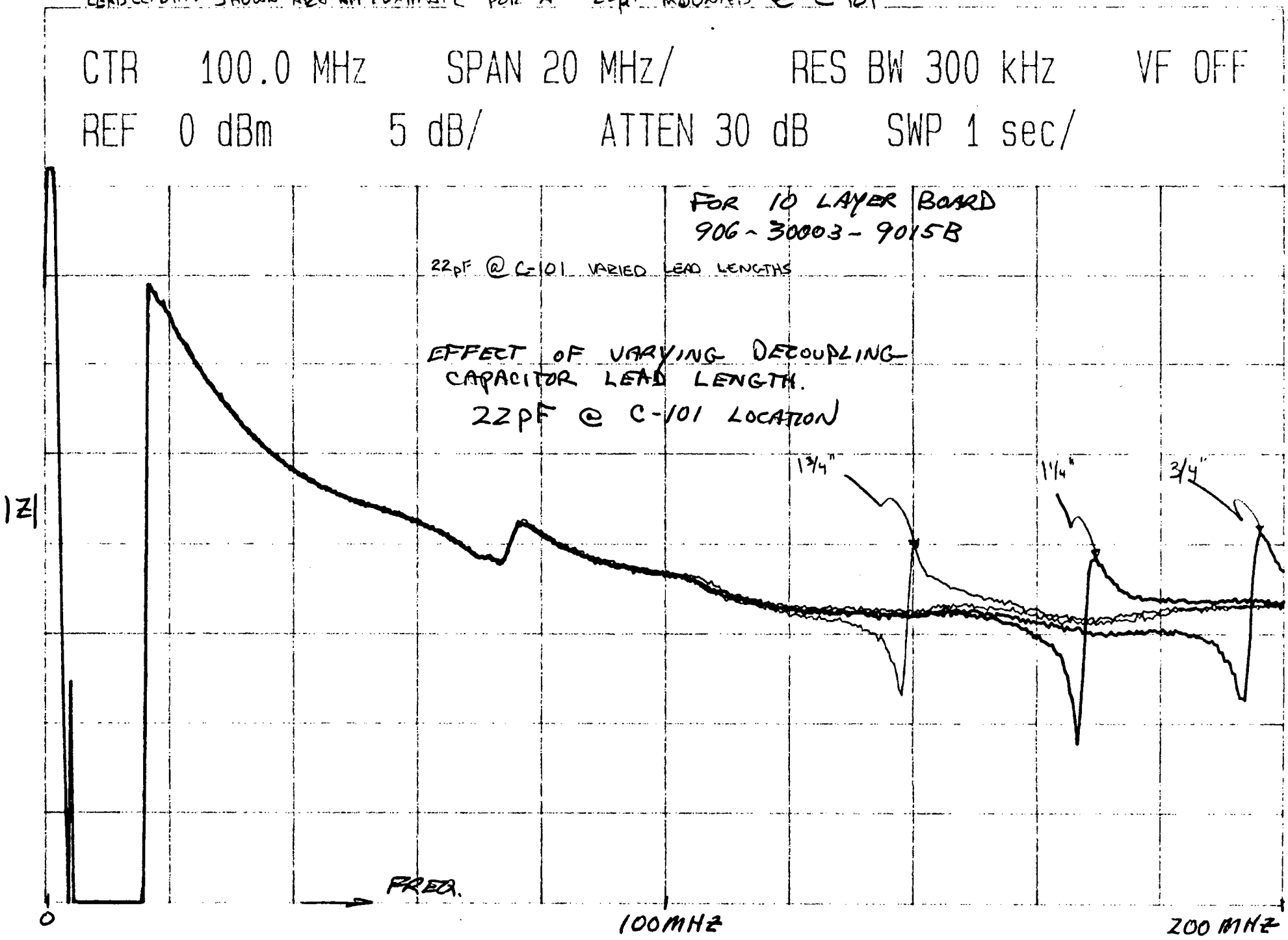
BLUE - 'MOCK' LOADED BOARD
RED - FULLY LOADED (COMPLETELY POPULATED BOARD)

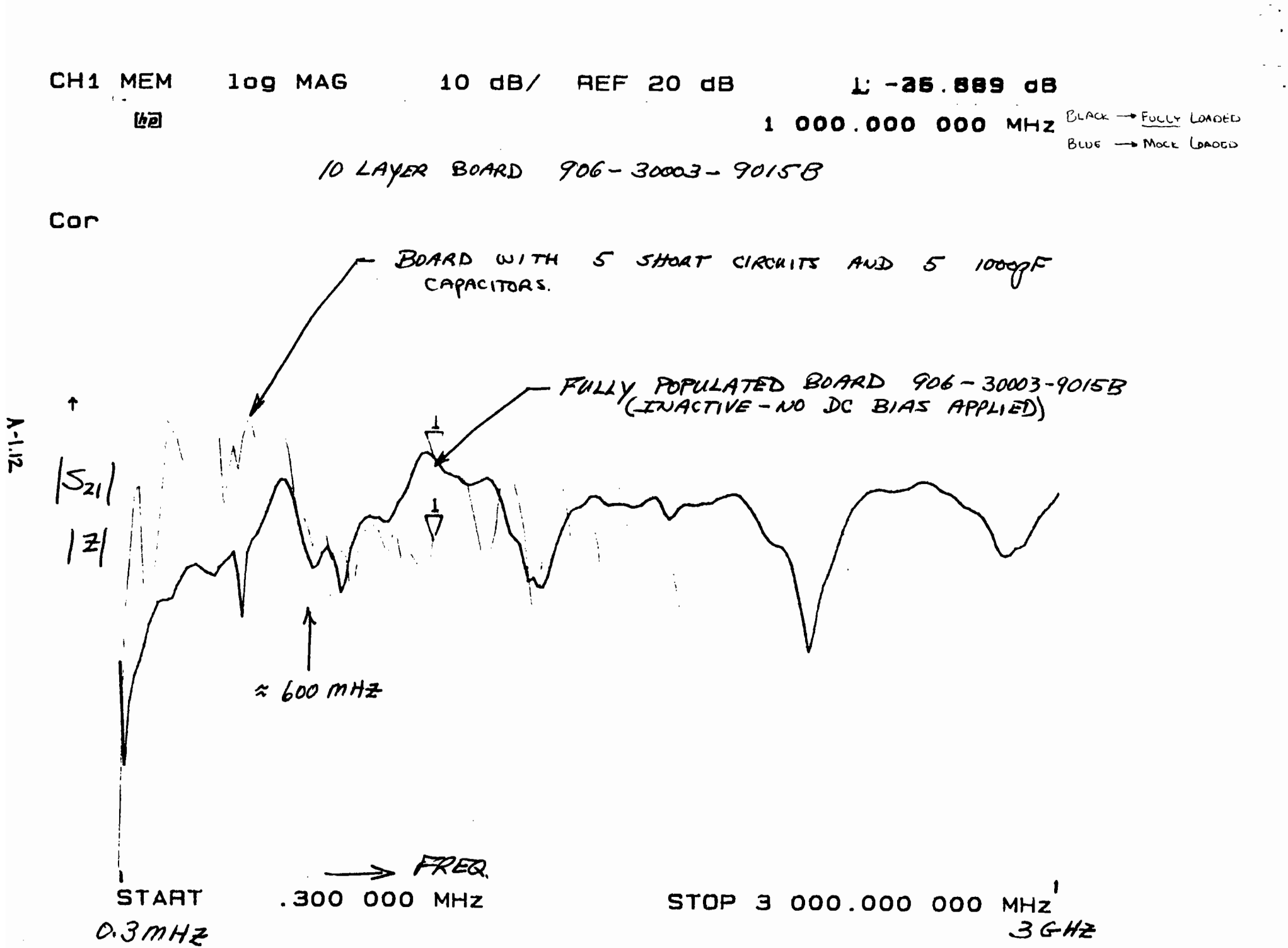


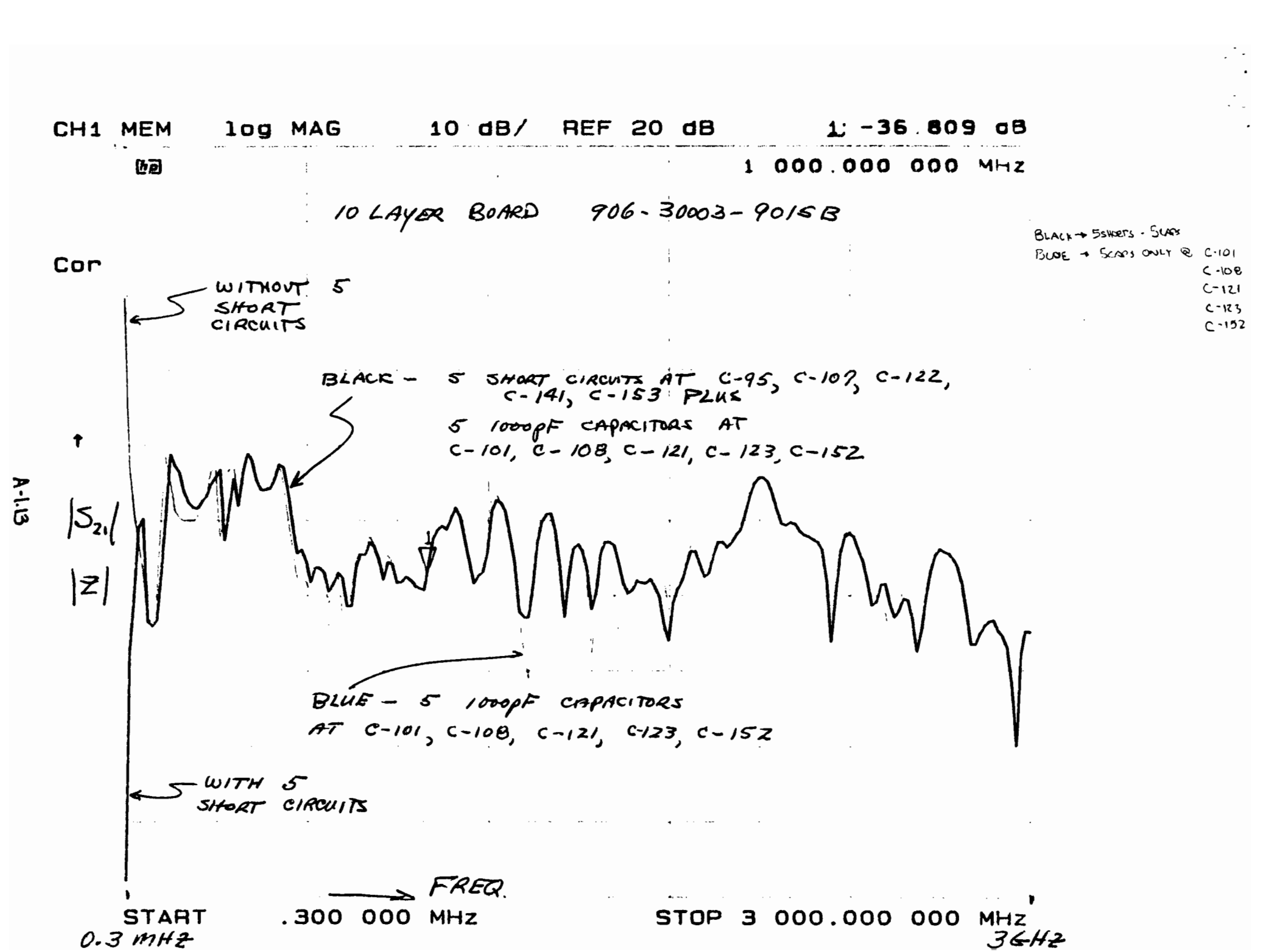
RED .005μF WITH 1/8" LEADS @ C-101 (LEADS NEAR VERTICAL, SEE CLOSE UP PHOTOGRAPHS)
BLUE .005μF WITH 1/2" LEADS @ C-101
NAKED BLUE BARE BOARD



LEAD LENGTHS SHOWN ARE APPROXIMATE FOR A 22pF MOUNTED @ C-101




CH1 MEM log MAG 10 dB/ REF 20 dB
L: -25.889 dB
1 000.000 000 MHz
BLACK → FULLY LOADED
BLUE → MOCK LOADED
10 LAYER BOARD 906-30003-9015B
Cor
BOARD WITH 5 SHORT CIRCUITS AND 5 1000pF CAPACITORS.
FULLY POPULATED BOARD 906-30003-9015B (INACTIVE - NO DC BIAS APPLIED)
A-1.12
|S21|
|Z|
≈ 600 MHz
FREQ.
START .300 000 MHz
0.3 MHz
STOP 3 000.000 000 MHz
3 GHz


CH1 MEM log MAG 10 dB/ REF 20 dB 1: -36.809 dB
1 000.000 000 MHz
10 LAYER BOARD 906-30003-9015B
BLACK → 5 SHORTS - SCANS
BLUE → SCANS ONLY @ C-101 C-108 C-121 C-123 C-152
Cor
WITHOUT 5 SHORT CIRCUITS
BLACK - 5 SHORT CIRCUITS AT C-95, C-107, C-122, C-141, C-153 PLUS 5 1000pF CAPACITORS AT C-101, C-108, C-121, C-123, C-152
|S21|
|Z|
BLUE - 5 1000pF CAPACITORS AT C-101, C-108, C-121, C-123, C-152
WITH 5 SHORT CIRCUITS
FREQ.
START .300 000 MHz
STOP 3 000.000 000 MHz
0.3 MHz
3GHz
A-1.13

Appendix 2:Procedure

The test board was found to have ten layers. Various locations were checked for capacitance and determined to be hooked between the ground and power planes. The average capacitance of these planes was measured at 2600pF.

Two SMA connectors were soldered to the board for input and output terminals. The sweep oscillator was hooked to input, while the spectrum analyzer was used to view the impedance as discussed in Theory & Background. Data plots were made under the following conditions:

Original Board (with about 1 in^2 hole in middle)
Bare board from 10MHz to 1GHz
One .01μF capacitor at three different locations from 10MHz to 200MHz
Three .01μF capacitors at two locations from 10MHz to 200MHz
One .033μF capacitor at one location from 10MHz to 200MHz
Five shorts and five .001μF capacitors from 10MHz to 200MHz to represent a loaded board
Five shorts and five .001μF capacitors from 10MHz to 1GHz

New Board (without hole)
Bare board from 10MHz to 200MHz
One .01μF at two different locations from 10MHz to 200MHz
One .005μF capacitor at one location with two variable leads (1/8in and 1/2in) from 10MHz to 200MHz
One 22pF capacitor at one location with three variable leads (3/4in, 1-1/4in, and 1-3/4in) from 10MHz to 200MHz

Actual Populated Board
Board scan from 10MHz to 1GHz

FORWARD TRANSMISSION COEFFICIENT S_{21}

Scattering parameter test set was used to study S_{21} (~~input impedance~~) of different setups:

$|S_{21}| \simeq |Z_{PCB}|$

Original Board (with about 1 in^2 hole in middle)
Five shorts and five .001μF capacitors from 300kHz to 3GHz to represent a loaded board
Five .001μF capacitors at various locations from 300kHz to 3GHz
Four .001μF capacitors at various locations from 300kHz to 3GHz
Three .001μF capacitors at various locations from 300kHz to 3GHz
Two .001μF capacitors at various locations from 300kHz to 3GHz
One .001μF capacitor from 300kHz to 3GHz
Bare board from 300kHz to 3GHz
Bareboard from 300kHz to 1 GHz

One .001uF capacitor at one location from 300kHz to 1GHz
Bare board from 300kHz to 200MHz
One .001uF capacitor from 300kHz to 200MHz

Actual Populated Board
board scan from 300kHz to 3GHz

Note: All plots can be found in Appendix 1

Appendix 3: Equipment List

2 X Printed Circuit boards
1 X Fully populate circuit board
Spectrum Analyzer
Sweep Oscillator
S-parameter Test Set
Network Analyzer
Digital Multimeter
Capacitance Meter
Plotter
Capacitors:
  3 X .01uF
  5 X .001uF
  1 X .033uF
  1 X 22pF
  1 X .005uF
5 pieces of wire used as shorts
various probes and adaptors as necessary

Appendix 4: References

Stanley V. Marshall, and Gabriel G. Skitek, *Electromagnetic concepts and applications*, Prentice Hall, Englewood Cliffs, New Jersey 07632, 1990.

Adel S. Sedra, and Kenneth C. Smith, *Microelectronic circuits*, Holt, Rinehart, and Winston, Inc., 1987.

Clayton R. Paul, *Analysis of linear circuits*, McGraw Hill Book Company, 1989.

John Sisler, "Eliminating Capacitors from Multilayer PCBs," *Printed Circuit Design*, pp. 14-23, July 1991.