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Title: **Printed Circuit Board Response to the Addition of Decoupling Capacitors**

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Printed Circuit Board Response to the Addition of Decoupling Capacitors

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Abstract

This report presents the results of a study which investigates the effectiveness of decoupling capacitors on multilayer printed circuit boards. The original objective of the research was to demonstrate that a significant level of high-frequency decoupling can be provided by taking advantage of the printed circuit board power bus interplane capacitance. Since large numbers of decoupling capacitors can affect the wiring of the design and the failure rate of printed circuit boards, it is important to make the most effective use of every capacitor. The project goal was to develop guidelines to assist circuit designers in choosing and applying decoupling capacitors wisely, and investigate the use of the printed circuit board power bus interplane capacitance for improving high frequency decoupling.

The results and conclusions reported herein are based on an extensive set of models and measurements. Printed circuit boards provided by Boeing were employed for the measurements. Several typical measured results are reported herein, and additional measurements have been included in previous reports to Boeing. Important conclusions drawn from these results include:

- The inductance of the traces and vias that connect decoupling capacitors to the power and ground planes is extremely critical. Minimizing this inductance should be a high priority.
- The printed circuit boards provided by Boeing (which use standard types of design procedures) had measured trace inductances through which decoupling capacitors were connected of $2-10\ nH$. Measurements on these boards indicated that all of the decoupling above 100 MHz was provided by the interplane capacitance of the power bus. The significant inductance of the interconnects prevented any of the added capacitors from supplying significant current at high frequencies.
- Decoupling capacitors should be positioned in a manner that minimizes the inductance of the connecting traces. The inductance per unit length of the internal planes is significantly lower than trace inductance. Therefore, a capacitor positioned away from the component it is meant to decouple is acceptable if a lower inductance connection to the internal planes is then achievable.
- The most effective means of improving high frequency decoupling is to maximize the capacitance between the internal power and ground planes.

Equations are provided that can assist a board designer in determining the frequency range over which the decoupling capacitors of a printed circuit board are effective. In this case, surface-mount capacitors are considered to be ineffective when insignificant current is supplied relative to the current provided by the interplane capacitance of the power bus. The equations provided can be used to determine if the decoupling for a particular board design can be improved by adding capacitors of a given value.

1 Introduction

The objective of this project was to: 1) develop guidelines to assist printed circuit board (PCB) designers in reducing the number of decoupling capacitors required in a given design, i.e., eliminating ineffective capacitors; 2) increase the usable frequency range for a smaller number of capacitors; and, 3) investigate the use of the interplane capacitance of the PCB power and return planes for achieving improved high frequency decoupling. The decoupling capacitors connected between the power and ground pins of an integrated circuit module provide a local source of charge during device switching. In the absence of this local source of charge, switching currents must be drawn through the high inductance connection of the power supply to the (low inductance) PCB power bus. The current surge passing through the power supply inductance results in a voltage sag on the power bus, potentially causing false logic switching. While the need for decoupling capacitors is well known in practice, determining the size and number of decoupling capacitors required to provide adequate decoupling for a given design remains to a considerable degree an art.

Other studies have investigated high frequency decoupling (above 10 MHz). Paul addressed the misconception that the high frequency decoupling performance of surface-mount capacitors is improved by placing large and small values of capacitance in parallel [1]. It was shown that the parallel and series resonances between the inductance associated with the interconnects of the capacitors and the surface-mount capacitors significantly affects the frequency response of the added capacitors. Another study investigated increasing the interplane capacitance of the PCB power bus to reduce high frequency noise on the power bus [2]. In this study Sissler demonstrated experimentally, from noise measurements on the power bus for a UNISYS 386i motherboard, that 137 surface-mount capacitors could be eliminated from the design by increasing the capacitance of the PCB power bus. The high frequency noise ($30 - 200$ MHz) for the novel design was significantly decreased as compared to the previous design with the additional 137 surface-mount capacitors.

The impedance of an ideal capacitor is given by $Z_c = \frac{1}{j\omega C}$, and decreases with frequency at 20 $\frac{dB}{decade}$. In practice, however, pure capacitance is seldom realized. The exception to this is the interplane capacitance of the PCB power bus, which can be of the order of $3 - 5$ nF for typical 8" square PCBs. The added series resistance and inductance of the interconnects of surface-mount capacitors compromises the ideal response of the capacitor. While the rate at which current can be drawn from an ideal capacitor is limited only by the 'load' to which it is connected, the rate at which current can be drawn through an RLC is limited not only by the load but also by the frequency response of the series network [3]. The surface mount decoupling capacitor is then behaving like an ideal capacitor only over a limited frequency range. The objective is to achieve ideal behavior from a decoupling capacitor over the widest possible frequency range.

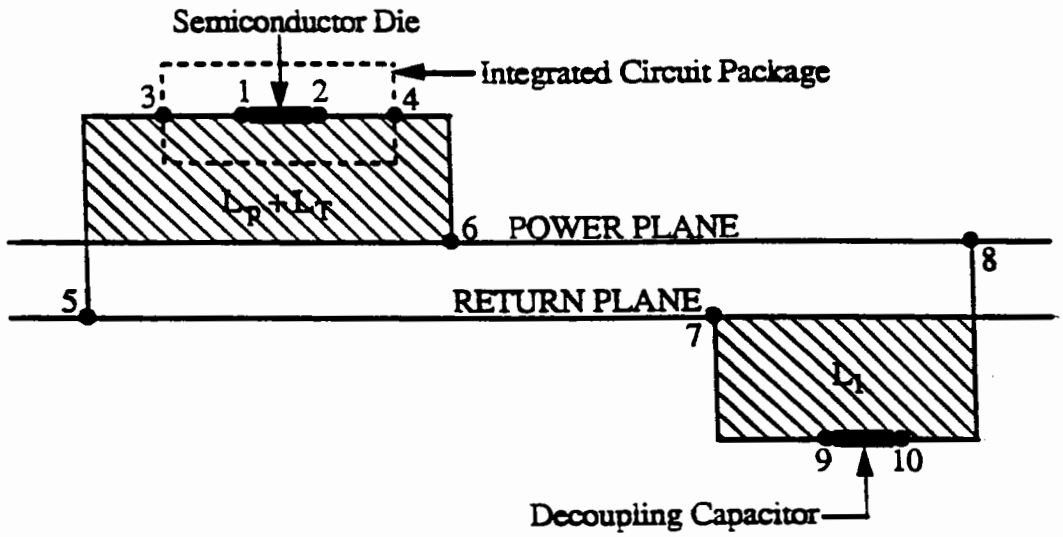
The study reported herein is conducted in the frequency domain, and focuses on high frequency decoupling in the $10 - 200$ MHz range. Frequency domain studies allow for a systematic investigation of the deviation of the response of decoupling capacitors added to a PCB from the ideal response as a function of frequency, and hence, the rise time of the current that can be supplied by the decoupling capacitor. These deviations are then easily related to the physical aspects of the mounting configuration such as the trace inductance and capacitor value.

An equivalent lumped circuit model is developed for analysis purposes in Section 2 from the physical configuration of the PCB. Simplifying approximations are made to obtain analytical expressions for the series and parallel resonance frequencies of added decoupling capacitors, in order to characterize the frequency range over which the capacitor is behaving as ideal, and that for which it deviates from ideal. The effects of trace inductance and capacitor size on the response of the nonideal element will be apparent from this simple analysis. The method for measuring the trace inductance and PCB response to decoupling capacitors will be described in Section 3. Measured results will be given in Section 4. The measurements include results for: 1) the effective frequency range of surface mount decoupling capacitors; 2) inductances of surface-mount capacitor interconnections to the PCB power bus from PCBs designed by Boeing (CAS); 3) inductances of surface-mount capacitor interconnect configurations for a test board designed for this study; 4) the variation of the PCB response with frequency as a function of interconnect inductance and surface-mount capacitance values; and, 5) the independence of the PCB response up to several hundred megahertz with variation in the location of the decoupling capacitor. Conclusions are given, and recommendations presented in Section 5.

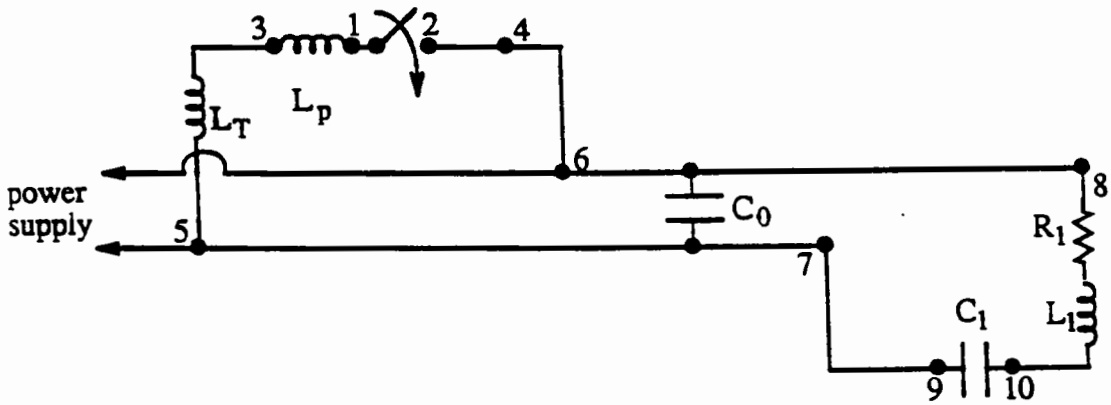
2 Equivalent Circuit Model

Measurements of the frequency response of the power bus for 7" × 8" unpopulated PCBs show that the power bus exhibits the frequency behavior of a (parallel plate) capacitor (see for example Figure 7). If a decoupling capacitor is added and placed at various locations on the PCB with identical interconnect geometry (series inductance and resistance), the measured response is identical up to 200 MHz at all locations. The PCB with added decoupling capacitors can then be modeled as a lumped circuit element for frequencies below approximately 200 MHz. The elements of the equivalent circuit can be related to physical aspects of the PCB as shown in Figure 1. The switching digital module is modeled simply as a switch which closes and opens. When the switch closes, a transient current is drawn through the digital circuit module. For many devices the rise time of the current is of the order of nanoseconds and is the source of high frequency noise or voltage ripple on the power bus. The lumped elements of the equivalent circuit model are the interplane capacitance of the PCB power bus C_o, the surface-mount decoupling capacitor C_1, the inductance of the loop formed by the traces and vias connecting C_1 to the power bus L_1, the inductance internal to the IC package L_p, and the partial inductance of the loop and traces that connect the IC package to the power bus L_T.

A general equivalent circuit model with n decoupling capacitors added is shown in Figure 2(a). The model does not include lumped elements for the power bus. For power and return plane widths greater than 6" and a separation less than 10 $mils$, the inductance per unit length is less than 0.02 $\frac{nH}{cm}$, which is negligible relative to the inductance of the surface mount capacitor interconnects. The series resistance and inductance associated with the traces and vias are a function of geometry and will in general vary from $20 - 100\ m\Omega$ for the series resistance, and $2 - 10\ nH$ for the series inductance. In any given design, several different values of capacitance might typically be used. While this equivalent circuit is easily analyzed using the computer, e.g., with SPICE, simple analytical expressions result from which insight can be gained by making some simplifying assumptions. If all capacitance and

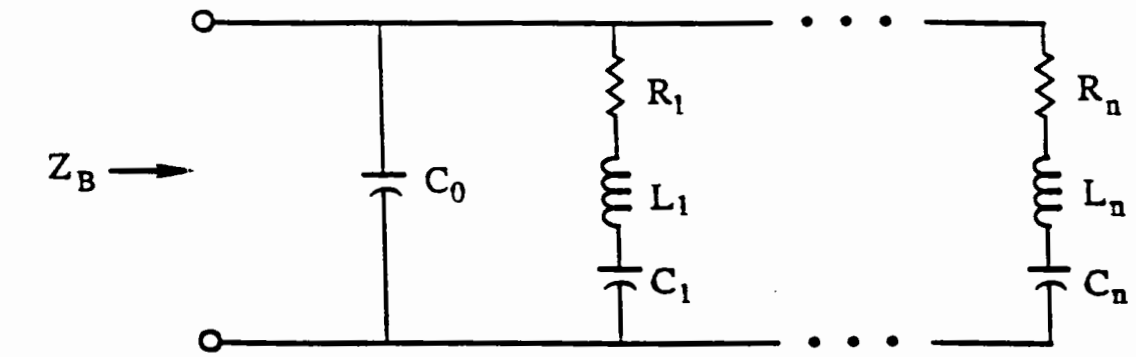


(a)



(b)

Figure 1: (a) Physical configuration and (b) equivalent circuit for an integrated circuit and decoupling capacitor mounted on a PCB.



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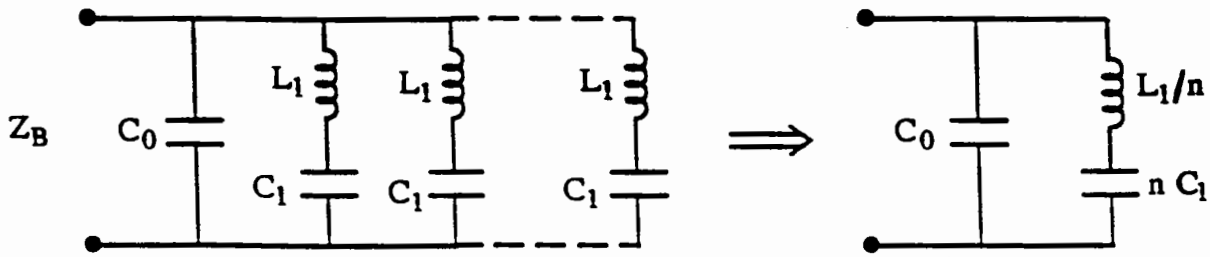


(b)

Figure 2: Lumped circuit model for n decoupling capacitors added to a PCB. (a) General model. (b) Simplified model.

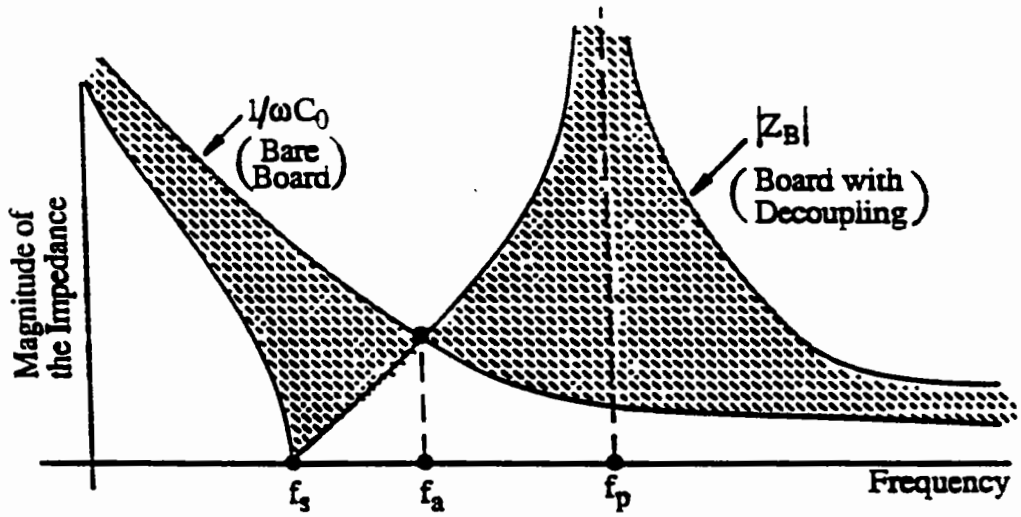


Figure 3: General | Z_B | versus frequency for the simplified model of Figure 2(b).

inductance values are assumed equal, and the resistance is neglected as shown in Figure 2(b), the PCB impedance is given by

$$Z_B = \frac{j\left(\omega\frac{L_1}{n} - \frac{1}{\omega n C_1}\right)}{1 - \omega C_o\left(\frac{\omega L_1}{n} - \frac{1}{\omega n C_1}\right)} \tag{1}$$

This is compared to the ideal PCB impedance if pure capacitance (without interconnect inductance and resistance) could be added resulting in

$$Z = \frac{1}{j\omega(nC_1 + C_o)} \tag{2}$$

The board impedance given in Eq. 1 results in zeros of impedance at the series resonance frequency

$$f_s = \frac{1}{2\pi\sqrt{L_1 C_1}} \tag{3}$$

and infinite impedance at the parallel resonance frequency

$$f_p = f_s\sqrt{1 + \frac{nC_1}{C_o}} \tag{4}$$

The generic impedance response for Eq. 1 is shown in Figure 3. It is seen for frequencies below the series resonance frequency that the decoupling capacitors behave as capacitors with an impedance of $Z \sim \frac{1}{j\omega(nC_1+C_o)}$. For frequencies near the series resonce frequency f_s, the impedance given by Eq. 1 is actually less than the ideal capacitor response of Eq. 2. However, at frequencies higher than f_s, the decoupling capacitors begin to look inductive as a result of the interconnect inductance. Thus the decoupling capacitor is no longer behaving as a capacitor but an inductor at frequencies above the series resonance frequency. The frequency at which $| Z_B | = \frac{1}{\omega C_o}$ is given by

$$f_a = f_s\sqrt{1 + \frac{nC_1}{2C_o}} \tag{5}$$

For frequencies above f_a the added decoupling capacitor provides no decoupling. It is clear from this simple analysis that minimizing the series inductance of the decoupling capacitor connection is paramount to achieving the ideal capacitor behavior over the widest possible frequency range, which in the time domain corresponds to the ability to supply current-ly rapidly. Lowering the interconnect inductance increases the series resonance frequency, thereby extending the range of ideal capacitor behavior. The frequency range over which ideal capacitor behavior is obtained can be increased by: 1) lowering the interconnect inductance and thereby increasing the series resonance frequency (with f_p likewise increasing), and 2) increasing the parallel resonance frequency by increasing n, the number of decoupling capacitors. Increasing n effectively divides the equivalent inductance of the interconnects by n.

3 Experimental Method

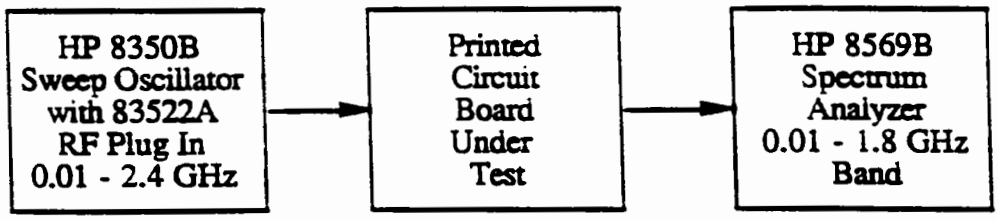
Two different test configurations were used in the course of this study for measuring the magnitude of the impedance of the PCB. Initially, a sweep oscillator and spectrum analyzer were employed as shown in Figure 4(a). The sweep oscillator and spectrum analyzer were connected to the PCB power plane through semi-rigid, 0.085", coaxial-cable probes, which were soldered to decoupling capacitor bonding pads. The center conductor of the coaxial cable was connected to the return plane and the outer shield was connected to the power plane as shown in Figure 4(b). For a DC power bus capacitance of $C_o = 3\ nF$, which was typical of the boards tested, $\mid Z \mid = \frac{1}{\omega C_o} = 5.3\ \Omega$ at $10\ MHz$. For frequencies above $10\ MHz$ then, $\mid Z \mid \ll 50\ \Omega$, and the sweep oscillator provides a constant current versus frequency through the PCB impedance. The voltage to the spectrum analyzer is then directly proportional to the magnitude of the PCB power bus impedance as shown in Figure 4(c). The series inductance shown in Figure 4(c) is the inductance resulting from the coaxial cable probes connected to the decoupling capacitor bonding pads of Board #1 and Board #2 (see Section 4). Typical values of inductance were $3-5\ nH$ for this connection. Results with this measurement system were easily repeatable and did not depend on the dressing of the test cables. The dynamic range of the system was $80\ dB$. The low frequency end of the measurement range with this test system was limited by the sweep oscillator which provided power only as low as $10\ MHz$.

An HP8753C vector network analyzer was also employed for the impedance measurements. The two ports of the network analyzer were connected to the two coaxial cable test probes attached to the PCB. In this case the PCB impedance can be directly related to the measured S_{21} between the attached coaxial cable probes as

$$S_{21} = \frac{Z_B}{Z_B + \frac{1}{2}Z_o} \tag{6}$$

where Z_B is the PCB impedance, and $Z_o = 50\ \Omega$ is the characteristic impedance of the measurement system. For $Z_B \ll Z_o$, which is generally the case, except possibly at the parallel resonance frequencies,

$$\mid S_{21} \mid \simeq \frac{\mid Z_B \mid}{25} = (\mid Z_B \mid -28)\ dB \tag{7}$$



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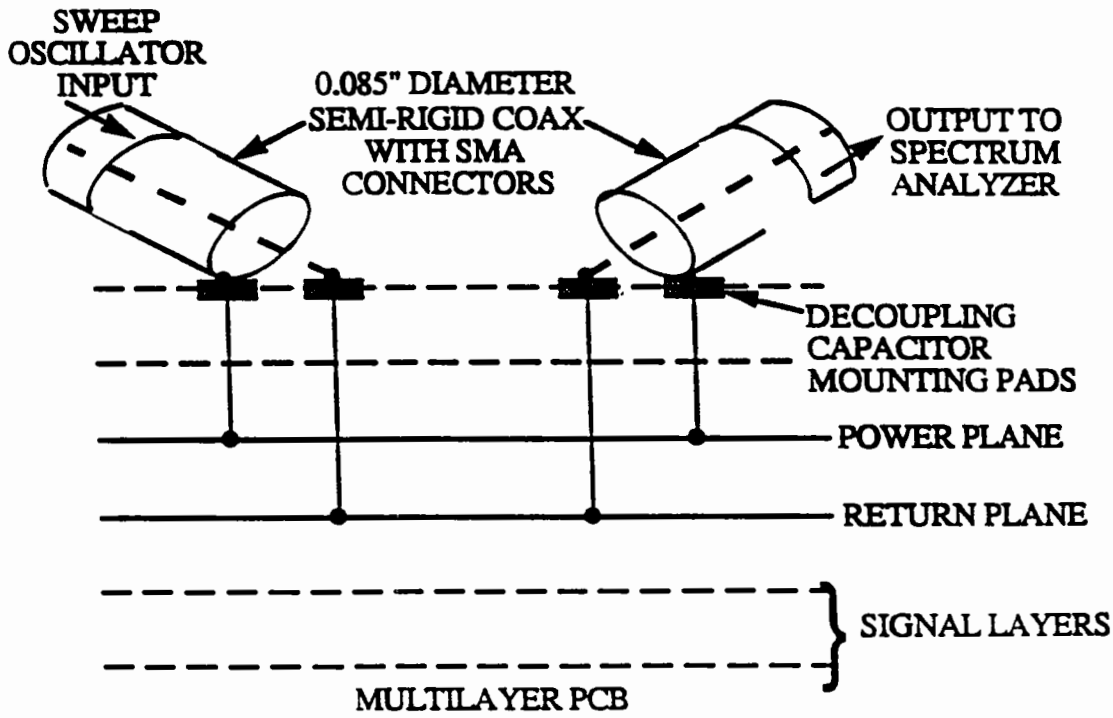

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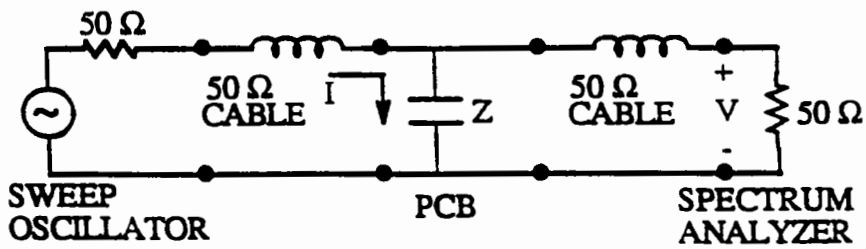


(c)

Figure 4: Test configuration for measuring $| V_B |\sim| Z_B |$ with the spectrum analyzer and sweep oscillator. (a) Block diagram of the test configuration, (b) connection of test probes to the power bus, and (c) equivalent circuit of the test configuration.

In addition to measuring the PCB impedance with the HP8753C, the series resistance of the decoupling capacitor interconnects can be obtained from measurements of S_{11} as described in Section 4.

4 Measured Results

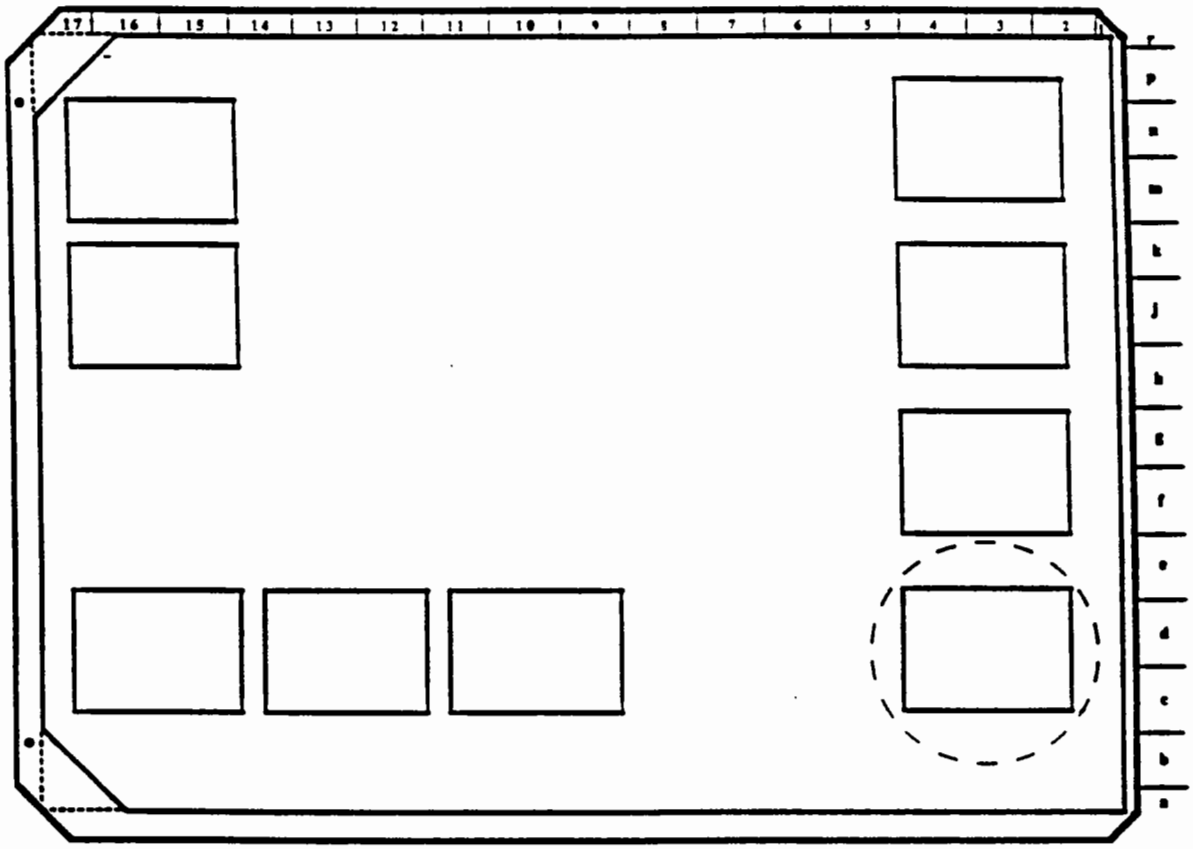
The test systems described in the previous section were employed to measure the inductance and resistance of typical interconnects, and the magnitude of the PCB impedance. The tests were performed primarily on two PCB designs provided by Boeing, and a third board designed and manufactured specifically for this study. The board designations used in the remainder of the report are:

- Board #1: 10 layer, 8" × 9" board # 906-30003-9015B
- Board #2: 6 layer, 8" × 10", board # 906-60072-9005A
- Board #3: 7" × 8"

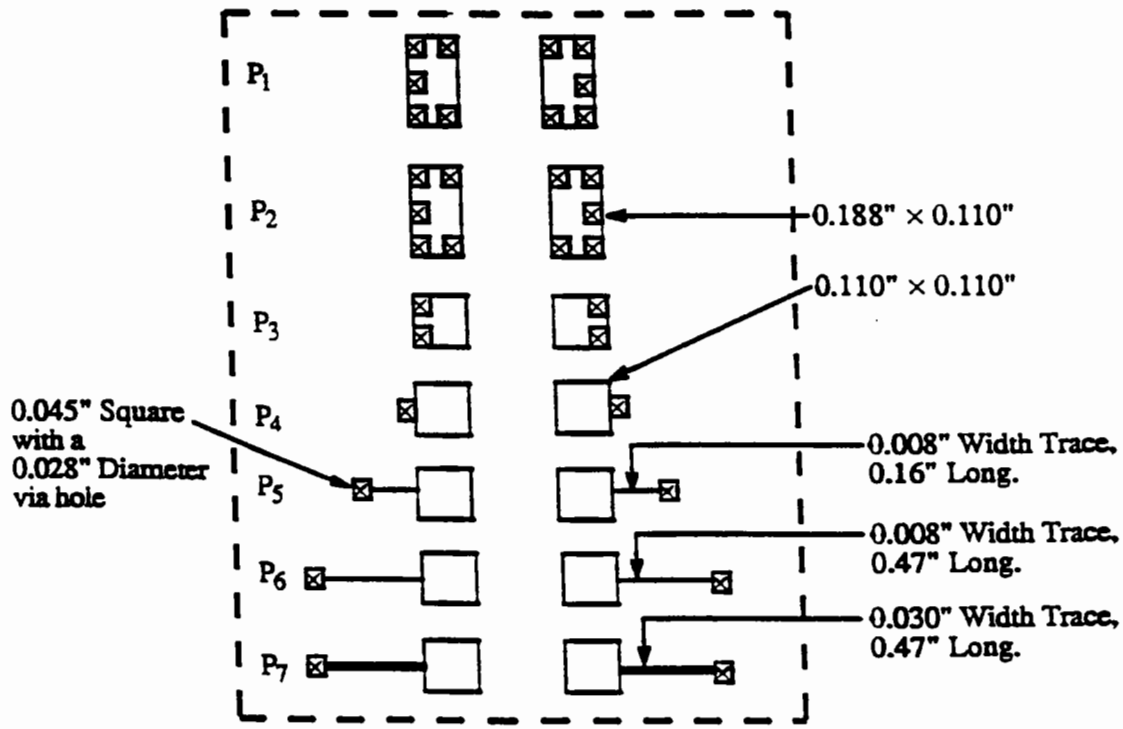
Board #3 consisted of a single power and return plane and 63 bonding pads for surface-mount capacitors connected to the power bus through six different geometric configurations of varying inductance and resistance, and distributed over the board as shown in Figure 5.

The measured magnitude of the board impedance for a board with no decoupling capacitors or devices is compared to an unpowered, fully populated board (different PCBs, but of the same type) in Figure 6. It is seen that $\mid Z_B \mid$ differs little in the two cases for frequencies above several hundred megahertz. The range of effectiveness for surface-mount capacitors is then limited to frequencies below several hundred megahertz. The series inductance associated with the surface-mount decoupling capacitor interconnect renders the capacitor ineffective at higher frequencies. A quarter-wavelength transmission-line resonance is observed in the magnitude of the impedance of the bare board at approximately 200 MHz. The loading effects of the fully populated board tend to mitigate resonances as can be observed from Figure 6. The first resonance of Board #3 was measured to be approximately 350 MHz, however, the magnitude of the impedance differed little from that expected for a parallel plate capacitor of $\mid Z_B \mid = \frac{1}{\omega C}$ up to 200 MHz. The measurements thus focused on the frequency range $10 - 200$ MHz.

The primary concern for effective decoupling in the frequency range $10 - 200$ MHz using surface-mount capacitors is minimizing the inductance of the traces and vias by which the capacitor is connected to the power bus. It is this inductance together with the value of capacitance that limits the rise time of the current that can be drawn from the decoupling capacitor. In the frequency domain, the interconnect inductance in series with the decoupling capacitor, together with the interplane board capacitance C_o, for all added decoupling capacitors as illustrated in Figure 2(a), is manifested as series and parallel resonances corresponding to zeros and poles, respectively, in the magnitude of the board impedance. The rise time of the current to an IC module is limited by the pole frequencies of the board response together with the internal impedance of the module.



(a)



(b)

Figure 5: Geometry of Board #3. (a) Board layout. (b) Dimensions of the decoupling capacitor interconnects.

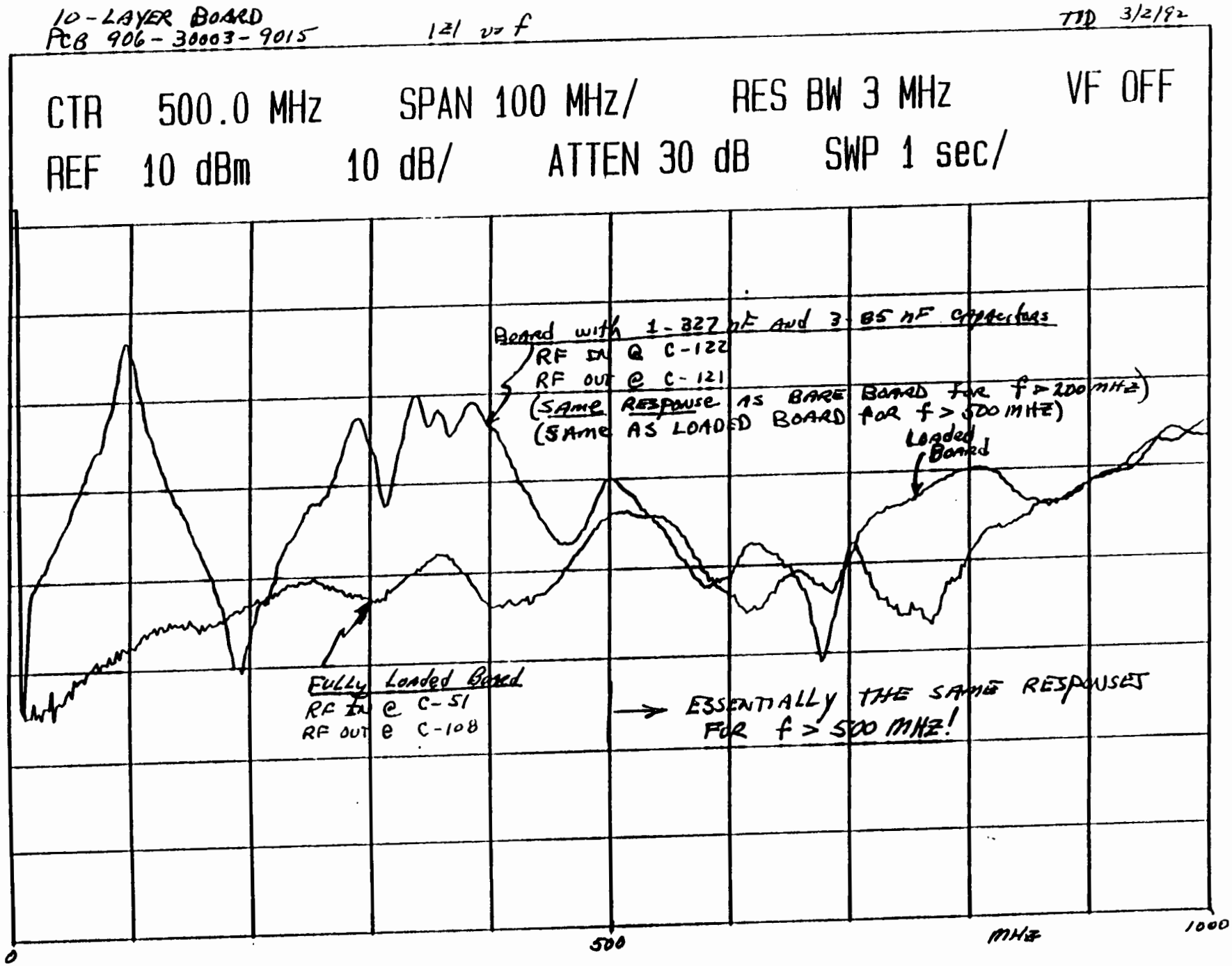


Figure 6: Comparison of $|V_B| \sim |Z_B|$ for a fully populated PCB (unpowered) to a PCB with no active or passive devices attached

The parallel planes of the power bus behave like a lumped capacitor for the measured frequency range $10-200\ MHz$. The measured magnitude of the impedance $\mid Z_B \mid$ for Board #3 is compared in Figure 7 with several points plotted for the ideal response of a lumped capacitor $\mid Z_B \mid = \frac{1}{\omega C}$. It is seen that below 200 MHz the unpopulated board (no devices or capacitors) behaves as a lumped capacitance. The deviation of the measured $\mid Z_B \mid = \frac{1}{\omega C_o}$ at 200 MHz is a result of the distributed board resonance at 350 MHz. The capacitance of the power bus of several PCBs designed and constructed by Boeing were measured with an RLC meter and were typically found to be in the range of 3 nF. For Board #3 in which the power and return planes were on adjacent layers and not laterally divided (e.g. into analog and digital regions), the measured power bus capacitance was 15.3 nF.

The significant capacitance of the PCB power bus provided a direct and straightforward means of measuring the inductance and resistance associated with the traces and vias connecting the surface-mount capacitors to the power bus. The equivalent lumped circuit model for a short placed across the mounting pads of a decoupling capacitor is shown in Figure 8. The series resistance R is sufficiently small so that the parallel resonance of the circuit is given by $f_p = \frac{1}{2\pi\sqrt{LC_o}}$. The trace inductance can thus be obtained by measuring the parallel resonance frequency. A typical measurement made with the HP8753C network analyzer is shown in Figure 9. The series inductance of surface mount decoupling capacitors was measured at several mounting locations for Board #1 and Board #2. The results are tabulated in Table 1. It is observed that the minimum inductance measured for these circuit designs was 2.6 nH and the maximum value was 7.7 nH. For other Boeing designed boards investigated, the values of inductance ranged from $2.5-10\ nH$. The average inductance is observed to be in the range of $4-5\ nH$. These values of inductance limit the frequency range over which effective decoupling is achieved to less than 100 MHz. The measurements of Table 1 were made with the spectrum analyzer and sweep oscillator system described in Section 3.

The series inductance and resistance of the decoupling capacitor interconnects was also measured for Board #3, and are given in Table 2 for the six different geometries shown in Figure 5. These measurement were made using the HP8753C network analyzer. The inductance was obtained from the parallel resonance frequency as discussed above. The series resistance is obtained from measurements of S_{11}. The impedance seen looking into the circuit shown in Figure 8 is entirely real at the parallel resonance frequency and can be obtained directly from the measurements. This resistance is the equivalent parallel circuit resistance which can be easily converted to the desired series resistance using circuit transformations. The trends indicated in Table 2 are as expected, *viz.*, inductance and resistance are highest for long and narrow traces. The bonding pads of Board #3 are larger (more surface area) than typically used so that low inductance bonding configurations using multiple via holes could be studied. The difference that the larger bonding pads make in the measured inductance versus conventional bonding pads is small for the configurations P_5, P_6, and P_7 (see Figure 5). A significant result in Table 2 is the 0.61 nH inductance measured for connection P_2. Minimizing the series inductance is paramount for effective addition of surface mount decoupling capacitors to the PCB. While the specific geometry of P_2 that was constructed and tested may present manufacturing difficulties, a multiple via bonding connection having an equivalent series inductance less than 1 nH, which can be manufactured within the framework of existing processes, is conceivable.

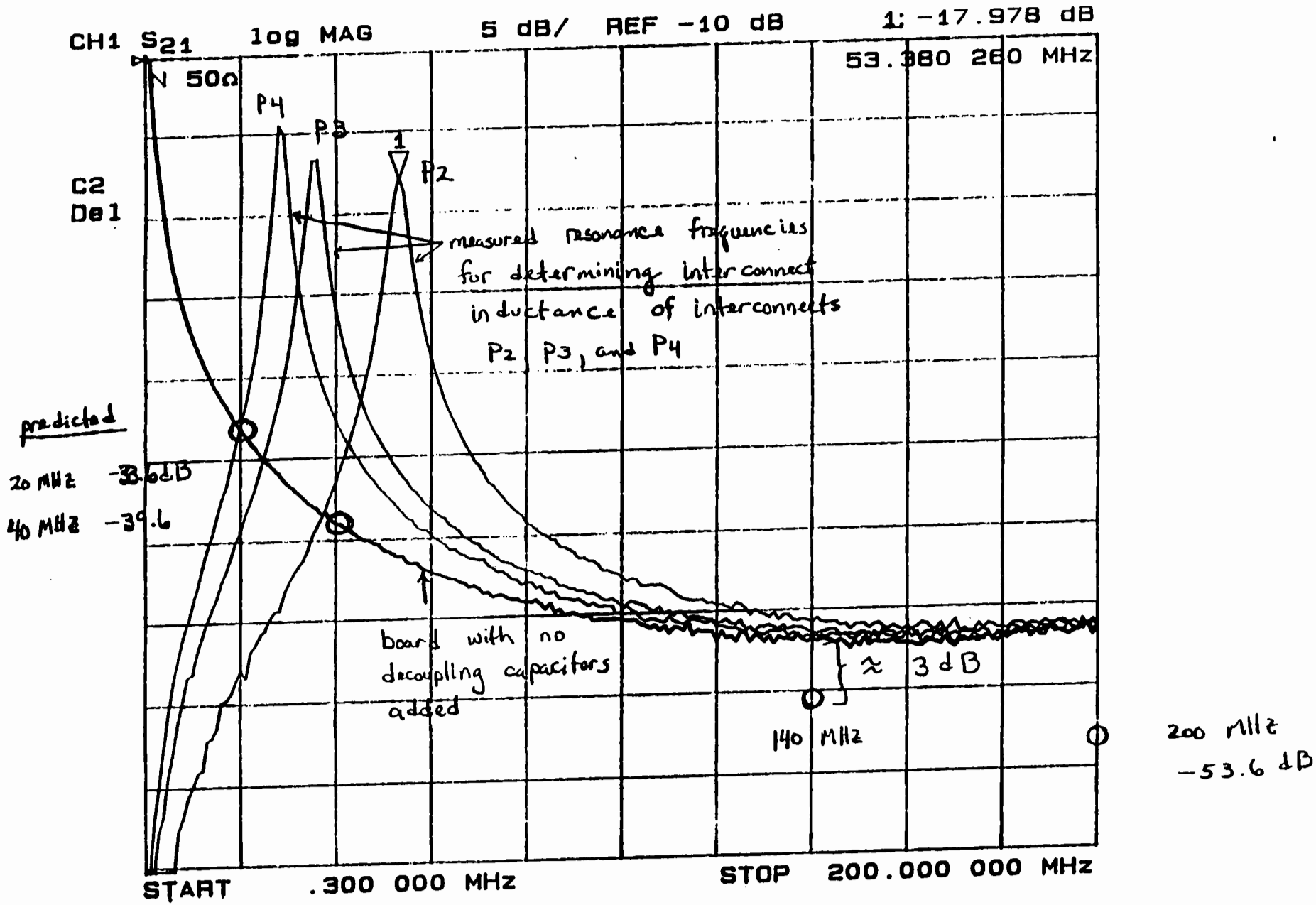


Figure 7: Measured | S_{21} | for Board #3 with no attached decoupling capacitors. Plotted points are calculated values for an ideal capacitor with $C_o = 15.3\ nF$.

Table 1: Interconnect Inductance Values for Board #1 and Board #2

10 LAYER BOARD		6 LAYER BOARD	
CAPACITOR LOCATION	INDUCTANCE (nH)	CAPACITOR LOCATION	INDUCTANCE (nH)
C-51	2.6	J-9	4.2
C-101	4.7	K-11	3.8
C-102	3.2	M-7	4.0
C-108	2.7	M-8	4.0
C-110	6.8	N-12	5.4
C-115	3.6	N-13	4.4
C-116	6.4	N-15	7.7
C-117	5.3	N-16	3.4
C-118	4.2		
C-119	3.4		
C-124	3.4		
C-155	4.5		
C-197	5.4		

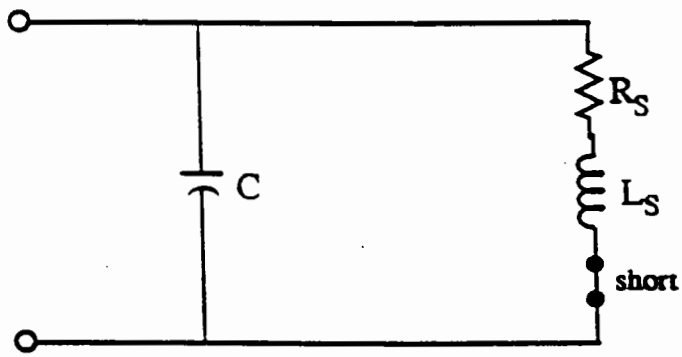


Figure 8: Equivalent circuit for measuring the series inductance of the surface mount capacitor interconnects.

Table 2: Interconnect Inductance Values for Board #3

CAPACITOR INTERCONNECT	R_s (mΩ)	L_s (nH)
P_2	12	0.61
P_3	17	1.32
P_4	22	2.00
P_5	54	7.11
P_6	95	15.7
P_7	53	10.3

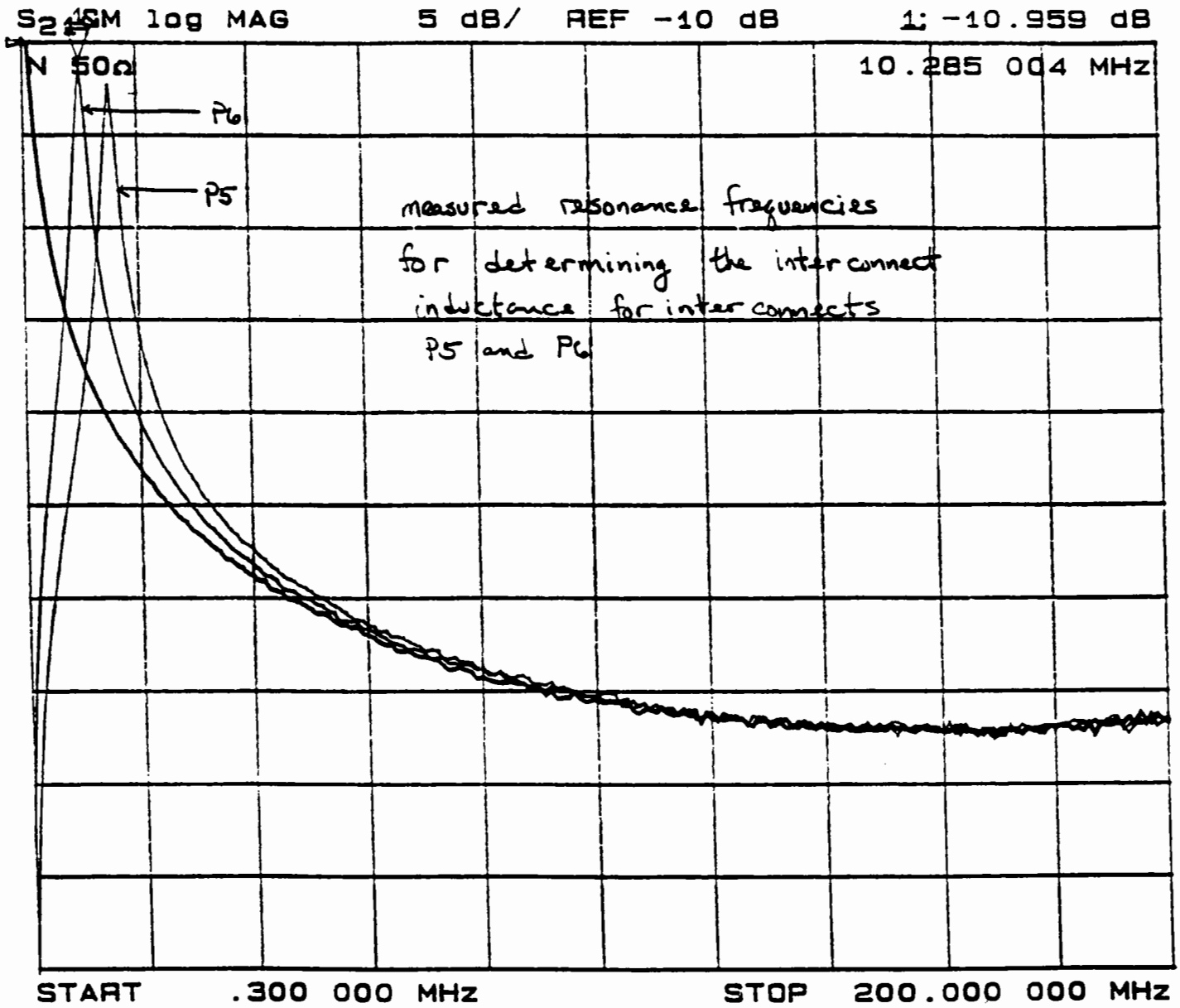


Figure 9: A typical measurement of $|\ S_{21}\ |$ for determining the interconnect inductance of surface-mount capacitor connections.

The effect of the series inductance of a surface-mount decoupling capacitor on the magnitude of the impedance of the PCB is shown in Figure 10 for Board #1, and Figure 11 and Figure 12 for Board #3. The results for Board #1 display a resonance phenomena at approximately 75 MHz. This was the case when measurements were conducted with the spectrum analyzer and sweep oscillator system as well as with the network analyzer. The exact source of this phenomena is unknown but believed to be a measurement artifact associated with the high inductance connections of the semi-rigid coaxial cable probes to the board. The connections to the power bus were made through available decoupling capacitor interconnects which averaged $4-5\ nH$ for Board #1 and Board #2. The connection to the power bus on Board #3 was made at P_2 with a measured inductance of 0.61 nH and this phenomena was not observed.

The effect of the series inductance on the series and parallel resonance frequencies of the magnitude of the board response $\mid Z_B \mid$ is clear. Larger values of inductance reduce the series and parallel resonances. This limits the frequency range over which the surface mount capacitor behaves as an ideal circuit element. For frequencies below approximately the parallel resonance frequency (or pole of Z_B) the capacitor has an ideal impedance of $\frac{1}{j\omega C}$ and the magnitude of the board impedance is,

$$\mid Z_B \mid \simeq \frac{1}{\omega (C_o + C_1)} \tag{8}$$

however, above the parallel resonance frequency $\mid Z_B \mid > \frac{1}{\omega C_o}$ and the series inductance of the capacitor interconnect dominates the frequency response rendering the added decoupling capacitor ineffective. The pole frequency thus determines the maximum frequency at which surface mount decoupling capacitors are effective, and this frequency is determined for a given value of capacitance by the inductance of the interconnect. The pole frequency can be moved to higher frequencies by lowering the capacitor interconnect inductance, or as indicated by the simple analysis given in Section 2, by adding multiple capacitors in parallel (for the same total capacitance) through the same inductance interconnects to effectively divide down the inductance. Thus, a larger value of capacitance through a smaller inductance is as effective at high frequencies as several smaller value capacitors (for the same total capacitance) connected through a larger inductance path if the LC product remains the same. This is illustrated in Figure 13. First, three 3.3 nF capacitors were connected to Board #3 through 7.11 nH inductance connections (see P_5 on Figure 5) and S_{21} measured ($\mid S_{21} \mid \simeq (\mid Z_B \mid -28) dB$). Likewise S_{21} was measured for a 10 nF capacitor connected through a 2.0 nH inductance connection. The LC product is not exactly identical, being $23.5 \times 10^{-18}\ s^2$ in one case, and $20 \times 10^{-18}\ s^2$ in the other, however, given this difference, the board response is nearly the same. The calculated series resonance of 32.8 MHz for the 3.3 nF capacitors agrees well with the measured value of 31.5 MHz. Likewise the calculated and measured values for the 10 nF capacitor agree well. Thus, minimizing the interconnect inductance of surface-mount decoupling capacitors enables the use of fewer, larger values of capacitance for the same decoupling.

Conventional thought suggests that decoupling capacitors be placed at or as close as possible to the integrated circuit package, which may have origins in the use of high inductance power traces as opposed to low inductance power planes. In practice this can be difficult as can be inferred from some of the larger values of decoupling capacitor interconnect inductance measured on Board #1 and Board #2. However, over the frequency range

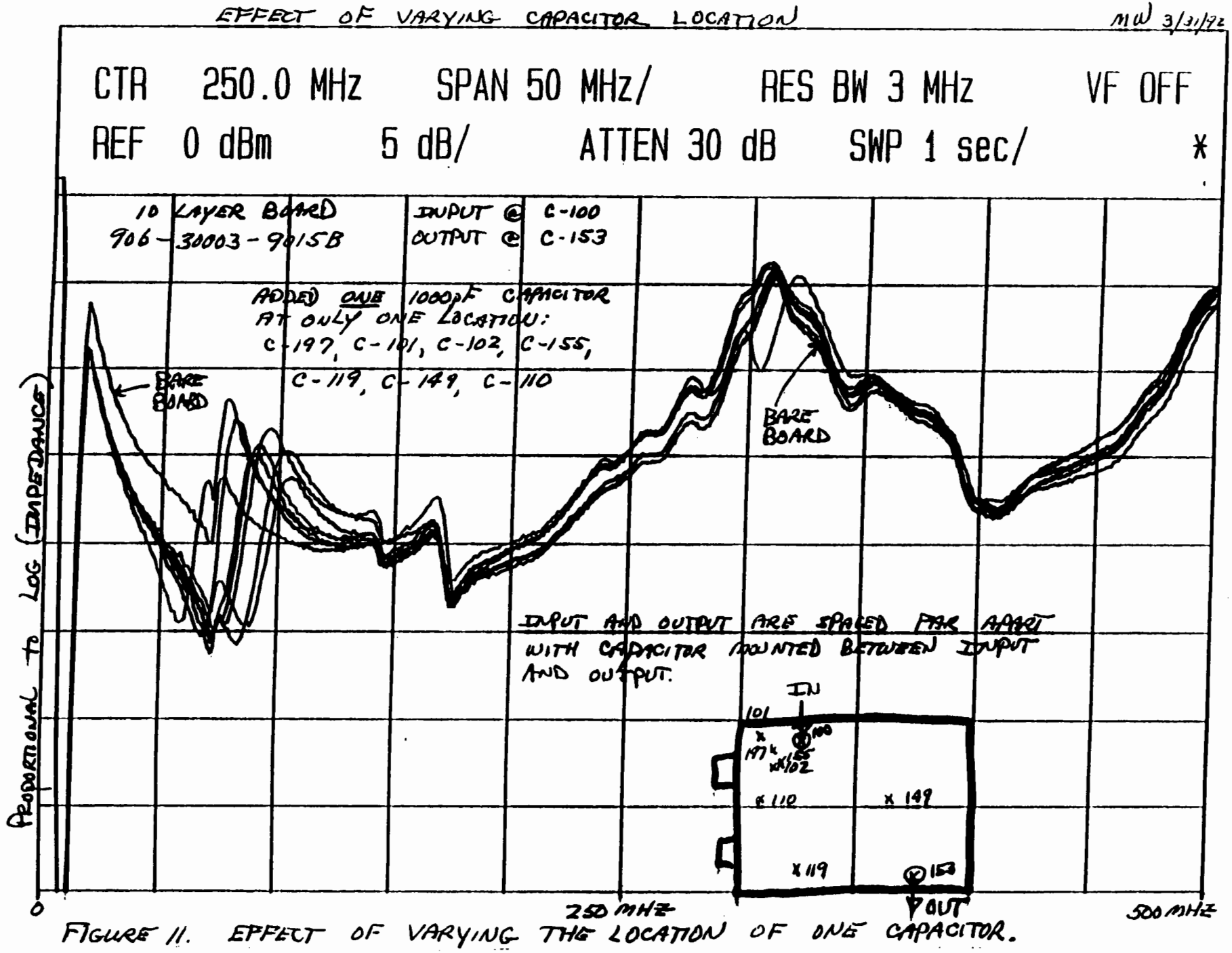


Figure 10: Effect of trace inductance on the measured $|V_B| \sim |Z_B|$ for a single added capacitor to Board #1 (see Table 1 for inductance values of different locations).

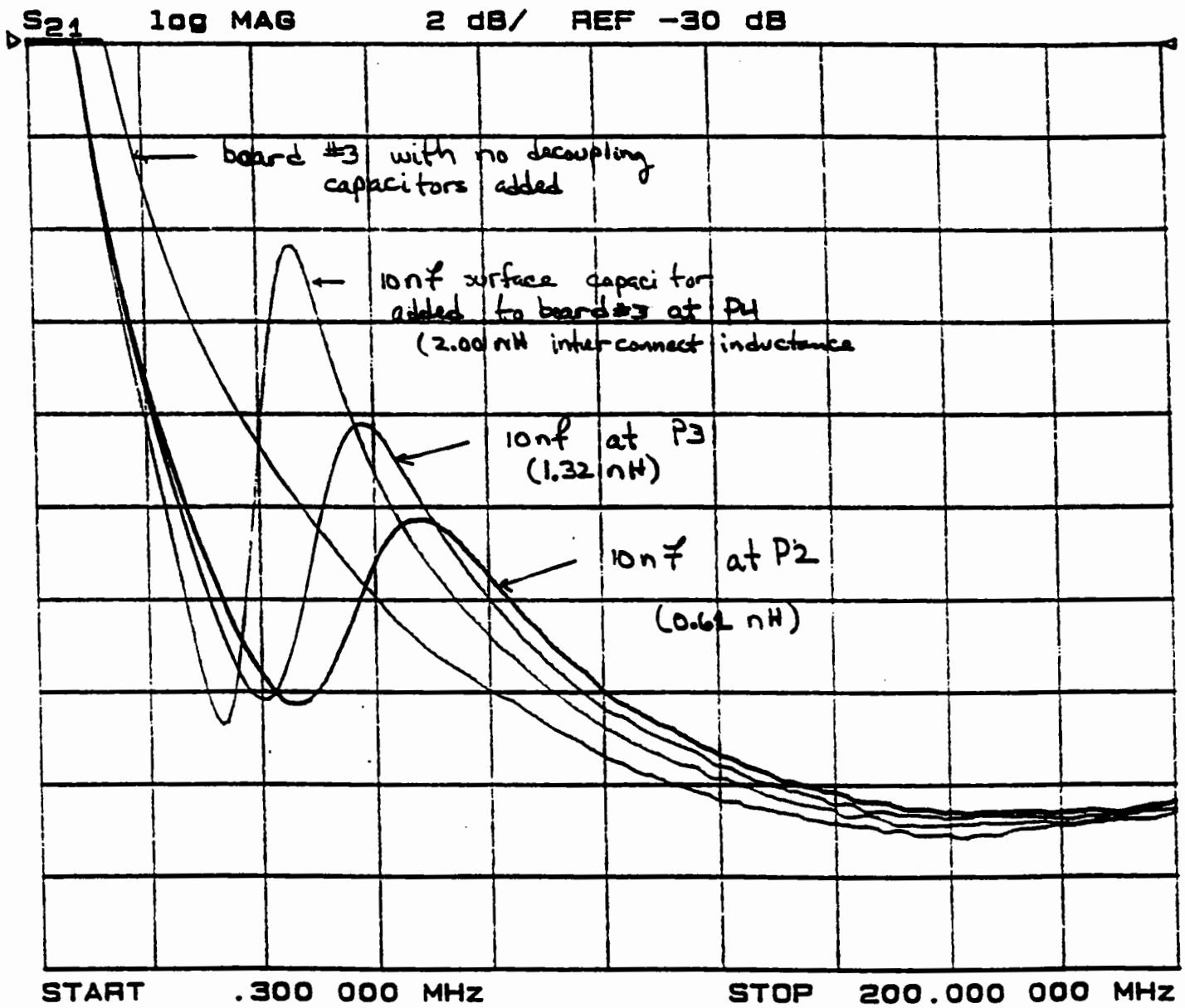


Figure 11: Effect of trace inductance on the measured $|\ S_{21}\ |$ with a single added decoupling capacitor for Board #3 at positions P_2, P_3, and P_4.

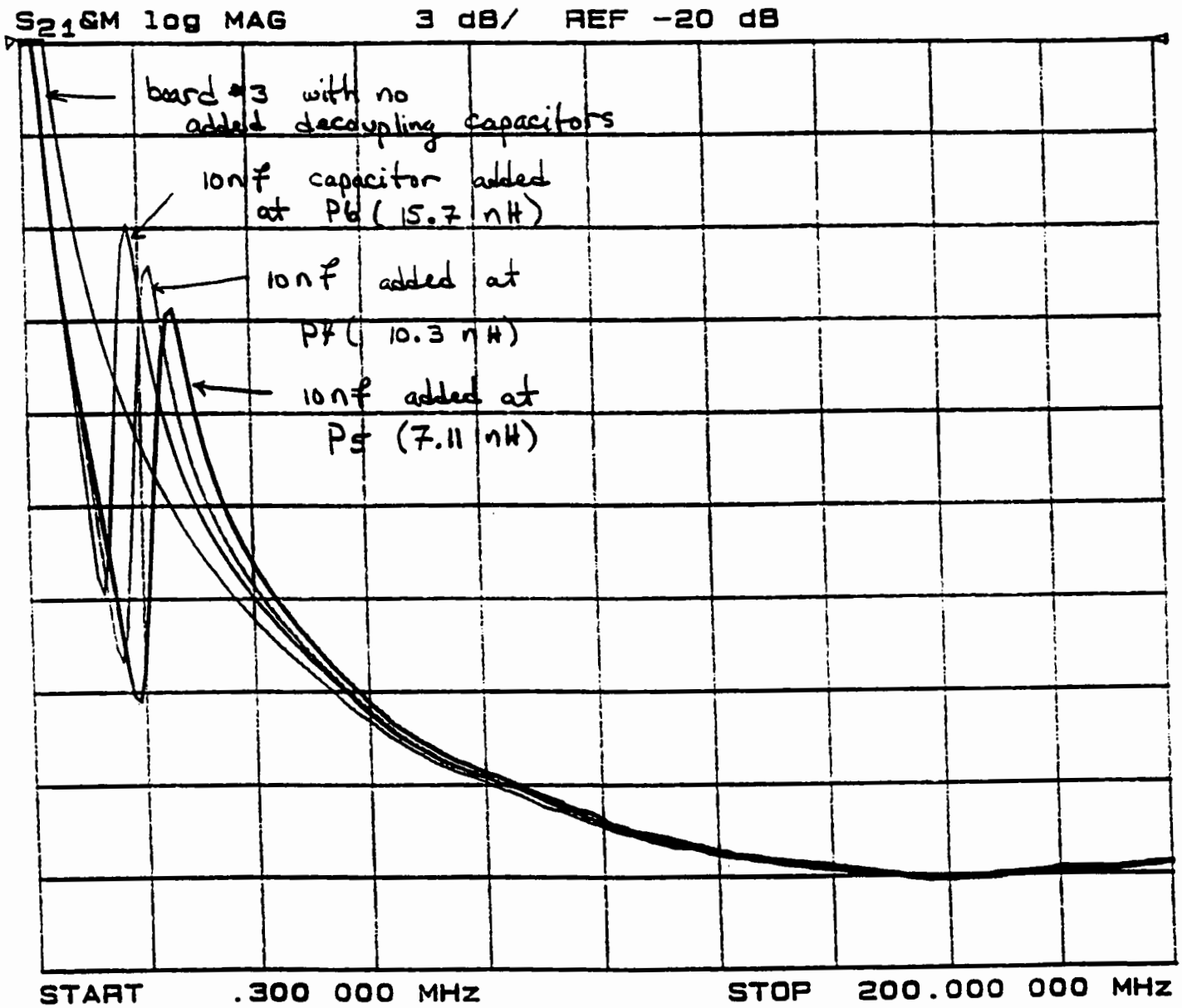


Figure 12: Effect of trace inductance on the measured $| S_{21} |$ with a single added decoupling capacitor for Board #3 at positions P_5, P_6, and P_7.

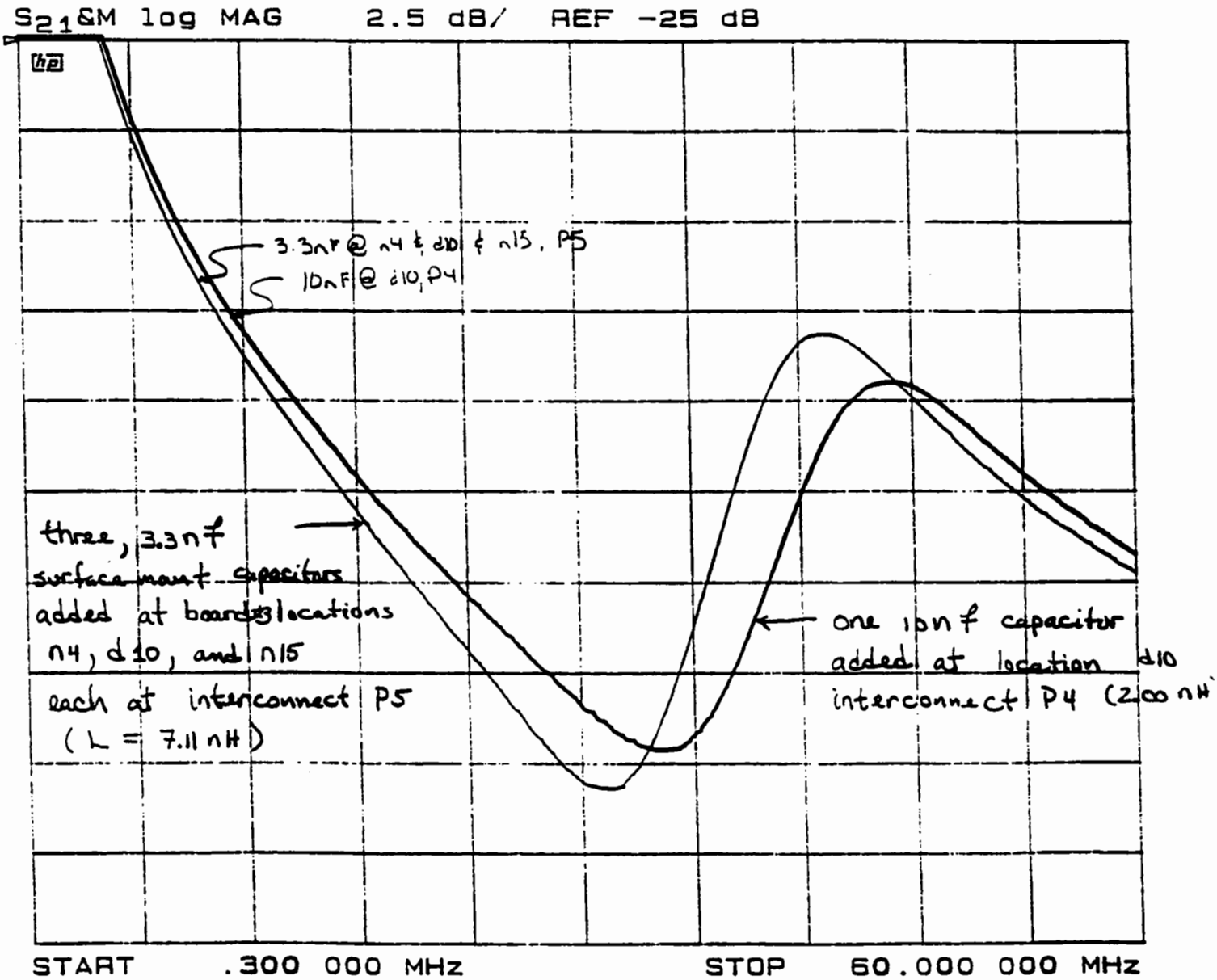


Figure 13: $| S_{21} |$ measurements for one 10 nF capacitor connected through P_4, compared with three 3.3 nF capacitors connected through P_5 (at locations $n4$, $d10$, and $n15$).

at which the $| Z_B |$ is behaving as a lumped circuit element. $| Z_B |$ should not depend on the location of the decoupling capacitor. This additional freedom of placement may allow for a (manufacturable) multiple-via connection to the power bus. This connection can be placed where the additional area required for such a configuration is available, whereas the necessary area may often not be available in the immediate vicinity of the device. The independence of $| Z_B |$ on the location of the decoupling capacitor is illustrated from $| S_{21} |$ measurements for the frequency range $0.3 - 200\ MHz$ in Figure 14 for a $10\ nF$ decoupling capacitor placed at the five positions $n15$, $k15$, $d13$, $d4$, and $j4$ (see Figure 5) with the test probes located at $d10$ and $d16$. The capacitor was connected to the power bus through traces having a measured inductance of $7.11\ nH$. The small variation in two of the traces is a result of using two different capacitors for the five curves.

The high frequency currents ($10 - 200\ MHz$) supplied by decoupling capacitors are confined to the inner surfaces of the power bus. The skin depth for copper at 10, 100, and 200 MHz is 20.9, 6.6, and 4.6 μm, respectively. The metallization thickness of 1 $oz.$ copper cladding is 1.38 $mils \simeq 35.9\ \mu m$. Thus, at 10 MHz the copper thickness is nearly two skin depths and over five skin depths at 100 MHz. If the power and return planes are placed on adjacent layers, which is desirable for a low inductance power bus, the high frequency currents are confined to the power bus. Another potential mechanism for undesirable coupling of the current drawn from decoupling capacitors to IC modules under which the current may travel is magnetic field coupling. However, for low inductance power planes, the mutual inductance is small and the coupling is negligible.

5 Recommendations

The recommendations for applying surface-mount decoupling capacitors to PCBs based on the analytical and experimental studies presented are:

- Minimal inductance interconnects are essential for achieving optimal performance from surface-mount decoupling capacitors. Sub-nanohenry interconnects should be pursued in the context of present manufacturing techniques.
- Decoupling capacitors should be positioned in an area that will allow minimal inductance connections to the power bus.
- The interplane capacitance of the PCB power bus should be maximized. This capacitance is the most effective means of improving high frequency decoupling. Maximizing the interplane capacitance also serves to minimize the inductance of the PCB power bus which is desirable.

As indicated by the previous discussion, effective high frequency decoupling (ten megahertz to several hundred megahertz) hinges on minimizing the inductance of the interconnects through which surface-mount capacitors are connected to the DC power bus. For current design and manufacturing practices within the Boeing corporation, as illustrated by measurements on Board #1 and Board #2, it is possible to achieve minimal inductance connections of approximately $2.5\ nH$. Many important considerations compete for the attention of a circuit designer, not the least of which is the placement of often a large number

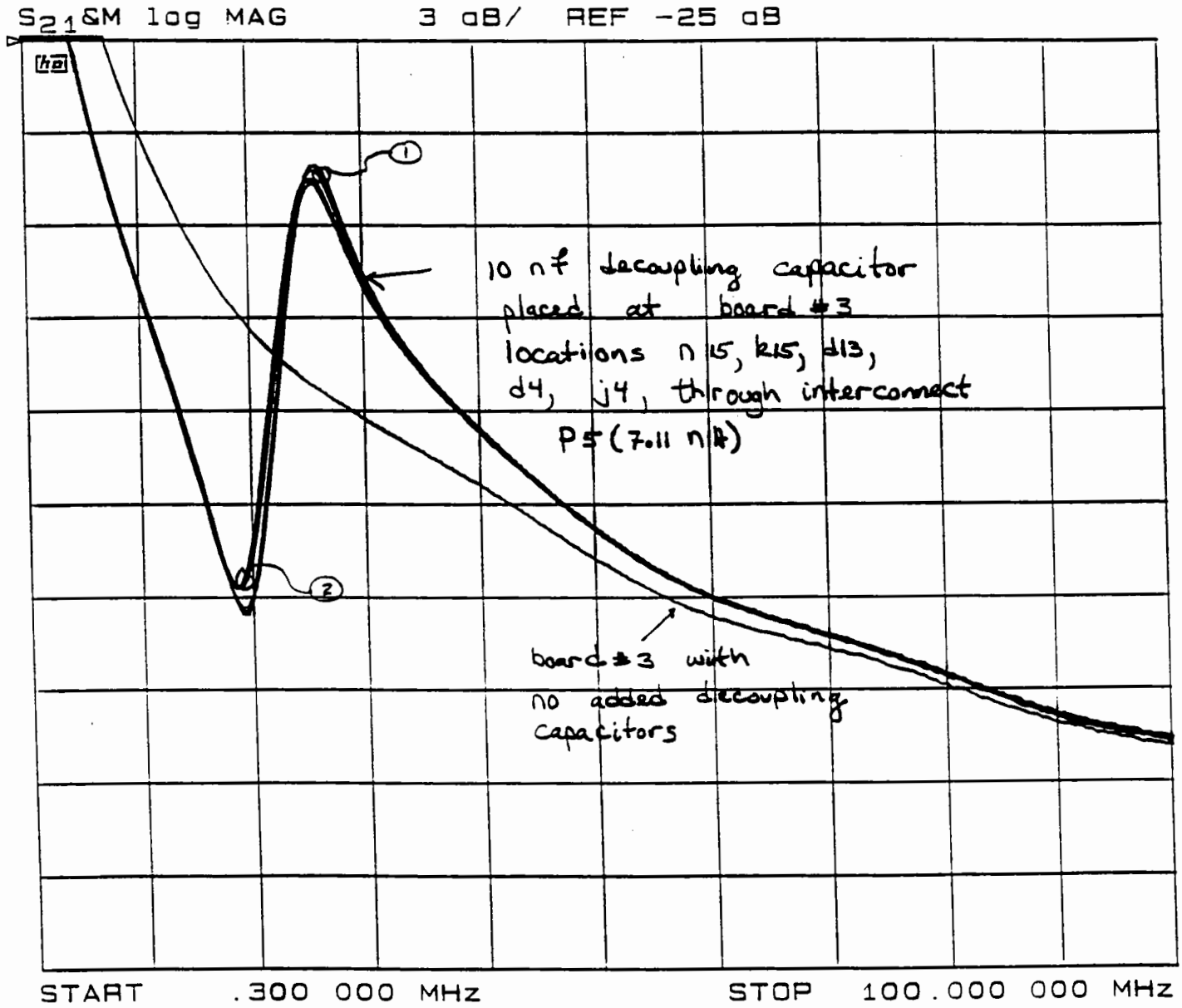


Figure 14: Measured $|S_{21}|$ for a 10 nF capacitor at different board locations (see text) connected through the same trace and via-hole inductance.

of interconnected components on a seemingly small board. However, maintaining the voltage ripple on the DC power bus within device manufacturer specifications to prevent faulty switching, through the proper addition of decoupling capacitors, is essential to ensure that the circuit functions as designed. It is recommended that the addition of surface-mount decoupling capacitors to the PCB through the lowest possible inductance connections be a primary concern. With no change in current Boeing manufacturing and design practices this has been measured to be approximately 2.5 nH. If space considerations preclude such connections directly at the IC module, placing the decoupling capacitor in the near vicinity of the IC module, within approximately $3 - 5$ cm of the device is sufficient.

Since the interconnect inductance through which the surface-mount decoupling capacitors are connected to the DC power bus is the limiting factor on the decoupling capacitors performing as ideal circuit elements, manufacturable, sub-nanohenry inductance connections (less than 1 nH) merit pursuance. It has been demonstrated in this study that sub-nanohenry inductance connections can be achieved with multiple via-hole connections. While the specific connection tested may not be within the repertoire of present manufacturing techniques, multiple via-hole connections should be investigated within present manufacturing constraints. A sub-nanohenry inductance connection will allow considerably fewer large value capacitors to be used with the same decoupling effectiveness as a greater number of smaller value capacitors (for the same total capacitance).

Finally, the interplane capcitance of the PCB power bus should be maximized. This capacitance is the best means for achieving high frequency decoupling. Maximizing the interplane capacitance of the PCB power bus also serves to lower the inductance of the bus. A low inductance power bus is essential for supplying fast rise-time currents. It is recommended that this be accomplished by placing the power and return planes on adjacent layers. This also serves to confine, to the power bus, high frequency (short rise time components) currents supplied by the decoupling capacitors to the IC module. In addition, placing the power and return planes on adjacent layers minimizes the mutual inductance between the power bus and loops coupling circuits to the power bus, circumventing interference with other circuits as discussed previously.

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