University of Missouri-Rolla
Electromagnetic Compatibility Laboratory

Title: Power Bus Decoupling on Multilayer Printed Circuit Boards

Report Number: TR94-8-023

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Abstract

Noise is introduced on the power bus of a standard multilayer printed circuit board by current drawn to a switching digital module through the resistance and inductance associated with the interconnecting traces and vias. Decoupling strategies allow for minimizing this noise voltage to prevent false switching of other devices on the power bus. Lumped element models have been developed which represent the impedance characteristics of the power bus interplane capacitance and additional decoupling branches below the distributed resonances of the board. Model analysis and circuit simulations have been performed to test the models and investigate the effects of the various board elements on the power bus voltage. The results of these studies were used to determine more effective decoupling strategies.

Abstract

Noise is introduced on the power bus of a standard multilayer printed circuit board by current drawn to a switching digital module through the resistance and inductance associated with the interconnecting traces and vias. Decoupling strategies allow for minimizing this noise voltage to prevent false switching of other devices on the power bus. Lumped element models have been developed which represent the impedance characteristics of the power bus interplane capacitance and additional decoupling branches below the distributed resonances of the board. Model analysis and circuit simulations have been performed to test the models and investigate the effects of the various board elements on the power bus voltage. The results of these studies were used to determine more effective decoupling strategies.

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1: Introduction

On complex printed circuit boards (PCBs), the switching of a digital device causes a sudden change in the amount of charge demanded by the device. This charge is drawn through the resistance associated with the finite conductivity of the interconnecting traces and vias and the inductance associated with the loop formed by the interconnects. Thus, such currents can cause temporary changes in the power bus voltage. If large enough, this noise voltage can lead to false switching of other devices connected to the bus as well as radiated electromotive interference. Additional decoupling capacitors connected between power and ground help to supply some of this charge and thus stabilize the bus voltage. Proper application of these decoupling capacitors is investigated in this study, as is the effect of the interplane capacitance of the PCB.

A lumped-element model of the PCB was developed for use in PSPICE simulations. The noise voltage due to a typical low-to-high transition of the IC package exhibited frequency components identical to the poles of the power bus impedance. Thus, by minimizing the impedance between power and ground in the frequency domain, the corresponding voltage fluctuations were also minimized. Mathematical analyses and PSPICE simulations were performed to investigate the stabilizing effects of decoupling capacitors. These studies showed that the reduction of the power bus impedance could best be achieved by prudent addition of decoupling capacitors

so as to minimize the effect of the corresponding interconnect inductances and by maximization of the amount of "pure" interplane capacitance.

2: Equivalent Circuit Modeling

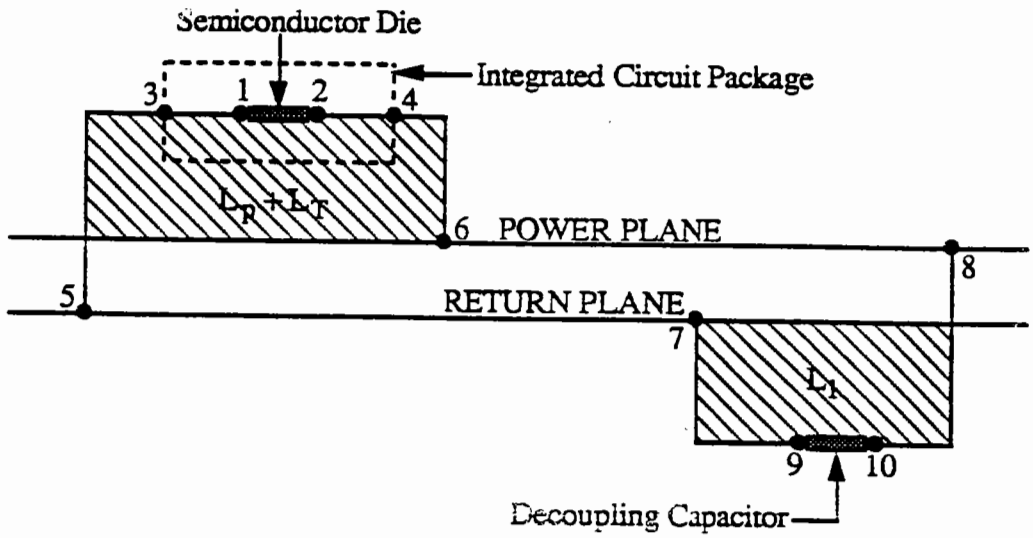
A circuit model was constructed for analysis purposes to accurately reflect the operation of a typical multilayer printed circuit board (PCB). The purpose of decoupling capacitors, as shown in Section 4, is to reduce the board impedance at high frequencies and to provide more available capacitance at high frequencies from which to draw charge. Therefore, the equivalent circuit model had to represent the PCB in the high-frequency range (10-300 MHz) in order to be useful.

The lumped-element circuit model used for analysis purposes was developed to represent the PCB from 10-300 MHz. Measurements were taken of board impedance as a function of frequency for a single decoupling capacitor placed in seven different locations on a 10 layer, 8" x 9" PCB. For different locations, the pole due to parallel resonance between the board capacitance and the inductance of the decoupling capacitor interconnects experienced slight shifts in frequency. These small variations were caused by changes in the amount of interconnect inductance due to imprecise soldering of the interconnects to the board. Other than these slight variations, the board impedance was found to be independent of the placement of the decoupling capacitor for frequencies below 300 MHz.[1] This independence with respect to location indicates that the operation of the interconnecting traces and vias does not correspond to the distributed-element characteristics of transmission lines. Thus, lumped-element

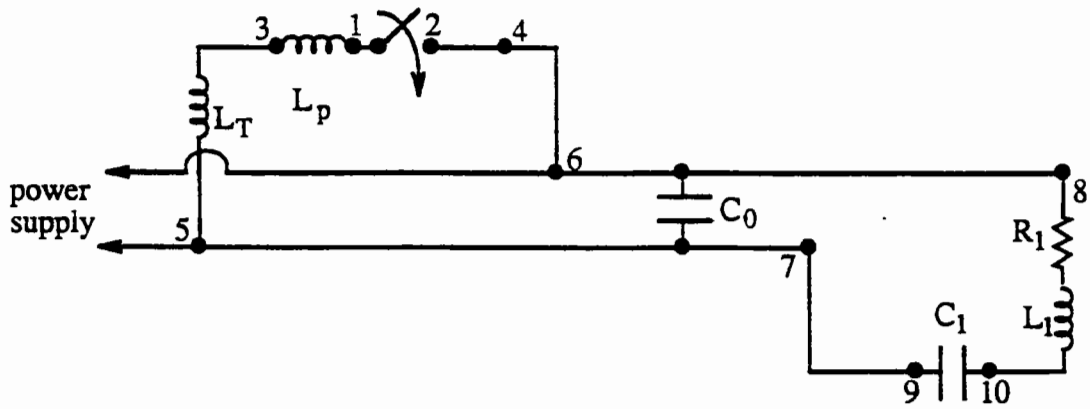
analysis techniques can be properly applied for frequencies below 300 MHz. Above 300 MHz, the transmission line resonances of the board are manifested, and the PCB no longer behaves as a lumped-element circuit.

The physical configuration of a decoupling capacitor mounted on a standard PCB with an IC package is presented in Figure 1a on the next page. Figure 1b shows the equivalent circuit corresponding to this configuration. The elements of this circuit are the surface-mount decoupling capacitor C_1, the resistance representing the finite conductivity of the traces and vias connecting C_1 to the bus R_1, the inductance associated with the loop formed by these interconnects L_1, the interplane capacitance of the PCB power planes C_0, the internal inductance of the digital module L_p, and the inductance associated with the loop of traces connecting the module to the bus L_T.[2]

On typical multilayer PCB's, a pair of adjacent layers is devoted to power and ground, respectively, as shown in Figure 1a. The equivalent power supply of Figure 1b was modeled simply as a DC voltage source accompanied by a series inductance. This inductance is associated with the loop connecting power and ground to the PCB.



(a)



(b)

Figure 1: (a) Physical Configuration and (b) Equivalent Circuit for an Integrated Circuit and Decoupling Capacitor Mounted on a PCB

Surface-mount decoupling capacitors connected between power and ground were modeled as ideal capacitors in series with an inductance and resistance, as shown in Figure 1b. The inductance results from the loop of traces and vias connecting the capacitor to the actual power planes, and the series resistance is associated with the finite conductivity of the interconnect. The approximately linear relationship between this inductance and resistance is evident in the measurements plotted in Appendix A.

The interplane inductance of the power planes can be approximated using the inductance equation for parallel plates

$$L=\frac{\mu_0 d}{W} \qquad (1)$$

where L is the inductance per unit length in the z-direction as shown in Figure 2 atop the next page. Typical values for W and d are 10 inches and 10 mils (0.010 inches), respectively. Assuming $\mu = \mu_0 = 4\pi x10^{-7}$ H/m, the inductance per unit length becomes L = 0.01257 nH/cm. For a typical square board, the length in the z-direction would be 10 inches, or 25.4 cm, resulting in a total interplane inductance of 0.319 nH. This value is significantly less than the inductance of the decoupling capacitor interconnects (on the order of 2-10 nH) and can therefore be neglected. Thus, the interplane (board) capacitance approaches pure capacitance and results in power bus impedances lower than those of single-sided boards.

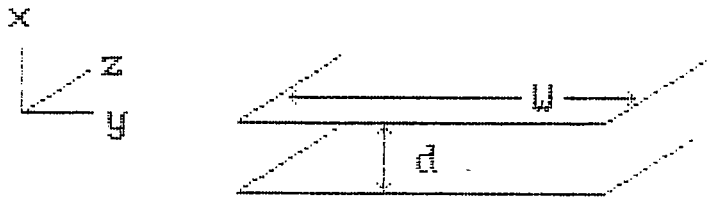


Figure 2: Model for Calculating Inductance per Unit Length

The connection of the digital switching devices to the power bus is usually through a totem-pole arrangement. These digital devices within integrated circuit packages normally consist of transistors (or FETs). For a typical high-gain transistor, the current drawn through the collector and emitter is nearly constant when the device is active. Thus, these transistors were modeled simply as two open/close switches in order to allow for linear, time-invariant analysis. When closed, these switches provide paths for supplying current to digital loads. Typical MOSFET loads were considered as capacitive with some series inductance and resistance due to interconnecting traces. This charging current, drawn in a matter of a few nanoseconds, gives rise to high-frequency noise on the power bus due to voltage drops across the associated trace inductance and resistance.

In reality, these digital switching devices have an internal resistance on the order of 1kΩ. Thus, a more accurate circuit model would have had a resistance of 1 kΩ in series with the ideal transistors. This additional impedance serves to dampen the oscillations of the noise on the power bus.

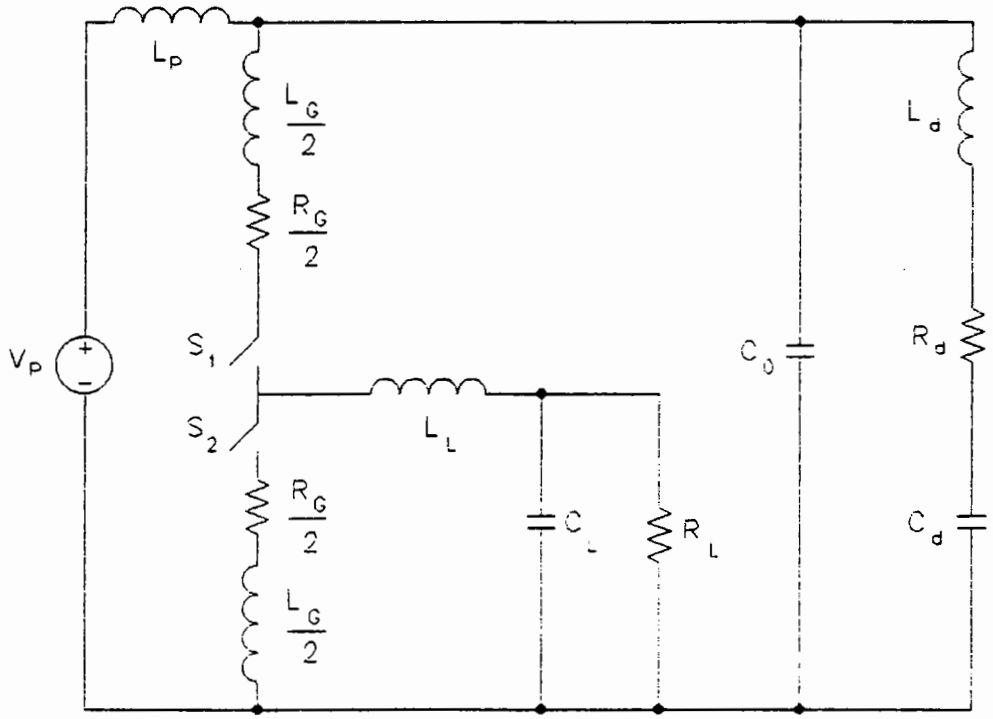


Figure 3: Equivalent Circuit Model for a Standard PCB

The complete equivalent circuit representing a typical PCB is presented in Figure 3 above. The L_d, R_d, and C_d represent the elements associated with the individual decoupling branches.

3: Mathematical Development

A simplified version of the equivalent circuit model can be used to show the need for decoupling capacitors. The various impedances shown in Figure 4 atop the next page represent the total impedances of the supply, gate configuration, and board. The power supply impedance, Z_P, results from the traces and vias used to connect the source voltage to the actual PCB. The gate impedance, Z_G, represents the impedance of a current-demanding load. The amount of current demanded varies in time as a result of enabling and disabling certain logic devices. The board impedance, Z_B, consists of the parallel combination of several decoupling branches. In Figure 4, Z_B consists of the board capacitance in parallel with a single decoupling branch modeled as a series inductor, resistor and capacitor. These include the board interplane capacitance and additional decoupling capacitors with some accompanying resistance and inductance due to interconnections. A more detailed discussion of this board impedance is presented in the next section.

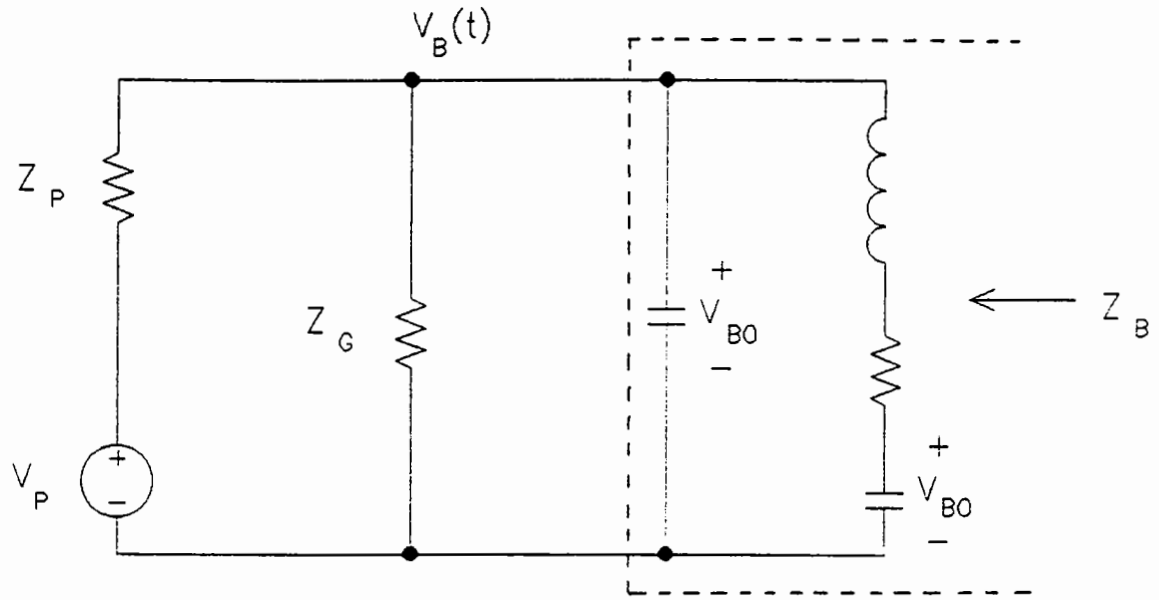
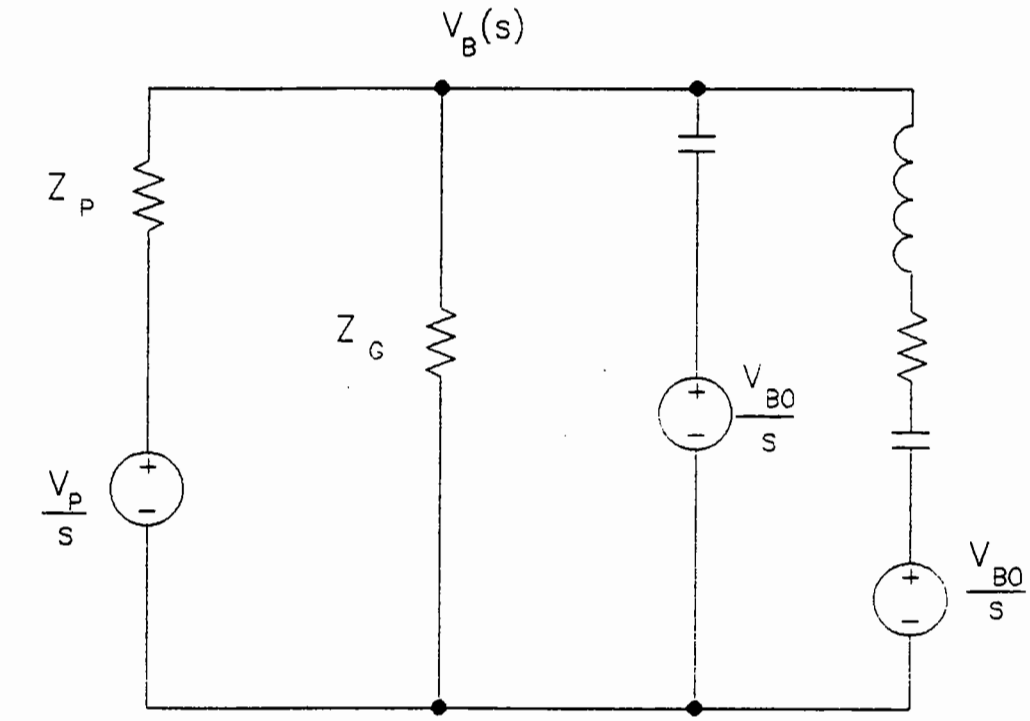
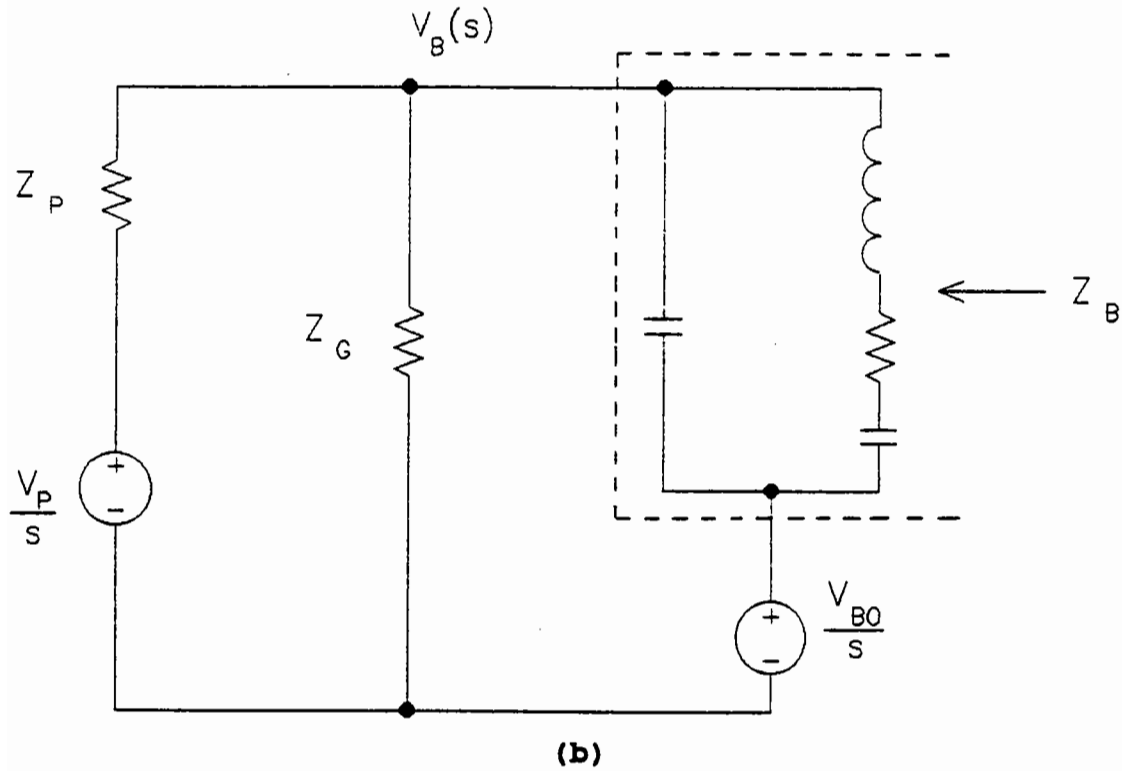


Figure 4: Standard PCB Model

Laplace transform techniques can be employed to analyze the circuit in Figure 4 with proper allowance for the initial capacitor voltages. In the Laplace transform domain, this simple model becomes the circuit presented in Figure 5a as shown on the next page. The proper source transformation for a capacitor with a non-zero initial condition is simply the capacitor impedance in series with an independent voltage source with value (V_{B0}/s), where V_{B0} is the initial capacitor voltage. Thus, the two additional voltage sources result from the initial voltages across the decoupling capacitors. Figure 5b shows the equivalent model with the two identical voltage sources combined in order to label Z_B appropriately.



(a)



(b)

Figure 5: Laplace-Transformed Standard PCB Model

For the circuit of Figure 5b, KCL at node V_B yields

$$\frac{V_B(s)-\frac{V_P(s)}{s}}{Z_P}+\frac{V_B(s)}{Z_G}+\frac{V_B(s)-\frac{V_{B0}}{s}}{Z_B}=0 \qquad (2)$$

Solving for the bus voltage in Equation (2) gives

$$V_B(s)=\frac{\frac{V_P}{s}Z_BZ_G+\frac{V_{B0}}{s}Z_PZ_G}{Z_BZ_G+Z_PZ_G+Z_BZ_P} \qquad (3)$$

The value of V_{B0}, the initial voltage across the decoupling capacitor, is equal to the DC source voltage, V_P. This equality of V_P and V_{B0} results in

$$V_B(s)=\frac{1}{1+\frac{Z_BZ_P}{Z_BZ_G+Z_PZ_G}}\frac{V_{B0}}{s} \qquad (4)$$

Typically, $|Z_P| >> |Z_B|$, and Equation (4) becomes

$$V_B(s) \simeq \frac{1}{1+\frac{Z_B}{Z_G}} \frac{V_{B0}}{s} \qquad (5)$$

As the coefficient of V_{B0}/s approaches 1, the inverse Laplace transform of Equation (5) indicates that the bus voltage as a function of time is equal to V_{B0}, the desired DC value. Therefore, in order to reduce fluctuations in the bus voltage, the coefficient of V_{B0}/s must approach 1. This can be achieved by either increasing the gate impedance or decreasing the board impedance. The gate impedance is generally fixed by the chip designer, so it is not possible to add series resistance to increase the gate impedance. Also, the addition of losses would slow the digital device considerably. Thus, the only available method of stabilizing the bus voltage is reduction of the board impedance.

4: Analysis of the Board Impedance in the Frequency Domain

A mathematical analysis of the board impedance in the frequency domain can be used to relate the board impedance to the magnitude and frequency of the time-domain ringing associated with the noise on the power bus voltage.

As stated in Section 2, the surface-mount decoupling capacitors can be represented by an ideal capacitor in series with a resistor and inductor. The impedance of this decoupling branch varies as a function of frequency, namely

$$Z(f)=R+j2\pi fL+\frac{1}{j2\pi fC}=R+j(2\pi fL-\frac{1}{2\pi fC}) \qquad (6)$$

At some frequency, the two imaginary terms will cancel out and the impedance will be minimized. This frequency is the series resonance frequency of the branch and is written f_0; thus, $Z(f_0)=R$. For this simple decoupling branch, the series resonance frequency is given by

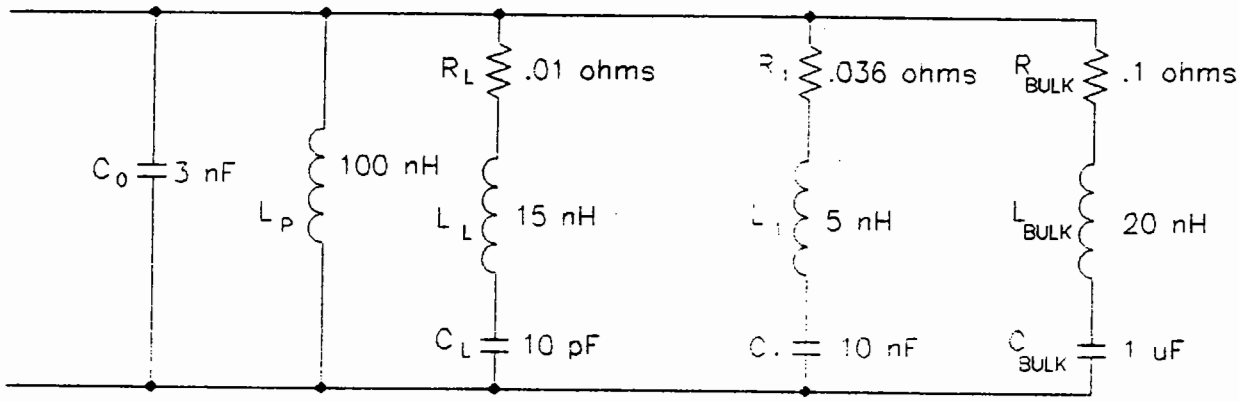
$$f_0=\frac{1}{2\pi\sqrt{LC}} \qquad (7)$$

For frequencies below f_0, the $-(1/2\pi fC)$ term dominates, and the branch is considered capacitive since the majority of the impedance comes from the term associated with the capacitance. For frequencies above the resonance frequency, the $(2\pi fL)$ term is

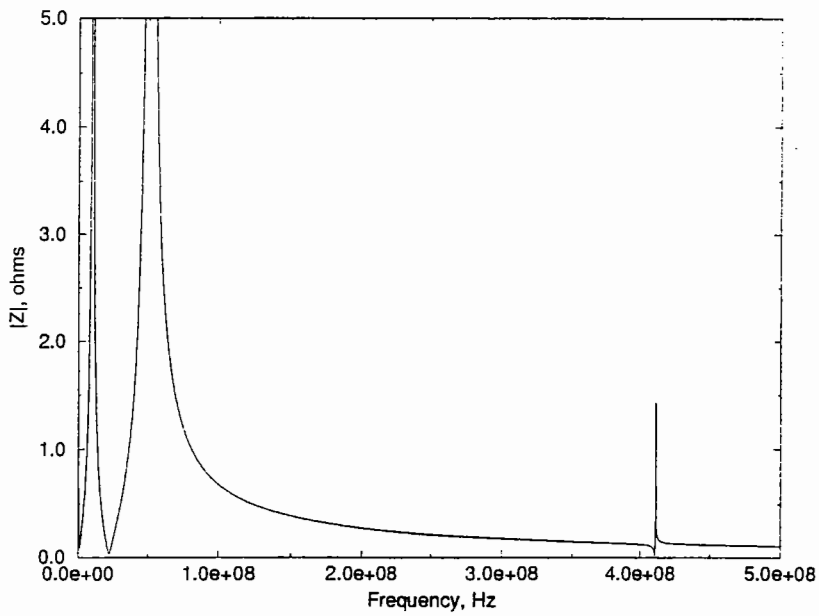
significantly larger, and the branch is considered inductive since the impedance depends heavily on the term associated with the inductance.

The board impedance of an actual PCB consists of several decoupling branches in parallel with the power supply inductance, gate impedance, and board capacitance. Figure 6 on the next page depicts a typical board impedance as a function of frequency. At the series resonance frequency of an individual branch, the branch impedance becomes R, typically on the order of 30 mΩ. Since this small value of resistance is in parallel with the impedances associated with the other branches, the total board impedance approaches zero at the series resonance frequencies of the individual branches. However, at frequencies at which parallel resonance occurs between the inductance of one branch and the board capacitance (called a pole frequency), the total board impedance becomes relatively large. These pole frequencies and zero frequencies alternate in frequency.

Since the current demanded by the load is drawn through the impedances of the branches of the PCB, the magnitude of the noise on the power bus is directly proportional to the board impedance. Therefore, the spikes in the board impedance correspond to significant ringing in the time-domain bus voltage at the pole, or parallel resonance, frequencies. This correspondence will be shown in the PSPICE simulations of Section 5.

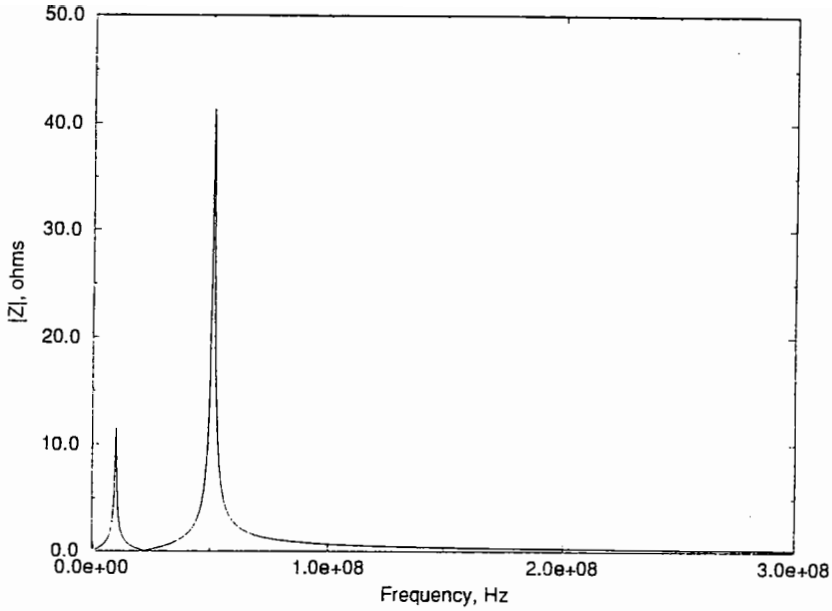


(a)



(b)

Figure 6: Circuit for Finding Typical Board Impedance (a) and Typical Board Impedance out to 500 MHz (b)



(c)

Figure 6: Typical Board Impedance at Low Frequencies (c)

In Figure 6b, the spike around 400 MHz occurs as a result of capacitance associated with the digital device C_L resonating with the inductance of the bulk decoupling branch L_{BULK}. In reality, there is typically 1 kΩ of series resistance associated with this load capacitance, thus decreasing the total board impedance. This 1 kΩ resistance was neglected in these studies, so the spike prevalent at 400 MHz is actually negligible. Thus, Figure 6c is a complete representation of a typical board impedance.

As described previously, above the series resonance frequency of each decoupling branch, the branch becomes inductive, and the branch impedance essentially increases linearly with frequency. This increasing impedance prevents significant current flow through the decoupling branch at very high frequencies. Nearly all charge is then drawn from the board capacitance, and the basic decoupling strategy fails.

5: PSPICE Simulations

5.1: PSPICE Circuit Model

The equivalent circuit model of Figure 3 was modified for use in PSPICE simulations. Two open-close switches were used to model the time-varying current path to the digital load. These simulations were used to obtain time-domain and frequency-domain results for low-to-high transitions of the digital device.

Since PSPICE does not have timed switches, voltage-controlled switches were inserted for the open/close switches of the equivalent circuit model. Thus, the only significant change was the addition of two pulse voltage sources to provide precise control of the voltage-controlled switches.[3] Since the DC source representing the power bus was 5 volts and the switch controls needed only to be on the order of 100 microvolts (0.0001 V), these pulse sources were simply inserted in series with the DC source, as shown in Figure 7 atop the next page.

Also indicated on Figure 7 are the 5 volts initially present across each capacitor connected between power and ground. Values are given on Figure 7 for the components that remained unchanged throughout the simulations. These values were measured from typical 6"-10" square boards with 8-10 mil plane spacing and accepted as standard.

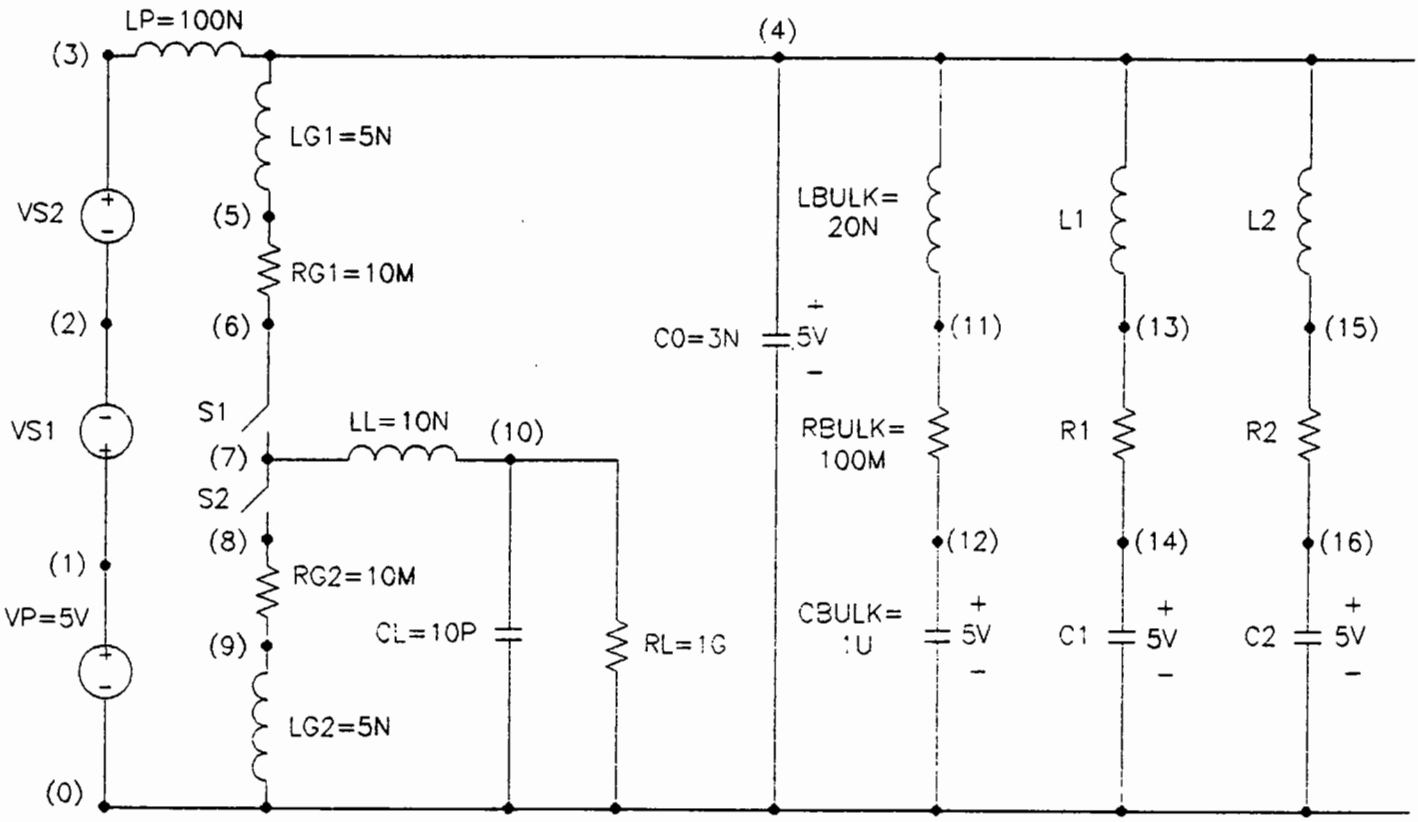


Figure 7: PSPICE Model

5.2: Response to a Single Low-to-High Transition

A single low-to-high transition of the digital device was modeled as both switches closing simultaneously, providing a current path from power to ground through only the inductance and resistance of the load interconnects. Prior to any switching, Switch 2 in Figure 7 was considered closed for a relatively long time, at least until there was no noise on the power bus. Switch 1 remained open, providing no path for charge to reach the load capacitor and give it a nonzero initial voltage. Then, at some instant, Switch 1 also closed, and large currents were drawn

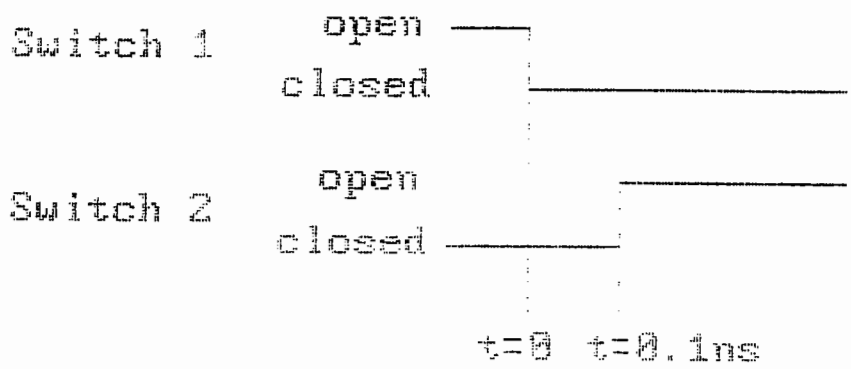


Figure 8: Timing Diagram for a Single Low-to-High Transition

straight through the load interconnect branch from power to ground until Switch 2 opened 100 picoseconds (100 ps) later. Figure 8 above clarifies the timing of these various switchings.

This timed switching introduced high-frequency noise on the power bus, and this noise was allowed to ring down for a given length of time. The analysis consisted of pursuing how well the system compensated for this noise. Additional decoupling components were progressively attached to decrease this ringing and thus improve the performance of the board. Results for these cases are presented in Figures 9 and 10 on the next two pages. A sample PSPICE circuit file including the necessary pulse sources is presented in Appendix B.

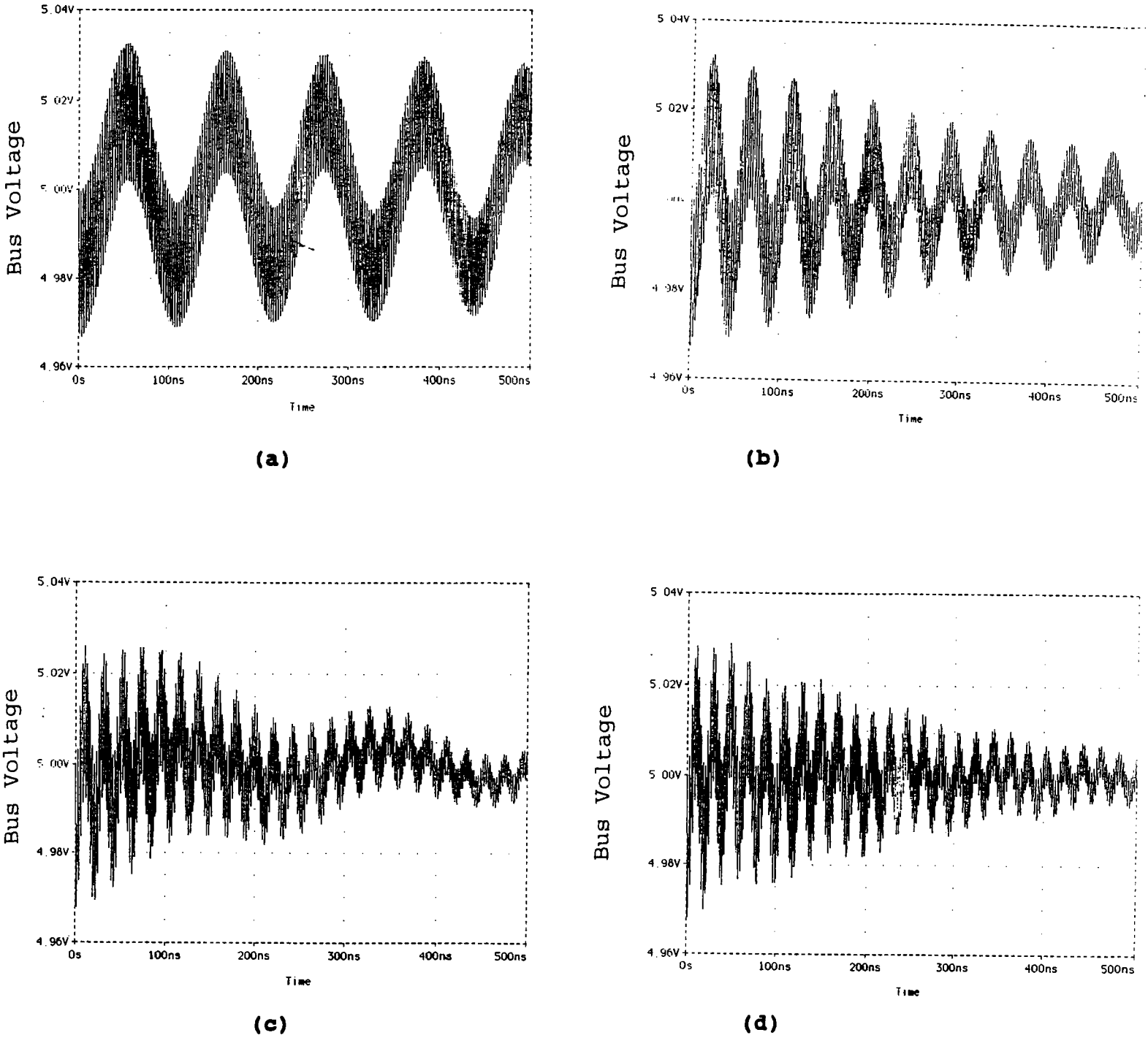
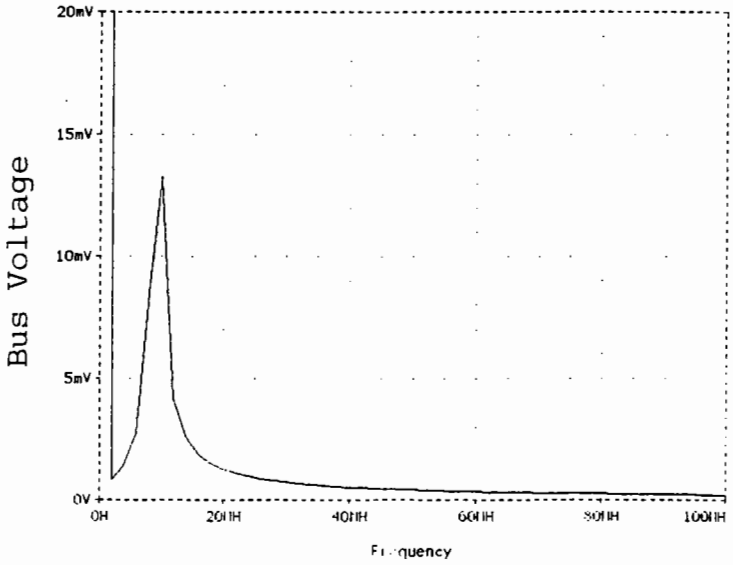
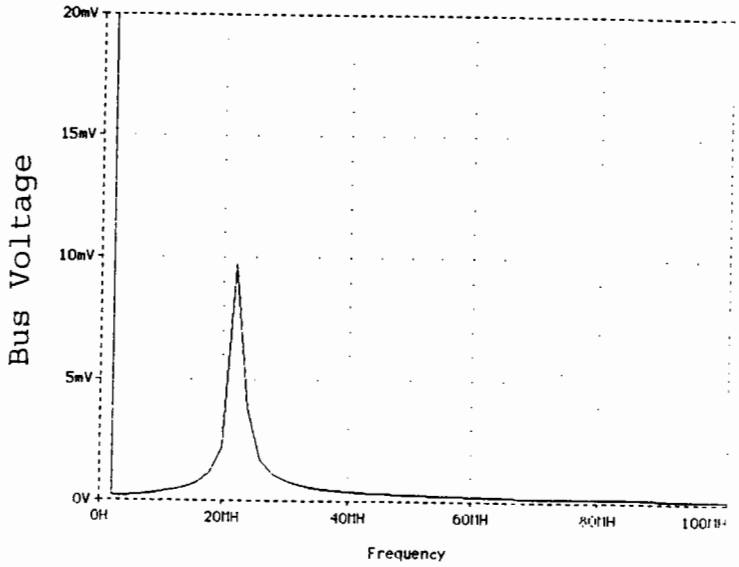


Figure 9: Time-Domain Bus Voltage for (a) Bare Board, (b) Board with Bulk Decoupling Branch Only, (c) Board with High-Frequency Decoupling Branch Only, and (d) Board with Bulk and High-Frequency Decoupling Branches



(a)



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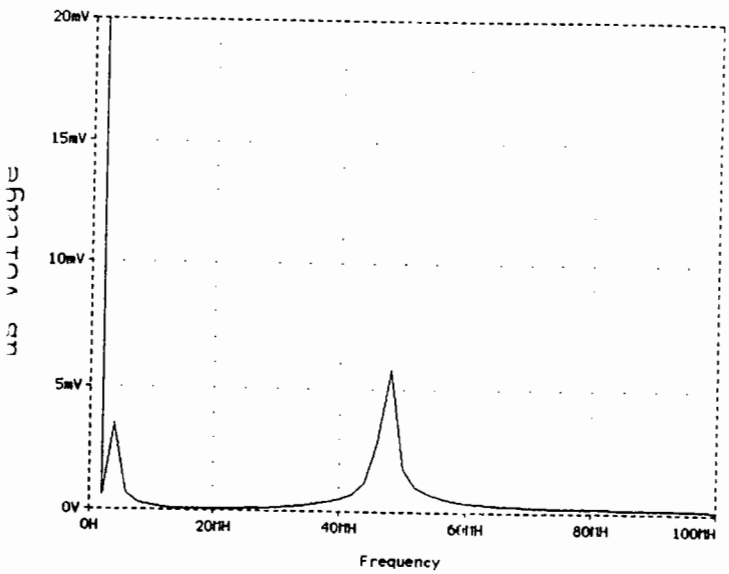

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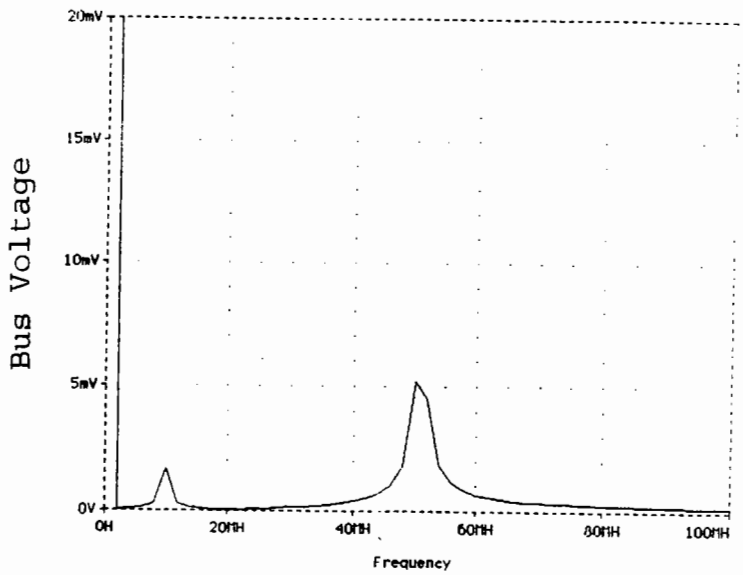


(d)

Figure 10: Frequency-Domain Bus Voltage for (a) Bare Board, (b) Board with Bulk Decoupling Branch Only, (c) Board with High-Frequency Decoupling Branch Only, and (d) Board with Bulk and High-Frequency Decoupling Branches

The bare board configuration consisted of the circuit presented in Figure 7 without any of the branches consisting of series L, R and C. The board with only the bulk decoupling branch corresponded to Figure 7 with no additional L1, R1, C1, L2, R2, or C2 components. The board with only the high-frequency decoupling branch had none of the bulk branch elements (LBULK, RBULK, CBULK) but did have L1=5nH, R1=36mΩ, and C1=10nF. For the last configuration, the bulk and high-frequency branches were simply placed in parallel; note that the impedance of this board is identical to that of Figure 6a.

The time-domain fluctuations in the bus voltage were decreased as additional decoupling branches were added. The representations of these voltages as functions of frequency clarify this lessened ringing. Additional decoupling served to move the poles higher in frequency and decrease their magnitudes as desired. The compatibility of the poles in Figure 10d and those of Figure 6c indicates the correspondence between the poles of the board impedance and the ringing in the time-domain bus voltage.

5.3: Response to a Pulse Train

A series of transitions in the logic level of the digital device can lead to further increases in the noise on the power bus. If such transitions occur periodically with period T=1/f and this frequency f corresponds to a pole frequency of the board

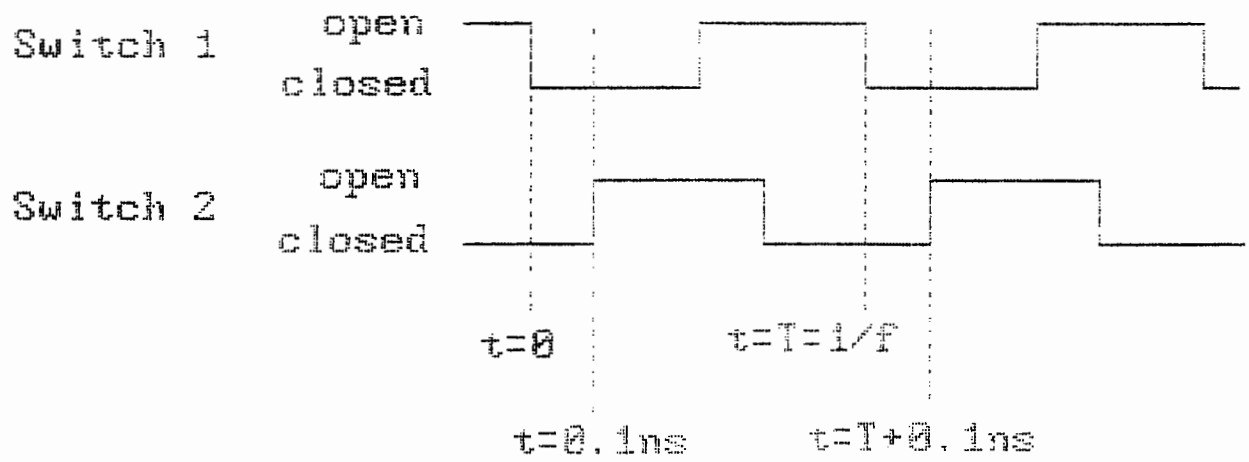
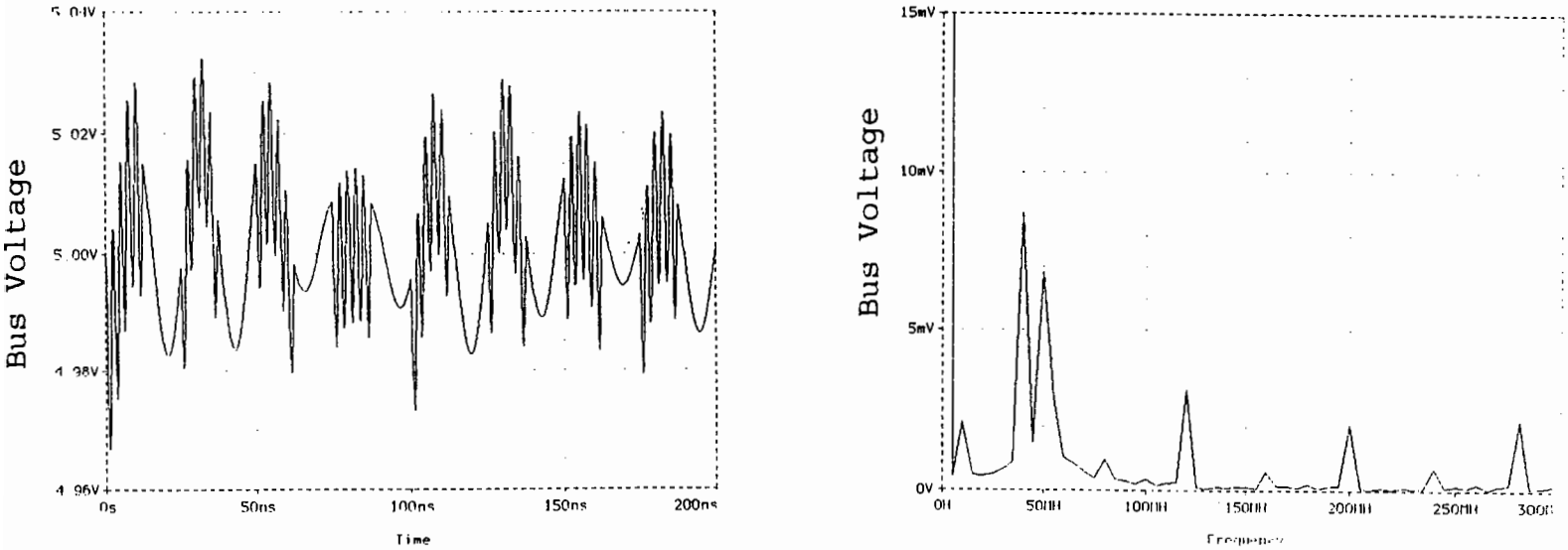


Figure 11: Timing Diagram for a Series of Transitions

impedance, ringing on the order of 80 mV can occur on the bus voltage. In contrast, for a single low-to-high transition, there was no frequency component larger than 15 mV for any board configuration, as evidenced in Figure 10. However, if the frequency of the transitions does not correspond to a pole frequency, the noise voltage is significantly decreased. Figure 11 above depicts the timing of these switchings, which are still separated by 0.1 ns.

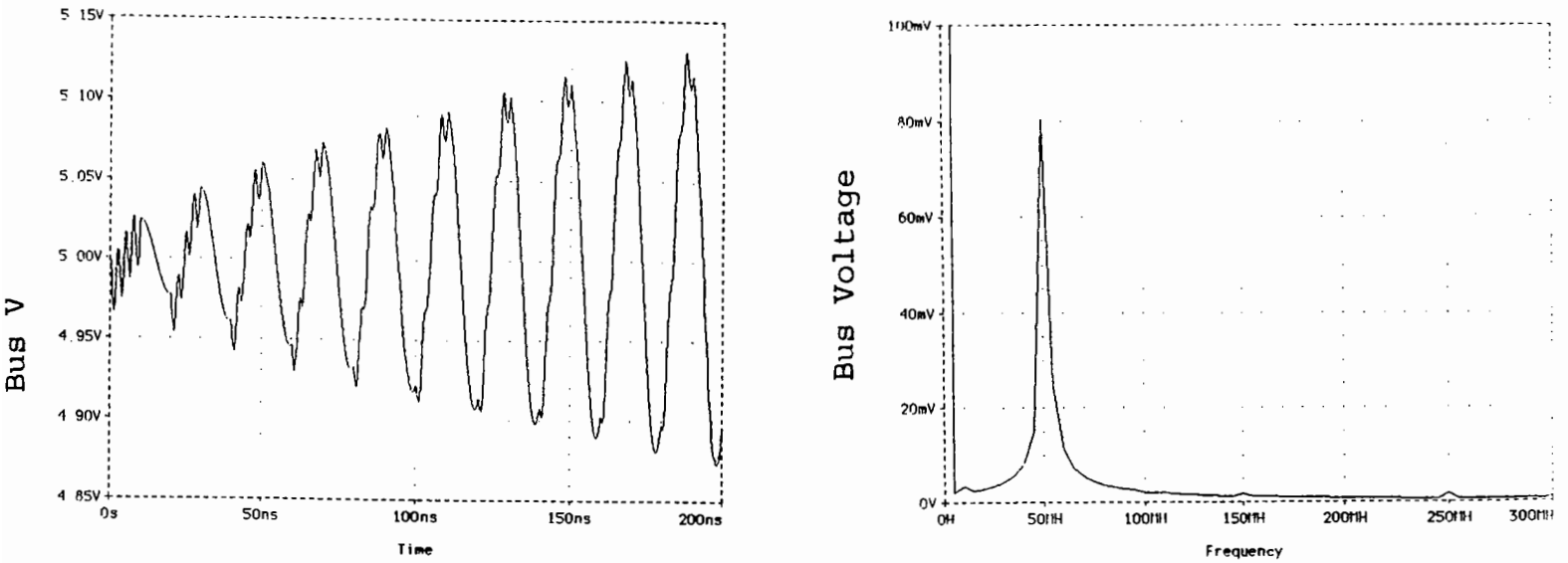
The board impedance of Figure 6c has poles at approximately 10 MHz and 50 MHz. The board configuration of Figure 6a was modeled on PSPICE and excited with a series of transitions with periods 25 ns (f=1/T=40MHz) and 20 ns (f=1/T=50MHz). This series of transitions was simulated by allowing a 50% duty cycle pulse train to control each of the switches, thus approximating the enabling and disabling of the digital device. The results of these simulations are presented in Figures 12 and 13 on page 26.

Note that for the pulse train frequency significantly less than the pole frequency of the board impedance as in Figure 12, the noise on the power bus is on the order of 10 mV. For the pulse train frequency equal to the pole frequency of the board impedance as in Figure 13, the ringing in the bus voltage is nearly 80 mV. Clearly, even after decoupling techniques are applied, it is desirable to minimize periodic switching of the logic device at a frequency corresponding to a pole of the board impedance.



(a) (b)

Figure 12: Response of Circuit of Figure 6a to Pulse Train With Frequency 40 MHz in the (a) Time Domain and (b) Frequency Domain



(a) (b)

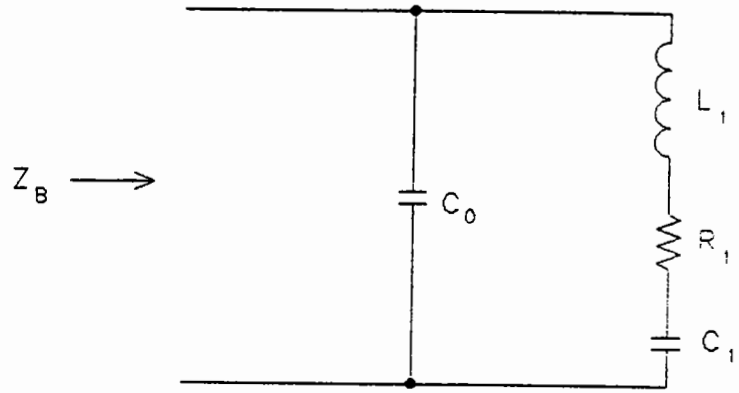
Figure 13: Response of Circuit of Figure 6a to Pulse Train with Frequency 50 MHz in the (a) Time Domain and (b) Frequency Domain

6: Reduction of the Board Impedance in the Frequency Domain

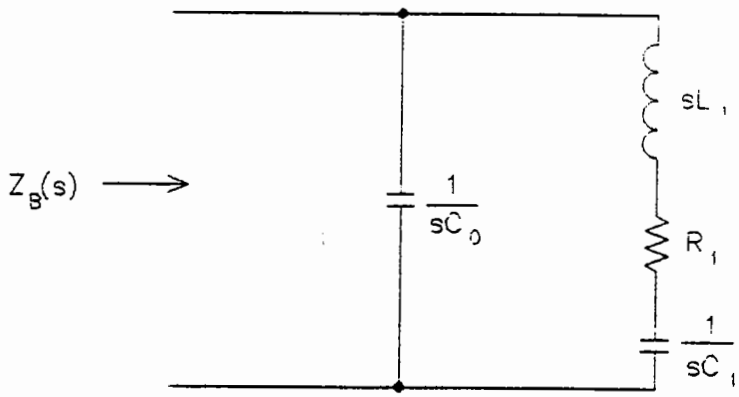
As shown in Section 3, minimizing the noise on the power bus is achieved by decreasing the board impedance. Further mathematical analysis can yield expressions which indicate methods for proper reduction of the board impedance.

6.1: Reducing Quality Factor of Simple Model Poles

Decreasing the quality factor of individual poles results in the desired decrease in the magnitude of the board impedance at the pole frequencies. Therefore, an approximate expression for the quality factor (Q) associated with the poles of the board impedance was needed to determine methods for reducing Q. The simple board impedance presented on the next page in Figure 14a was analyzed in the Laplace-transform domain; this transformed circuit is depicted in Figure 14b.



(a)



(b)

Figure 14: Simple Model of Board Impedance (a) and Laplace-transformed Simple Model of Board Impedance (b)

It can be shown that this simple board impedance as a function of the Laplace-transform variable (s) is given by

$$Z_B(s) = \frac{s^2 L_1 C_1 + s C_1 R_1 + 1}{s C_0 L_1 C_1 \left(s^2 + s\frac{R_1}{L_1} + \frac{C_0 + C_1}{C_0 L_1 C_1}\right)} \qquad (8)$$

The denominator of this board impedance expression is proportional to the denominator of the general form of the

transfer function of a biquadratic circuit.[4] In mathematical terms,

$$sC_0L_1C_1\left(s^2+s\frac{R_1}{L_1}+\frac{C_0+C_1}{C_0L_1C_1}\right)\sim s\left(s^2+s\frac{\omega_0}{Q}+\omega_0{}^2\right) \qquad (9)$$

Therefore, the expression for the resonant frequency becomes

$$\omega_0=\sqrt{\frac{C_0+C_1}{C_0L_1C_1}}=\sqrt{\frac{1}{L_1}\left(\frac{1}{C_1}+\frac{1}{C_0}\right)} \qquad (10)$$

and the quality factor, the ratio of reactance to resistance at the resonant frequency, can be expressed as

$$Q=\frac{\omega_0L_1}{R_1}=\frac{\sqrt{\left(\frac{1}{C_1}+\frac{1}{C_0}\right)L_1}}{R_1} \qquad (11)$$

Thus, in order to reduce the quality factor of these simple model poles, the series inductance L_1 should be decreased, while the board capacitance C_0 and series resistance R_1 should be increased. Figures 15, 16, and 17 show the reduction of the board impedance as a result of decreasing L_1, increasing C_0, and increasing R_1, respectively. The board configuration shown in Figure 14a was used to generate each of these figures. All but one of the elements were held at constant values while the parameter of interest was changed. Thus, C_0=3nF, L_1=5nH, R_1=36mΩ, and C_1=10nF unless otherwise specified on the figure.

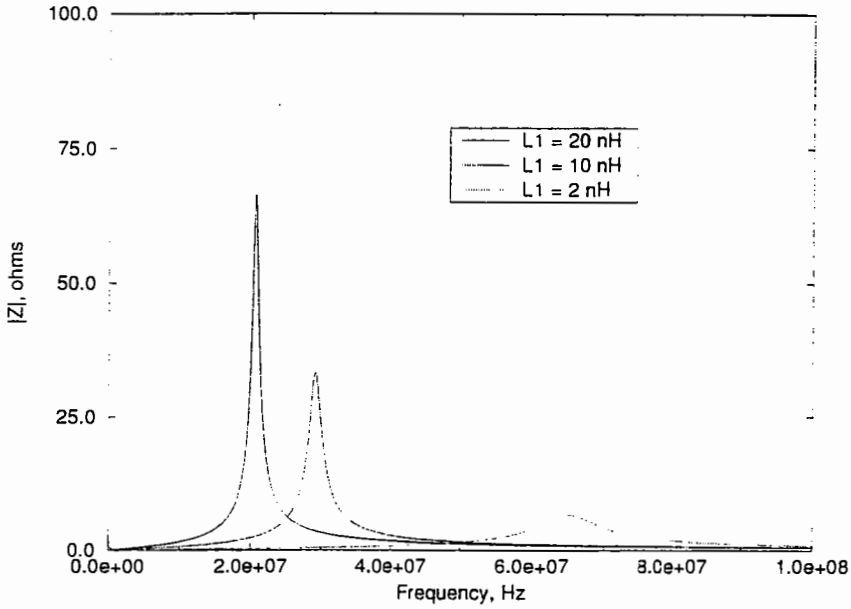


Figure 15: Effect of Reducing L_1 on the Board Impedance

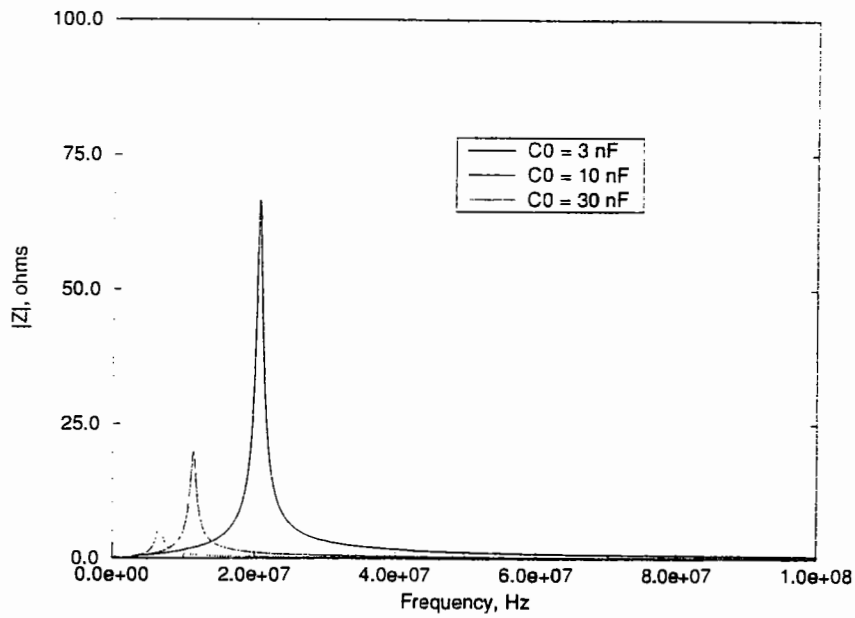


Figure 16: Effect of Increasing C_0 on the Board Impedance

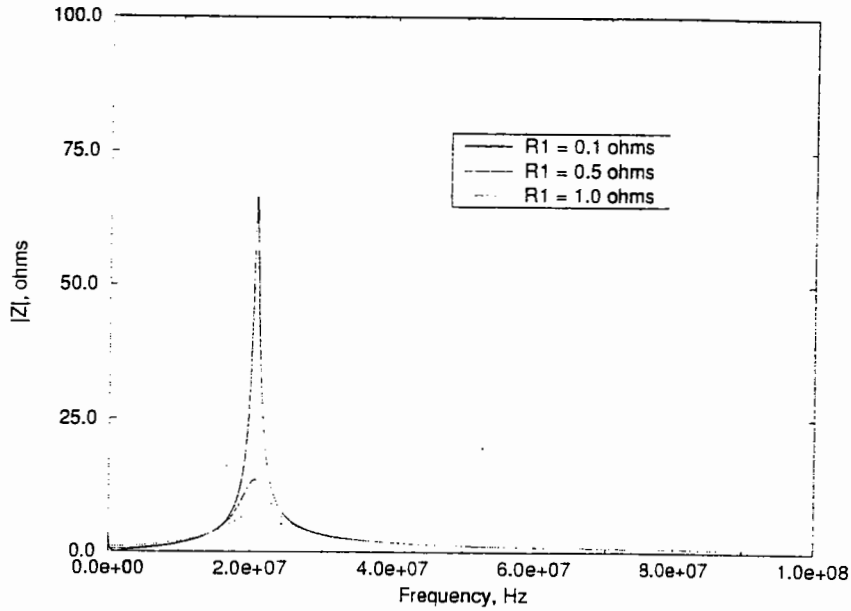


Figure 17: Effect of Increasing R_1 on the Board Impedance

Realistically, adding series resistance to each of the numerous high-frequency decoupling branches in a typical design is not feasible due to space considerations. For these branches, the only methods of reducing Q involve minimizing the trace inductance and increasing the board capacitance. However, since the number of bulk (low-frequency) decoupling branches is on the order of 1-10, increasing the series resistance is a feasible technique for reducing the quality factor of the pole associated with the branch.

6.2: Extending Results for Simple Model Poles to Complex PCB's

Typical decoupling strategies involve more than one surface-mount decoupling capacitor. As shown in the Section 4, for frequencies below the resonance frequencies of the individual branches, the decoupling branches can be considered capacitive.

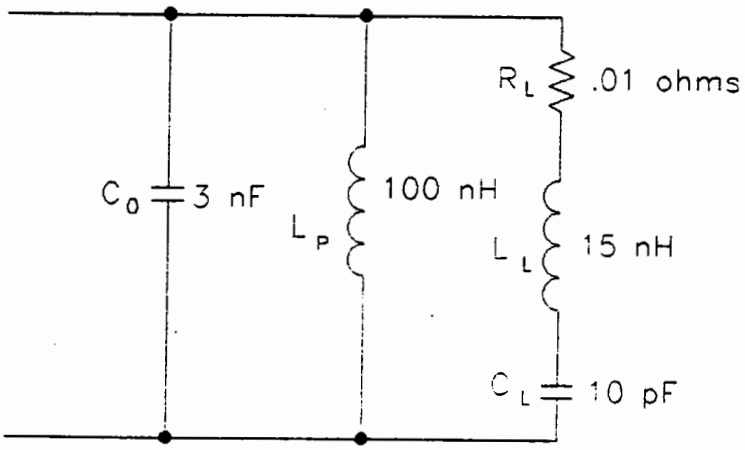
Above these resonant frequencies, these same branches can be considered inductive. As long as the poles and zeros associated with these branches are spaced far apart in frequency, this inductive nature gives rise to large values of branch impedance after the branch has gone through resonance. This large parallel impedance can thus be neglected from the expression for the overall board impedance. Therefore, the models presented in Figures 14a and 14b and the results stemming from their analysis are approximately applicable for boards with multiple decoupling branches. For these more complex PCBs, C_0 in Figures 14a and 14b is actually the parallel combination of the board capacitance with the decoupling branches for frequencies below the series resonances ($f<f_0$) of the individual branches. The series inductances of the decoupling branches for frequencies above the series resonances ($f>f_0$) of the individual branches result in large branch impedances. Since these high branch impedances are in parallel with the rest of the board impedance, the inductive branches are neglected in this analysis.

Hence, for circuit boards with multiple decoupling branches, further reduction of the board impedance in the frequency domain can be achieved by applying the same techniques used to decrease the board impedance of simple model poles. That is, the board impedance can be lessened by reducing the series inductance or increasing the series resistance of the individual decoupling branches, or by increasing the capacitance still active on the PCB (parallel combination of board capacitance with decoupling

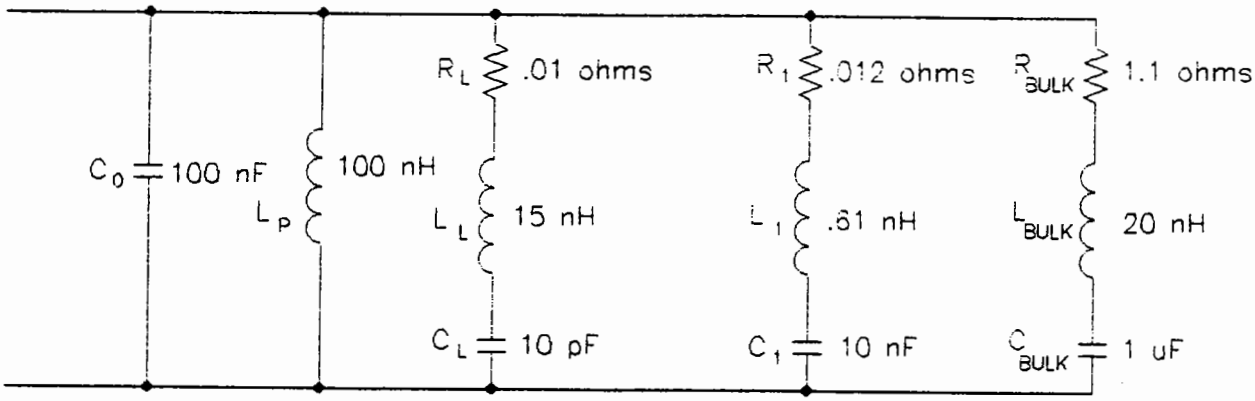
branches at frequencies below the individual branch series resonance).

7: Results

The desired decrease in the board impedance in order to minimize noise on the power bus is thus achieved by the application of decoupling capacitors with minimal interconnect inductance, addition of series resistance to the bulk decoupling branches, and maximization of interplane capacitance. Two circuits used to calculate board impedances for various configurations are depicted in Figure 18 atop the next page. Along with Figure 6a, the impedances of these configurations were analyzed to determine the effectiveness of the decoupling. The values presented in Figure 18b for the board capacitance (C_0=100nF), high-frequency decoupling branch inductance (L_1=0.61nH) and resistance (R_1=12mΩ), and bulk decoupling branch resistance (R_{BULK}=1.1Ω) were considered the best achievable values for each of the components.



(a)

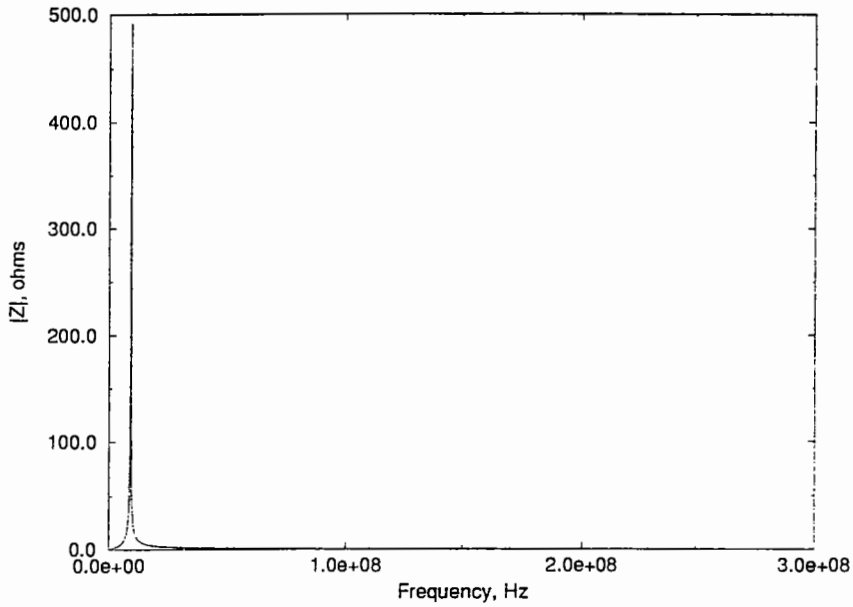


(b)

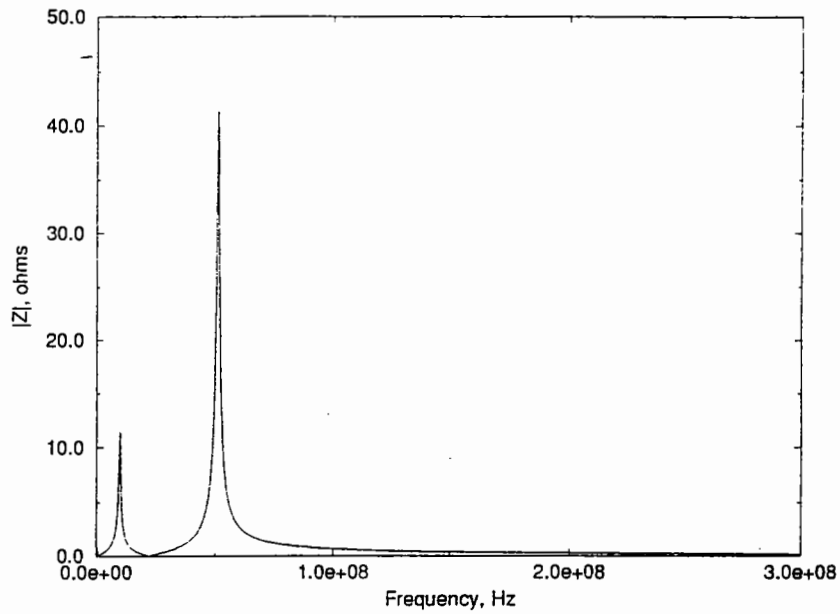
Figure 18: Configurations for Calculating Board Impedances for (a) Bare Board and (b) Optimal Decoupling Board

Plots of the various board impedances as functions of frequency are presented in Figure 19 on pages 37 and 38. The magnitudes of these impedances are on the order of 500Ω for the bare board, 40Ω for the board decoupled as in Figure 6a, and 1.0Ω for the board with optimal decoupling. Clearly, the addition of

the decoupling branches results in significant reduction of the board impedance. However, further reduction can be achieved by minimizing series inductance, adding series resistance, and maximizing interplane capacitance. A final PSPICE simulation with a single low-to-high transition was performed to analyze the bus voltage in the time and frequency domains. The noise voltage was found to be on the order of 12μV, significantly less than the 5mV of Figure 10d, as shown in Figure 20 on page 39.

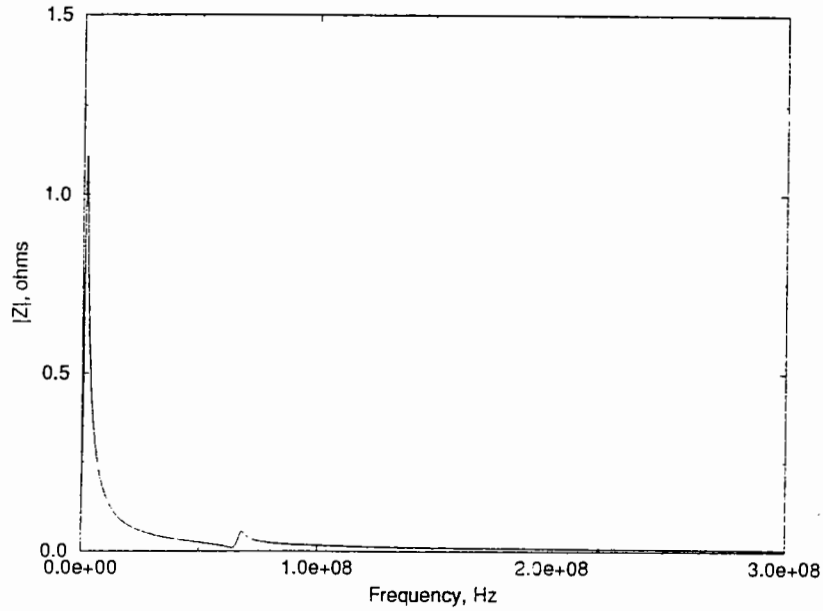


(a)



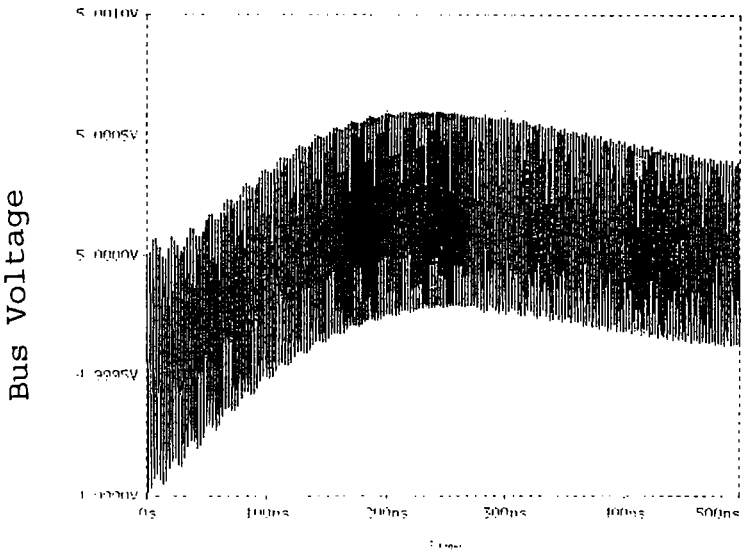
(b)

Figure 19: Board Impedance as a Function of Frequency for (a) Bare Board and (b) Board with High-Frequency and Bulk Decoupling Branches

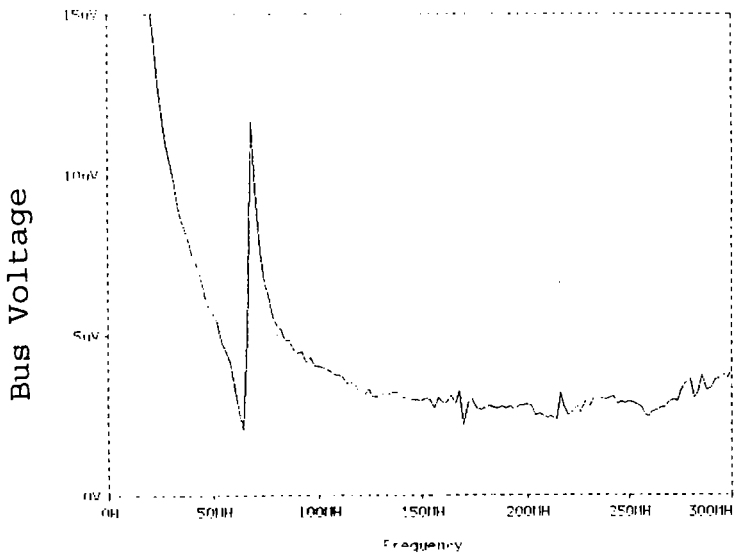


(c)

Figure 19: Board Impedance as a Function of Frequency for (c) Board with Optimal Decoupling



(a)



(b)

Figure 20: Bus Voltage as a Function of (a) Time and (b) Frequency for Board with Optimal Decoupling

8: Summary

The switching of digital devices on typical multilayer PCBs causes sudden current demands. Noise voltage is introduced on the power bus of the PCB when this charge is drawn through the inductance and resistance associated with the traces and vias used to connect the device to the board. Minimization of this noise prevents false switching of other devices connected to the bus as well as radiated EMI.

An equivalent circuit model applicable for frequencies below the resonances of the board (300 MHz) was developed in order to simulate the effects of low-to-high transitions on standard multilayer PCBs. The noise voltage on the bus due to such transitions was related analytically to the magnitude of the board impedance. Reduction of the noise voltage was thus achieved by decreasing the impedance of the power bus. Surface-mount decoupling capacitors were judiciously applied to reduce the magnitude of the board impedance. This impedance was then further decreased by minimizing interconnect inductance, adding series resistance to low frequency decoupling branches, and maximizing the interplane capacitance. PSPICE simulations supported the conclusions of the mathematical analyses and introduced the notion that switching at a frequency corresponding to a pole frequency of the bus impedance resulted in significant noise at that frequency.[5]

Altogether, the power bus of a standard multilayer PCB can

be designed so as to minimize the board impedance and thus decrease the noise on the bus voltage over a wide range of frequencies. The reduction of the board impedance can best be achieved by adding decoupling capacitors with minimal interconnect inductance and maximizing the interplane capacitance of the PCB.

9: References

1: T.H. Hubing, J.L. Drewniak, T.P. Van Doren, and D.M. Hockanson, "Power Bus Decoupling on Multilayer Printed Circuit Boards," University of Missouri-Rolla, 1993, pages 10-11.

2: T.P. Van Doren, J.L. Drewniak, and T.H. Hubing, "Printed Circuit Board Response to the Addition of Decoupling Capacitors," Department of Electrical Engineering, University of Missouri-Rolla, 1992, page 6.

3: J.F. Morris, A PSPICE User's Guide, Department of Electrical Engineering, University of Missouri-Rolla, 1990, pages 25-26.

4: M.E. Van Valkenberg, Analog Filter Design, Holt, Rinehart and Winston, New York, 1982, pages 119-120, 143.

5: J.L. Drewniak, T.H. Hubing, T.P. Van Doren, and P. Baudendistel, "Modeling Power Bus Decoupling on Multilayer Printed Circuit Boards," IEEE EMC Symposium Digest, August 1994.

Appendix A: Linear Relationship Between Trace Inductance and Resistance

Professors Drewniak and Van Doren measured the following values of inductance and resistance for different trace lengths.

Inductance (nH)	Resistance (mΩ)
0.61	12
1.32	17
2.00	22
7.11	54
15.7	95

Table 1: Inductance and Resistance of Different Trace Lengths

This data is represented by the X's in the figure below. The proximity of these points to the linear regression of these inductance and resistance values shows that the data is rather well correlated. This line is given by the equation $f(n) = 0.181n - 1.894$, where n is resistance in mΩ and f(n) is inductance in nH.

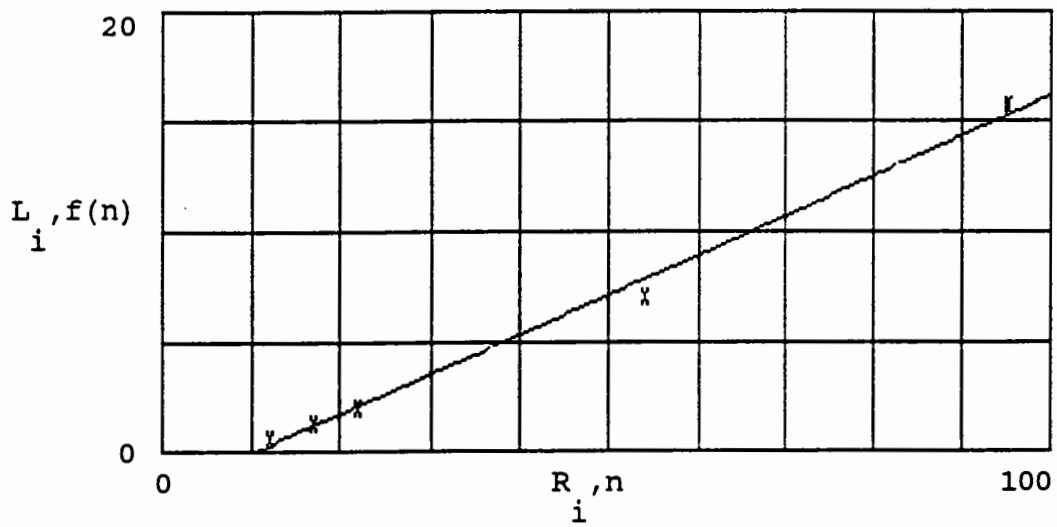


Figure 21: Linear Regression of Trace Inductance and Resistance

Appendix B: Sample PSPICE Circuit File

The following is an actual circuit file used in the PSPICE simulations.

```
MODEL FOR BOARD WITH BULK AND HIGH-FREQUENCY DECOUPLING BRANCHES
VP 1 0 DC 5
VS1 1 2 PULSE(10U 0 0 1F 1F 600N 700N)
VS2 3 2 PULSE(0 10U .1N 1F 1F 600N 700N)
LP 3 4 100N
LG1 4 5 5N
RG1 5 6 10M
S1 6 7 1 2 SWITCH
S2 7 8 3 2 SWITCH
RG2 8 9 10M
LG2 9 0 5N
LL 7 10 10N
CL 10 0 10P
RL 10 0 1G
C0 4 0 3N IC=5
RBULK 4 11 100M
LBULK 11 12 20N
CBULK 12 0 1U IC=5
R1 4 13 36M
L1 13 14 5N
C1 14 0 10N IC=5
.MODEL SWITCH VSWITCH(RON=1U ROFF=1MEG VON=0 VOFF=10U)
.TRAN 1N 500N UIC
.PROBE
.END
```