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Title:

Report on the Efficacy of Split Groundplanes as an EMI Deterrent

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Abstract

EMI can often be reduced by selectively filtering various parts of a given system. One common method employed by designers is to provide a large series impedance by splitting the groundplane near the chassis and routing I/O lines over the split. In this manner, PCB designers hope to lower the level of noise currents contributing to radiation. This work studies the efficacy of the groundplane split as a deterrent for EMI associated with I/O lines being driven against other extended reference structures. A test-board was developed to analyze the impedance of the groundplane split with various configurations. This study concludes that the groundplane split is an ineffective method for reducing high-frequency EMI associated with I/O lines being driven against extended reference structures.

1 Introduction

Low-frequency based design principles are often implemented on PCBs to reduce high-frequency EMI. Unfortunately, geometries that can be modeled as lumped elements at low frequencies must be modeled with distributed elements or transmission lines at higher frequencies. One such design technique is the split groundplane. A split groundplane is often implemented on PCBs that have I/O lines routed to a remote device. Hypothetically, the groundplane split may reduce EMI by introducing a large series impedance in two possible "noise" current conduction paths. Noise sources on the printed-circuit level are not well understood, although much work is currently being done to characterize PCB noise sources [1], [2], [3], [4]. Several possible noise sources are suggested herein to facilitate a discussion on the influence of the split groundplane. The first suggested EMI noise path of concern is shown in Figure 1. Multiple reference structures connected to the chassis at various locations result in conducting loops in the system. Magnetic fields that couple the loops generate parasitic currents. This may be a particularly difficult problem at low frequencies (below *500 MHz*), because the reactance of the loop is small and higher levels of current may be conducted. The connector plate on a PCB is connected to the chassis. A low-impedance connection is desired between the connector plate and chassis, but may be difficult to achieve. A poor connection between the connector plate and the chassis may result in confining the current to certain regions. The "necking" of current results in a higher concentration of magnetic fields in this area. Consequently, the connection between the connector plate and the chassis may be modeled as an inductor. A potential difference between the connector plate and the chassis may drive the EMI antenna as shown in Figure 1. I/O lines decoupled or otherwise connected to the PCB reference plane, and the chassis may comprise a dipole-type EMI antenna.

At low frequencies, splitting the groundplane near the connector plate effectively breaks the conducting loop by placing a high reactive impedance in series with the loop. Subscribing to a single-point ground in devices is expected to reduce the level of low-frequency current being conducted around the interior of the chassis. As an example, a typical groundplane split in a daughter-card may be modeled approximately as a 20 pF capacitor. The inductance of the parasitic loop may be approximately 40 nH. Looking at the parasitic loop in Figure 1, *40 nH* may seem low. However, most of the conductors are large conductors, not wires, and the value for the loop inductance extracted from the experimental data presented in Section 3 is less than *40 nH*. At frequencies well below the series resonance at 178 MHz, the capacitance of the split loads the loop. However, signal return lines that are routed over the split are often decoupled to the chassis island. This raises the capacitance between the reference plane of the daughter-card and the chassis. Decoupling the signal return lines to the chassis island may lower the series resonance to tens of MHz, consequently lowering the efficacy of the split.

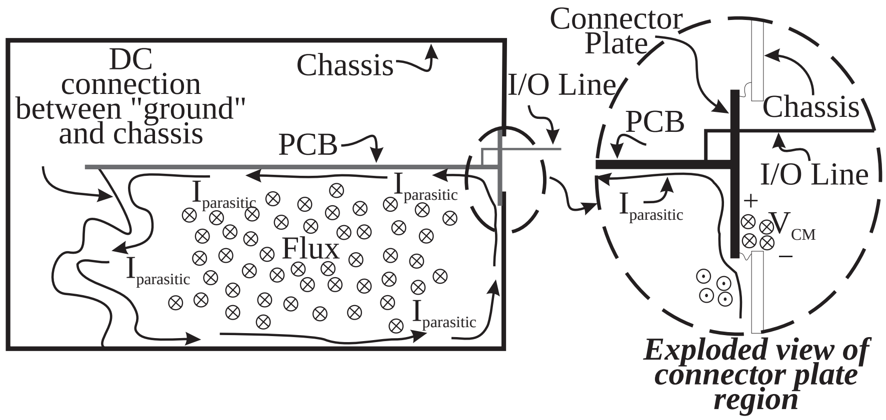


Figure 1: Depiction of how conducting loops and poor connector plate connectivity may result in radiated fields. The connector plate region is exploded to show detail.

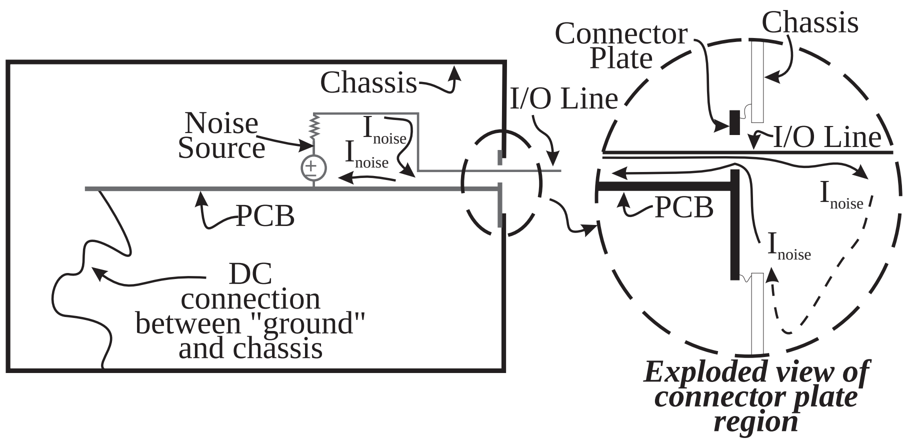


Figure 2: Schematic showing how noise coupled to an I/O line may radiate from a device.

The role of the split in reducing EMI resulting from conducting loops in a chassis is not the focus of this study, but rather is discussed for completeness. The focus of this study is the role of the groundplane split in EMI from radiating I/O lines. Figure 2 shows one way that noise coupled to an I/O line may result in radiation. Noise may be coupled to the line several ways, including capacitive, or inductive coupling. Noise may result from a line being connected through a low impedance to a noisy power-bus when the signal line is driven high or low. If the line is decoupled to the reference plane of the PCB, the noise currents should be shunted to the reference and not radiate. Unfortunately, decoupling capacitors are not very useful beyond a few hundred megahertz [5]. The series inductance resulting from mechanically placing the capacitor typically dominates the element's behavior after several hundred megahertz. Therefore noise can be conducted to and radiated from an EMI antenna composed of the I/O line and the chassis. A split is often introduced in the groundplane near the connector plate. The PCB groundplane region isolated from the signal ground is called the "chassis-island". I/O lines are then decoupled (or filtered) to both the signal

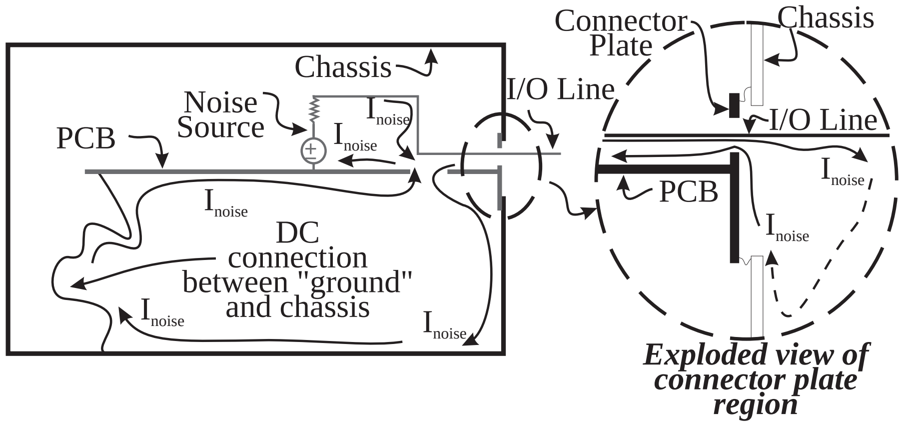


Figure 3: Schematic showing where noise currents may be conducted around the inside of the chassis, because of the relatively high impedance of the split.

return on the PCB, and the chassis-island. In this fashion, noise incident on the I/O line is shunted back to the chassis and does not interfere with the system, providing that the noise bandwidth is within the effective range of the decoupling capacitor.

In this report, theory is developed to describe the high-frequency behavior of the groundplane split. Models are developed to facilitate a discussion of the benefits or hindrances of the split. An s-bus test-board was designed and built to analyze the split and determine the effect of the split on EMI. The results of the experimental studies are contained herein.

2 Theory

The groundplane split is expected to reduce EMI associated with I/O lines being driven against the chassis by placing a large series impedance in the path of the noise current. However, placing a split in the PCB forces the noise currents to take a longer conducted path, and not necessarily a high-impedance displacement current path. Figure 3 shows how a noise current may return to its source along the inside of the chassis. The longer current path is a loop and can be modeled as an inductor at low frequencies, and the groundplane split can be modeled as a capacitor. Figure 4 shows the low-frequency lumped element model for the noise circuit. L_{loop} is the lumped element model for the noise current path below the PCB in Figure 3. The EMI antenna, consisting of the I/O line being driven against the chassis, is shown as a simple lumped element model with an antenna resistance that varies with frequency. This model should be adequate below the full-wave antenna resonance. The groundplane split at low frequencies should not appreciably reduce the level of the noise current, because the alternate current path is a relatively low impedance. Furthermore, if the EMI antenna resonance frequency is defined as the frequency at which the

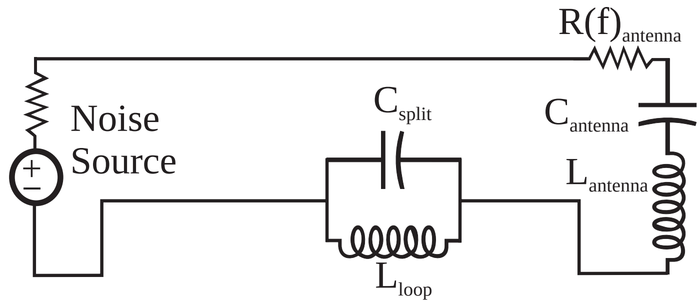


Figure 4: Lumped element circuit model depicting a noise source driving an I/O line over a split groundplane.

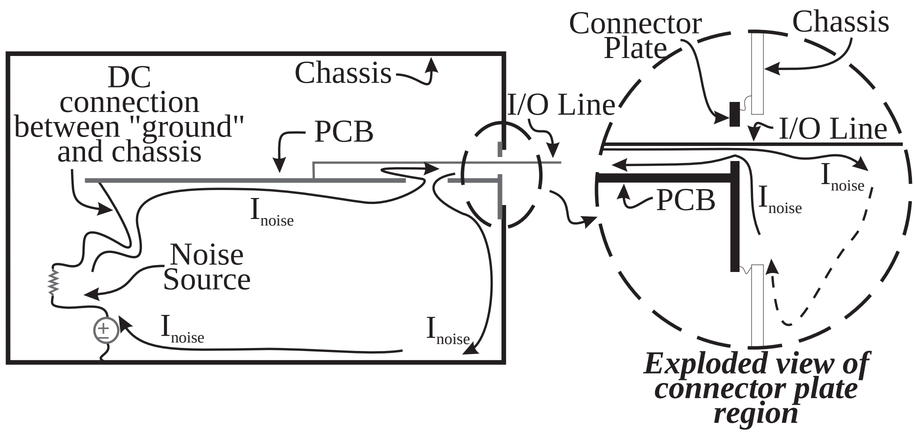


Figure 5: Schematic showing how a split groundplane may increase radiation if the power-bus is noisy with respect to the chassis.

antenna reactance is zero, the introduction of the groundplane split will simply shift the resonance frequency, and not necessarily reduce the level of radiation. The radiated levels could be reduced if the resonance frequency were shifted to a frequency where the radiation resistance was significantly higher than without the split. However, this is not a dependable design parameter because cable lengths may be standard, and the end-user may wish to change the cable. The split groundplane design will provide a high series impedance over a narrow bandwidth around the parallel resonance between L_{loop} and C_{split}. Beyond this resonance, the parallel circuit looks capacitive and begins to short. Fortunately, filtering capacitors may be used to shunt noise currents back to the internal reference structures. Therefore, the behavior of the parallel circuit may be ignored below the series resonance of the filtering capacitors.

The noise models shown in Figures 3 and 4 assumes the noise source is driving the I/O line relative to the reference plane. However, if the power-bus itself is being driven relative to the chassis, as shown in Figure 5 the groundplane split exacerbates the noise problem. The noise source

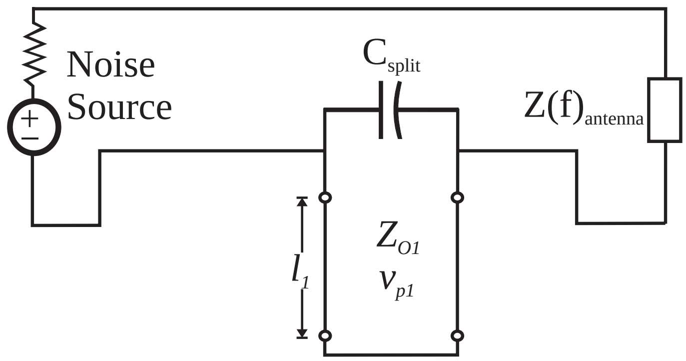


Figure 6: Circuit model depicting a noise source driving an I/O line over a split groundplane. L_{loop} has been replaced with a transmission line model.

in Figure 5 may be a power-bus that has significant RF noise with respect to another reference structure in the chassis. Various connectors, reference planes, and the chassis provide a conduction path for noise currents to return to the hypothetical noise source. Without connectivity between the PCB reference planes and the chassis near the connector plate, the I/O line (shown connected to the PCB reference plane in Figure 5) can be driven against the chassis where the I/O line exits the chassis. When the groundplane is continuous, the I/O line is at relatively the same potential as the chassis where the I/O line exits the system. Consequently, the EMI antenna terminals are shorted, and EMI is reduced.

The high-frequency behavior of the split groundplane design is more complicated. The extended current path imposed on the noise currents by the split may be of significant electrical extent and must be treated as a shorted transmission line. The transmission line model may be different for every device, adding to the difficulty of a generalized analysis. Figure 6 shows the new circuit model, where l_1 is the length of the transmission line, Z_{O1} is the transmission line characteristic impedance, and v_{p1} is the phase velocity in the transmission line. The transmission line of length l_1 is the high-frequency model for the loop below the PCB in Figure 3. The transmission line model is somewhat crude for modeling the loop. The loop is comprised of various planes and connectors that may have resonances other than those predicted by a simple transmission line model. However, the transmission line model should provide a reasonable approximation. The width of the slot is assumed small with respect to wavelength. The antenna lumped element model has been replaced with a simple frequency varying impedance. The focus of this research is to characterize the impedance of the circuit as influenced by the groundplane split, so other parameters such as the antenna, and the transmission line characteristics of the microstrip (trace over a groundplane) are not well modeled in the circuit diagrams.

The impedance of the transmission line will oscillate with frequency between a small (short)

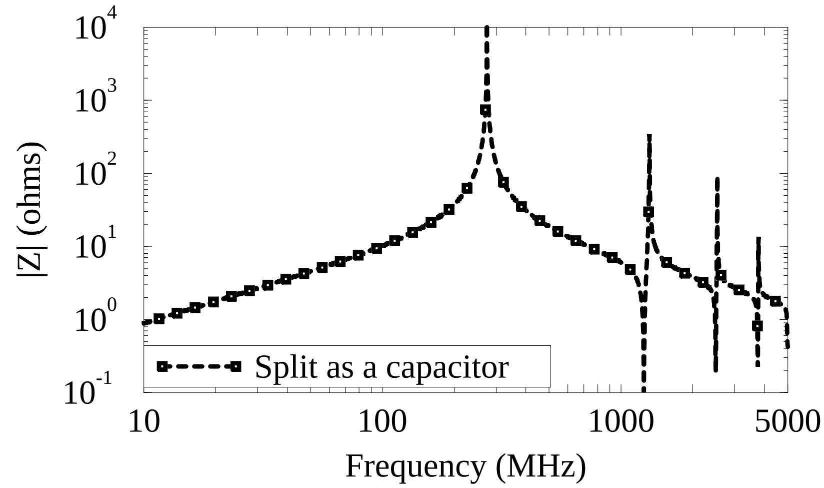


Figure 7: Magnitude of impedance for the model consisting of C_{split} in parallel with a shorted transmission line.

and large (open) reactance. The impedance of the parallel circuit comprised of the transmission line and the groundplane split capacitance is

$$Z(\omega) = j\frac{Z_{O1}\tan\left[\frac{\omega}{v_{p1}}l_1\right]}{1-\omega C_{split}Z_{O1}\tan\left[\frac{\omega}{v_{p1}}l_1\right]}. \tag{1}$$

Figure 7 shows the magnitude of the impedance as given by Equation 1. The parameters were approximated as: $l_1 = 12\ cm$, $C_{split} = 20\ pf$, $v_p = 3.0\times10^{10}\frac{cm}{s}$, and $Z_{O1} = 35\Omega$. The phase velocity was chosen because the loop is air filled, but the other parameters were chosen simply as realistic transmission line parameters for the example. Below 100 MHz the magnitude of the parallel circuit is below 10 Ω. Assuming a 70 Ω EMI antenna input impedance and a low source impedance, the groundplane split would need to provide almost 1 $k\Omega$ to significantly reduce EMI. The pole near 300 MHz results from the parallel resonance between C_{split} and L_{loop} (see Figure 4). A narrow band around the pole may provide the circuit with the necessary attenuation, but a more broadband effect is desired to yield a dependable reduction in EMI. The poles and zeros beyond *300 MHz* result from transmission line resonances.

In the preceding discussion, the groundplane split was treated as a lumped element capacitance. However, even on small daughter-cards the split length is on the order of 10 cm. Common s-bus cards are 8 cm wide. If the splits were completely embedded in $FR-4$ material, the splits would no longer be electrically small beyond a few hundred megahertz. Currents take the path of least impedance, therefore it is well accepted that the return current for a microstrip circuit will return directly under the trace, given a continuous groundplane. When the groundplane is split, displacement current will cross the split. However, if the split is electrically long, it will behave as a slotline transmission line. The electric-field distribution in the split is a function of frequency. Depending on the "mode" excited in the groundplane split, the impedance may vary between small

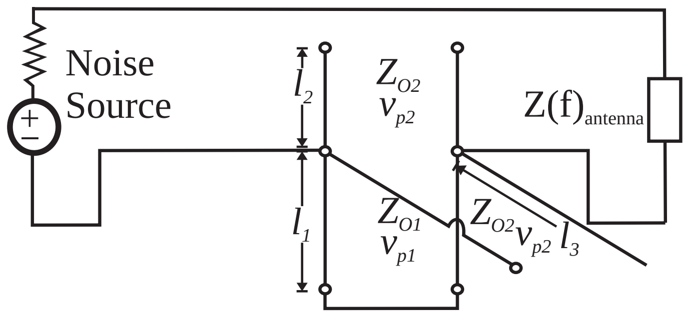


Figure 8: Circuit model depicting a noise source driving an I/O line over a split groundplane. L_{loop} and C_{split} have been replaced with transmission line models.

and large values. The split must then be treated as a transmission line that is sourced where the trace crosses the split. Furthermore, the impedance of the split is dependent on the field distribution in the split on both sides of the trace. Consequently, the high-frequency model for the groundplane split in parallel with the conducting loop consists of three transmission lines in parallel as shown in Figure 8. The transmission line of length l_1 models the loop below the PCB shown in Figure 3, while the transmission lines of length l_2 and l_3 model the groundplane split on either side of the trace. The impedance of the three parallel transmission lines is given by,

$$Z(\omega) = j\frac{Z_{O1}Z_{O2}\tan\left[\frac{\omega}{v_{p1}}l_1\right]\cot\left[\frac{\omega}{v_{p2}}l_2\right]\cot\left[\frac{\omega}{v_{p2}}l_3\right]}{Z_{O2}\cot\left[\frac{\omega}{v_{p2}}l_2\right]\cot\left[\frac{\omega}{v_{p2}}l_3\right] - Z_{O1}\tan\left[\frac{\omega}{v_{p1}}l_1\right]\cot\left[\frac{\omega}{v_{p2}}l_2\right] - Z_{O1}\tan\left[\frac{\omega}{v_{p1}}l_1\right]\cot\left[\frac{\omega}{v_{p2}}l_3\right]}. \quad (2)$$

The magnitude of the impedance is shown in Figure 9, and compared to the magnitude of the impedance with the split treated as a capacitor. The characteristic impedance of the split was assumed $Z_{O2} = 25\Omega$, and the phase velocity was assumed to be half the speed of light in a vacuum $v_{p2} = 1.5 \times 10^{10} \frac{cm}{s}$. The total length of the split was taken as 8 cm, with $l_2 = 3$ cm and $l_3 = 5$ cm to model a trace crossing a split just off center. The card width *8 cm* was chosen to approximately model a standard s-bus daughter-card. The phase velocity was chosen to simulate a slotline completely embedded in FR-4 material with a relative dielectric constant $\epsilon_r \approx 4$. The characteristic impedance of the line was chosen as a realistic value for a slotline. The results for the transmission line modeled split correlate closely with the capacitor model up to a few hundred megahertz, as expected. The highly oscillatory behavior of the impedance at higher frequencies makes the split difficult to use as an EMI deterrent. Depending on the noise source, a broadband high- or low-impedance may be necessary. However, according to the model, the groundplane split results in both high- and low-impedances over narrow bandwidths.

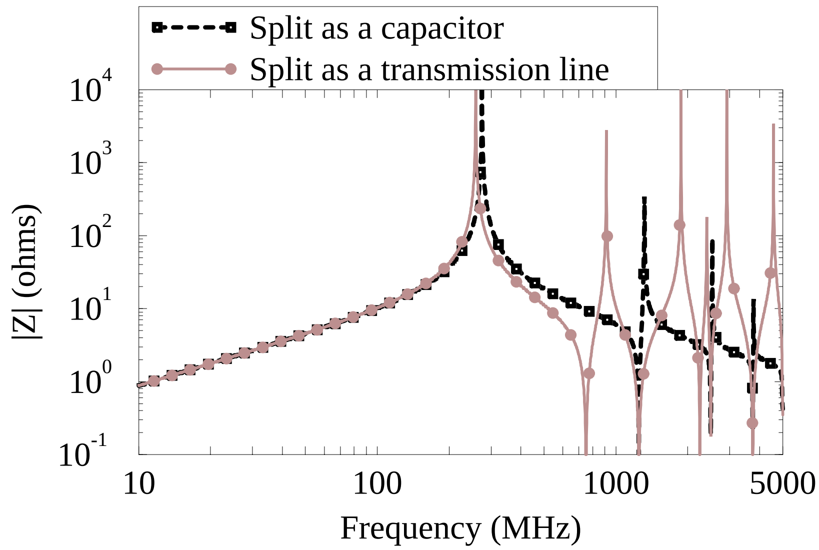


Figure 9: Comparison of the magnitude of the impedance for the split modeled as a capacitor and the split modeled as two parallel transmission lines.

3 Experimental Results

Test-boards were developed to analyze the role of the groundplane split in EMI and determine the validity of the models. The test-boards are s-bus daughter-cards. S-bus cards are frequently used by Sun Microsystems and therefore the test-boards may be analyzed in a wide range of high-speed machines. The test-boards were used in a Sparcstation 20 and an S1000 server and similar results were observed. The board layouts may be found in the Appendix.

Two test-boards were developed. The boards are identical except that one has a continuous groundplane and the other has a split groundplane. The boards were fitted with SMA PCB jacks to allow measurement at different locations around the boards. Figure 10 shows the basic design for the test-board with a groundplane split. For detailed figures regarding the board layout, the reader is referred to the Appendix. For measuring the impedance of the groundplane split, the SMA PCB mount jack was connected to the SMA bulkhead through with a short 0.085" semi-rigid coaxial cable. The housing of the SMA jack was connected to the chassis island, while the center-conductor was routed over the split using zero ohm resistors. The impedance of the groundplane split was measured using a HP4291A Impedance/Material Analyzer ($1\ MHz - 1.8\ GHz$). A Sparcstation 20 and a S1000 Server were used as test-beds. The results from each test-bed were similar. The general setup configuration is shown in Figure 11. The impedance analyzer was calibrated and then compensated to the end of the attached semi-rigid cable. Consequently, the value measured by the analyzer was the impedance measured at the SMA PCB mount jack on the chassis island. No peripherals or power cables were connected to the test-bed during impedance measurements.

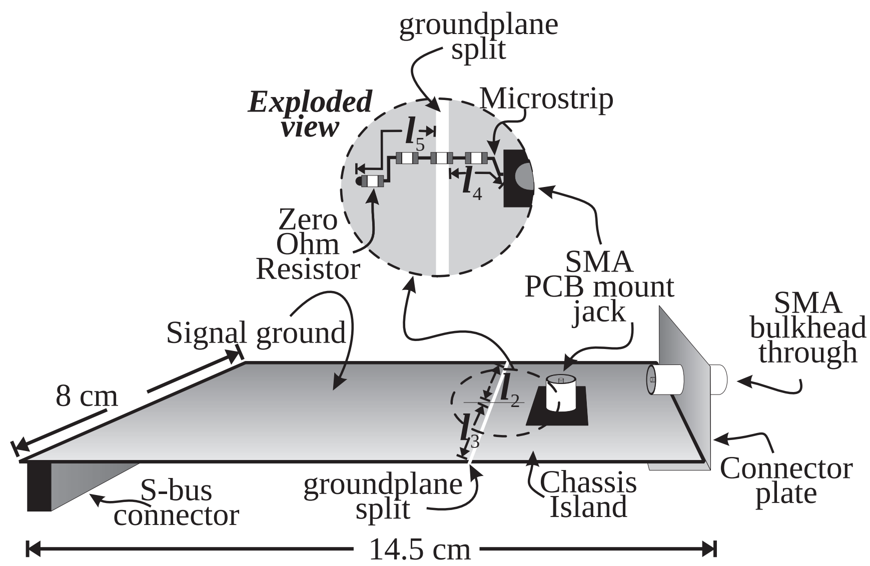


Figure 10: Test-board layout showing the basic setup for taking measurements. The exploded region shows how the center conductor of the SMA jack was routed over the trace to the signal ground using microstrip traces and zero ohm resistors. The lengths designated by l_2, l_3, l_4, and l_5 are the lengths of the transmission lines comprising the equivalent circuit model.

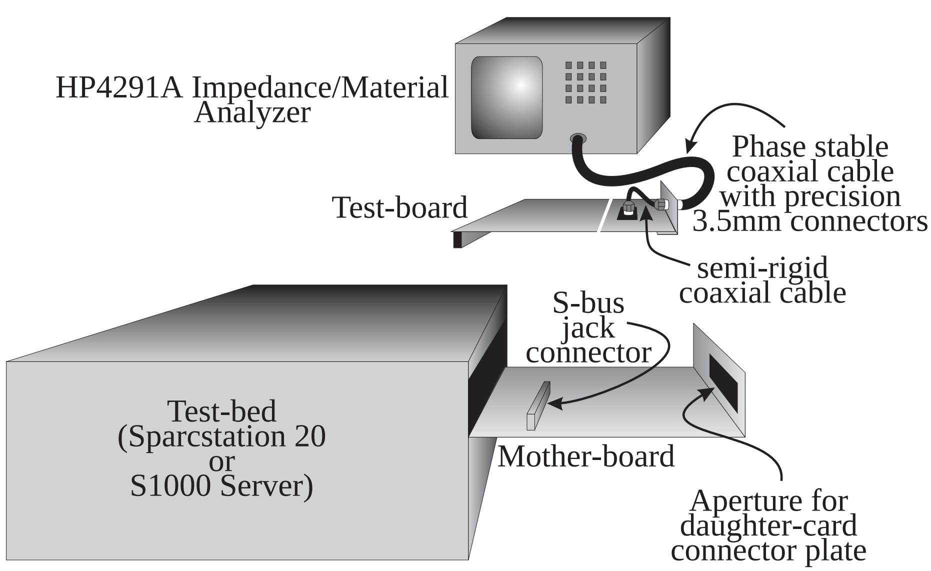


Figure 11: Schematic depicting the configuration used for taking impedance measurements.

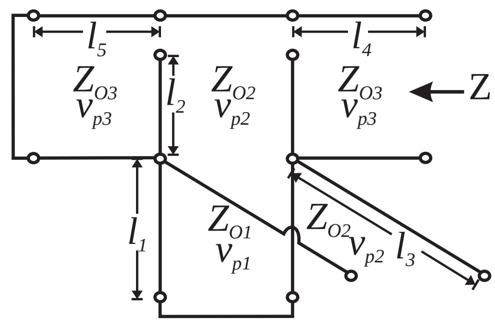


Figure 12: Transmission line model for measuring the impedance of the groundplane split with the test-board.

The configuration of the test board prohibits the direct measurement of the groundplane split. The impedance analyzer can be calibrated and compensated to the SMA PCB jack, however the trace that crosses the gap and connects to the signal ground adds electrical length to the measurement path. The transmission line model for this setup is shown in Figure 12. The transmission line of length l_1 models the loop below the PCB as shown in Figure 8. The lines of length l_2 and l_3 model the groundplane split on either side of the trace. The transmission line of length l_4 models the microstrip between the split and the calibrated reference plane, and the line of length l_5 models the "stub" that is shorted to the PCB reference plane on the other side of the split. The parameters l_2, l_3, l_4, and l_5 are shown in Figure 10. The analytical impedance measured by the impedance analyzer is then given by

$$\begin{aligned} Z(\omega) \quad = \quad & jZ_{O3}\left\{Z_{O1}Z_{O2}\cot\left(\frac{\omega}{v_{p2}}l_2\right)\cot\left(\frac{\omega}{v_{p2}}l_3\right)\tan\left(\frac{\omega}{v_{p1}}l_1\right)+Z_{O3}\left[\tan\left(\frac{\omega}{v_{p3}}l_4\right)+\tan\left(\frac{\omega}{v_{p3}}l_5\right)\right]\times\right. \\ & \left[Z_{O2}\cot\left(\frac{\omega}{v_{p2}}l_2\right)\cot\left(\frac{\omega}{v_{p2}}l_3\right)-Z_{O1}\tan\left(\frac{\omega}{v_{p1}}l_1\right)\cot\left(\frac{\omega}{v_{p2}}l_2\right)-\right. \\ & \left.\left. Z_{O1}\tan\left(\frac{\omega}{v_{p1}}l_1\right)\cot\left(\frac{\omega}{v_{p2}}l_3\right)\right]\right\}\times\left\{Z_{O3}\left[1-\tan\left(\frac{\omega}{v_{p3}}l_4\right)\tan\left(\frac{\omega}{v_{p3}}l_5\right)\right]\times\right. \\ & \left[Z_{O2}\cot\left(\frac{\omega}{v_{p2}}l_2\right)\cot\left(\frac{\omega}{v_{p2}}l_3\right)-Z_{O1}\tan\left(\frac{\omega}{v_{p1}}l_1\right)\cot\left(\frac{\omega}{v_{p2}}l_2\right)-Z_{O1}\tan\left(\frac{\omega}{v_{p1}}l_1\right)\cot\left(\frac{\omega}{v_{p2}}l_3\right)\right]- \\ & \left. Z_{O1}Z_{O2}\tan\left(\frac{\omega}{v_{p3}}l_4\right)\cot\left(\frac{\omega}{v_{p2}}l_2\right)\cot\left(\frac{\omega}{v_{p2}}l_3\right)\tan\left(\frac{\omega}{v_{p1}}l_1\right)\right\}^{-1}. \end{aligned} \tag{3}$$

Some parameters can be determined empirically from the data, and some from the literature. Initially the continuous groundplane was analyzed to determine the exact lengths of l_4 and l_5. The phase velocity and characteristic impedance for the PCB transmission lines (microstrip) were calculated to be [6]

$$Z_{O3} \quad = \quad 47\Omega \tag{4}$$

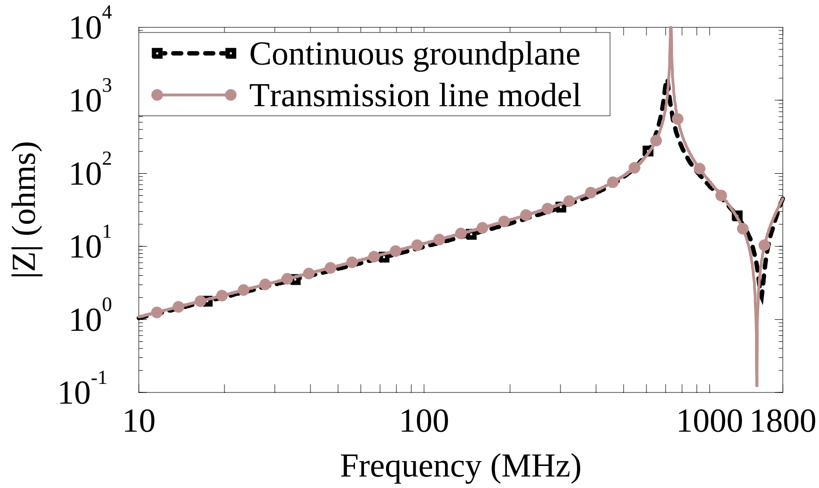


Figure 13: Comparison of the magnitude of the impedance for the transmission line model and experimental data for the continuous groundplane test-board.

$$v_{p3} = \frac{3.0 \times 10^{10}}{\sqrt{3.0}} \frac{cm}{s}, \tag{5}$$

where $\sqrt{3.0}$ is the effective relative dielectric constant for the microstrip geometry. The length of the transmission line "stub" where the microstrip is connected to the PCB ground was measured to be $l_5 = 1.5\ cm$. Experimentally, a quarter-wave resonance was observed around 660 MHz, indicating that the length of the transmission line between the location of the groundplane split and the calibrated reference plane must be $l_4 = 4.8\ cm$. Figure 13 shows a comparison between the transmission line model and the experimental data for the continuous groundplane. The results agree well, although at the resonances the magnitude of the impedance is quite different. This results from the loss in the conductors of the test-board, as well as an imperfect termination to the transmission line.

The parameters associated with the groundplane split transmission lines can be determined in a similar manner. The test-board with the split groundplane was connected to the impedance analyzer without being connected to the mother-board. Ferrite sleeves were used to isolate the test device from the test equipment. The equivalent circuit should be the same as in Figure 12 with the omission of the transmission line with a characteristic impedance Z_{O1}, which models the loop below the PCB in the chassis. The length of the open-terminated transmission lines can be measured with a ruler on the test-board. The characteristic impedance and phase velocity can be determined empirically to match the experimental results. Figure 14 shows a comparison between the transmission line model and the experimental data for $l_2 = 2.8\ cm, l_3 = 5.0\ cm$ and $l_2 = 0.7\ cm, l_3 = 7.1\ cm$ (see Figure 10). The zero ohm resistors were approximately *2 mm* wide. The characteristic impedance and phase velocity for the open-terminated transmission lines were determined to be

$$Z_{O2} = 37\Omega \tag{6}$$

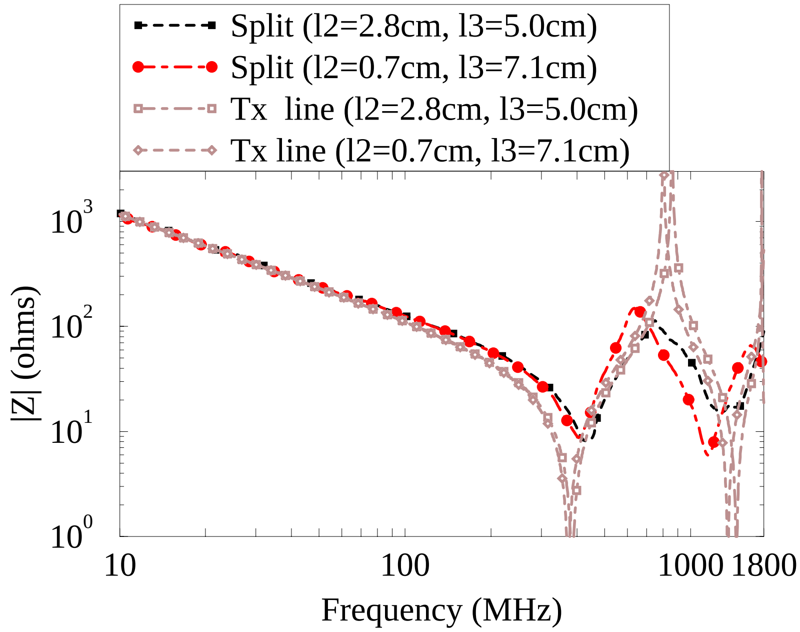


Figure 14: Comparison of the magnitude of the impedance for the transmission line model and experimental data for the split groundplane not installed in the mother-board. The impedance was measured at two locations, $l_2 = 2.8\ cm, l_3 = 5.0\ cm$ and $l_2 = 0.7\ cm, l_3 = 7.1\ cm$ (see Figure 10).

$$v_{p2} = \frac{3.0 \times 10^{10}}{\sqrt{1.2}} \frac{cm}{s}, \tag{7}$$

where $\epsilon_r \approx 1.2$. The phase velocity was chosen by matching the approximate resonance frequencies of the data with the resonance frequencies of the slotline model. The characteristic impedance Z_{O2} was found by matching the model impedance and the experimental impedance results at *10 MHz*, and solving for Z_{O2}.

The discrepancies at the extrema indicate some shortcomings of the transmission line model. The magnitudes of the impedance at the extrema do not match well, because the loss in the conductors and the terminations are not defined in the transmission line model. The loss in the conductors will result in a higher impedance at the zeros. At the poles, several parameters influence the value of the impedance. The transmission line models use perfect shorts and opens to model the split, loop, and microstrip terminations. On the PCB current necking results in higher density magnetic-fields (inductance), and open circuits have fringing electric-fields (capacitance). Furthermore, the transmission line models do not account for the finite dimensions of the transmission line conductors, which will dampen the resonances in the same manner that the finite dimensions of dipole antenna conductors dampen the antenna resonances [7]. The groundplane split transmission line is a slotline transmission line. The slotline is embedded in FR-4 material surrounded by air, therefore the characteristic impedance is a function of frequency [8]. The phase velocity and characteristic impedance determined for the slotlines empirically were chosen because they gave the best fit for a constant value. Despite the deficiencies, the model describes the relevant physics associated with the groundplane split, and shows fair agreement when compared to the experimental results.

The first resonance shown in Figure 14 is a series LC resonance. The loop consisting of the microstrip crossing the groundplane split and terminating on the signal ground is in series with the split, which at lower frequencies should look capacitive. The resonances beyond 350 MHz, however, result from transmission line resonances. If the slot were modeled as a simple capacitor over the observed bandwidth, moving the location where the trace crosses the groundplane split would result in no change in the resonance frequencies. However, the experimental results show a shift in the resonance frequencies, as predicted by the transmission line model.

The split groundplane was installed in the S1000 and the impedance was measured with the impedance analyzer. The parameters for the final unknown transmission line were matched empirically, and determined to be $Z_{O1} = 137\Omega$, $v_{p1} = 3.0 \times 10^{10} \frac{cm}{s}$, and $l_1 = 6.0\ cm$. The phase velocity was chosen because the loop (or transmission line) beneath the PCB in the chassis was air filled. The length l_1 was chosen to approximately match the transmission line resonances with the resonances found in the experimental data, and the characteristic impedance Z_{O1} was determined by equating the impedance for the model and the experimental results at *10 MHz*, and solving for Z_{O1}. Figure 15 shows the comparisons for the split groundplane test-board installed in the S1000. The transmission line model shows similar impedance oscillations compared to the experimental data, although the location of the first resonance is significantly displaced. This is a result of the discrepancies between the simple transmission line model for the loop and the actual properties of the loop. The parameters of the transmission line could be modified to provide a closer match, however, the parameters used to provide the model data for Figure 15 are sufficient for describing the general impedance curve for the split groundplane system. An artificial "mother-board" was constructed to verify that the resonances were a result of the transmission line nature of the system, and not dependent on the chassis or lumped elements in the test-bed. The artificial mother-board was created by soldering four inch wide copper tape to four via pads that were connected to the reference planes of the test-board. The vias were located adjacent and parallel to the top of the s-bus connector. The copper tape was wrapped around the bottom of the test-board and brought back up to the top of the card under the connector plate. The copper tape was then connected to the chassis-island using the conductive adhesive backing of the copper tape. The results for the magnitude of the impedance for the artificial mother-board are shown in Figure 15. The experimental results for the artificial mother-board and the test-board installed in the S1000 show good agreement. By changing the area of the loop created by adding the artificial mother-board, the first resonance can be shifted in frequency. Although the first resonance (a parallel LC resonance) frequency does not agree well for the three data sets, the oscillatory nature is evident in all three sets. The smaller oscillations observed in the experimental data with the test-board installed in the

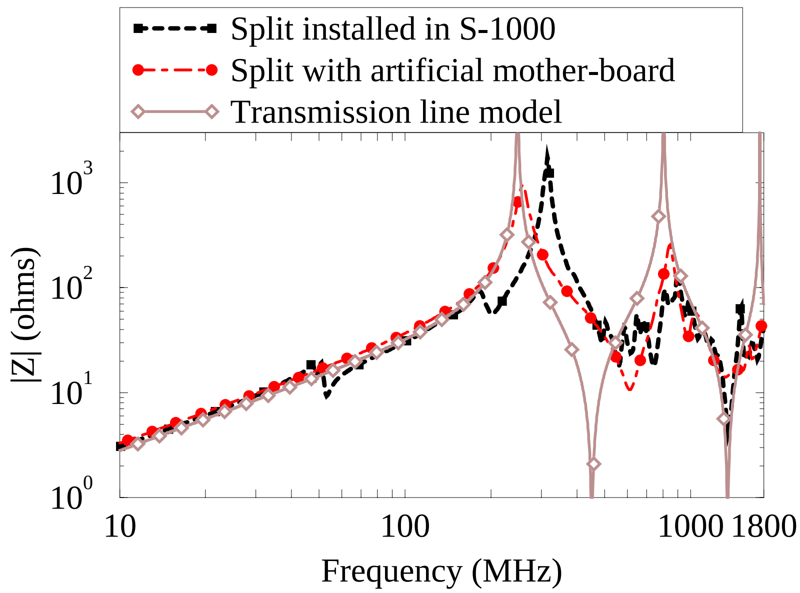
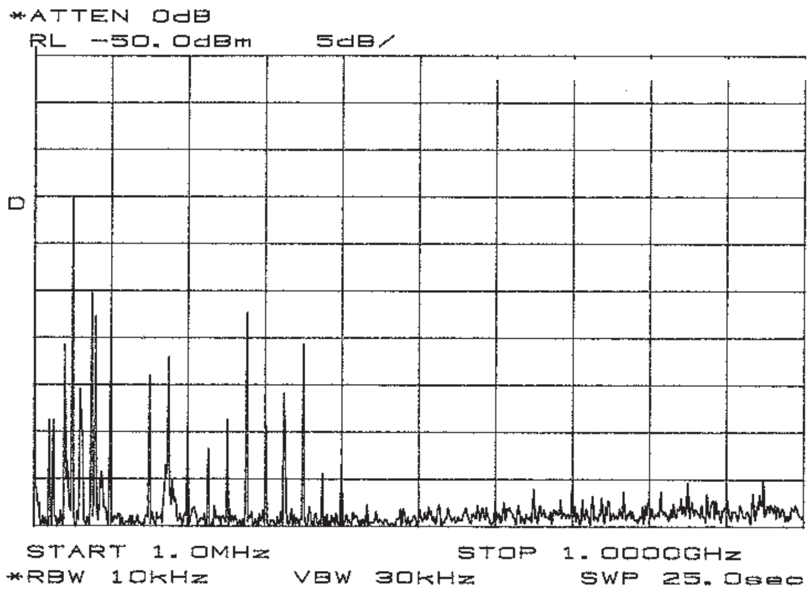


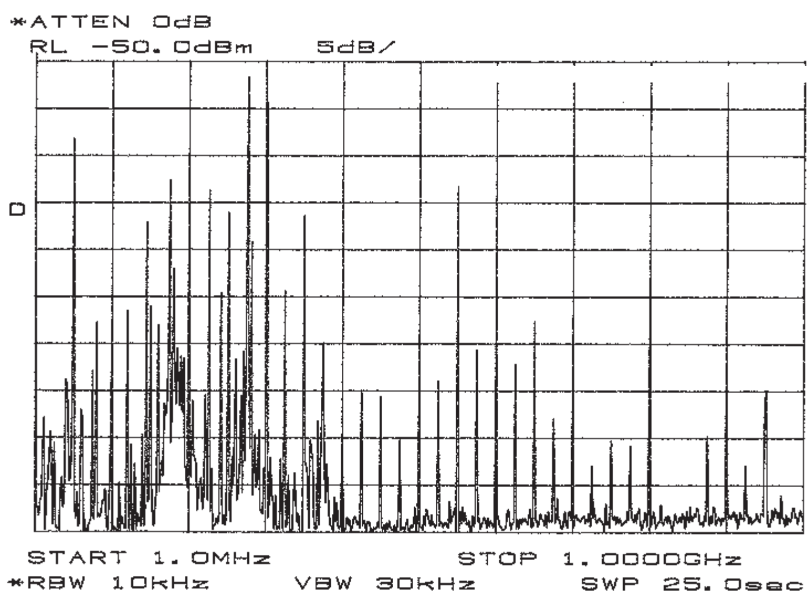
Figure 15: Comparison of the magnitude of the impedance for the transmission line model, experimental data for the split groundplane installed in the S1000, and experimental data with the artificial mother-board.

S1000 may be a result of parasitic resonances in the S1000, such as cavity resonances or coupling to other circuitry.

The previous tests were designed to analyze the impedance of the groundplane split and determine if the transmission line model could adequately describe the split groundplane system. However, the model is only useful in determining the utility of the groundplane split as an EMI deterrent for I/O lines. The groundplane split may influence other noise sources differently. The final test indicates whether the groundplane split reduces radiated energy or not. The test-board was installed in the S1000 with an I/O line connected to V_{CC}. A 1 m section of 24 AWG copper wire was connected to the I/O line, and power was supplied to the S1000. No cables other than the I/O line and the power cable were connected to the S1000. The system was setup in a shielded chamber and the radiated fields were measured with a horizontally polarized EMCO log-periodic dipole array (200 $MHz - 1$ GHz) connected to an HP8563E Spectrum Analyzer (9 $kHz - 1$ GHz). No active circuitry was on the daughter-card, although a *25 MHz* clock is routed through the s-bus connector from the mother-board to the top of the daughter-card. The clock trace on the daughter-card was *2 cm* long and was left floating. The results are shown in Figure 16 for the configuration with the continuous groundplane test-board and the split groundplane test-board. The split groundplane test-board resulted in significantly higher levels of radiation over a large bandwidth.



(a)



(b)

Figure 16: Radiated fields for the test-card installed in a S1000 with (a) the continuous groundplane test-card, and (b) the split groundplane test-card.

4 Conclusion

Designers often use a split groundplane technique to isolate PCB reference planes (signal groundplanes) from "quiet" grounds. This investigation focused on the efficacy of the split groundplane as a deterrent for EMI associated with noisy I/O lines. A test-board was designed and the series impedance provided by the groundplane split was analyzed. A transmission line equivalent circuit was developed to model the groundplane split. The transmission line model was found to have fair agreement up to 1.8 GHz, which was the limit of the test equipment. The model could have been improved through repeated trial-and-error, however, the transmission line model presented gave sufficient results for predicting the high-frequency dependence of the groundplane split. At high-frequencies the groundplane split impedance oscillates between high and low values. Consequently, the groundplane split can not be used to provide a strictly high- or low-impedance over a large bandwidth. The radiated fields for a continuous groundplane and a split groundplane were observed. The radiated fields for the split groundplane were significantly higher over the observed bandwidth. Because of the oscillatory nature of the split groundplane impedance, this study concludes that the split groundplane is an ineffective technique for reducing broadband EMI associated with noisy I/O lines.

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5 Appendix: Test-board Layout Diagrams

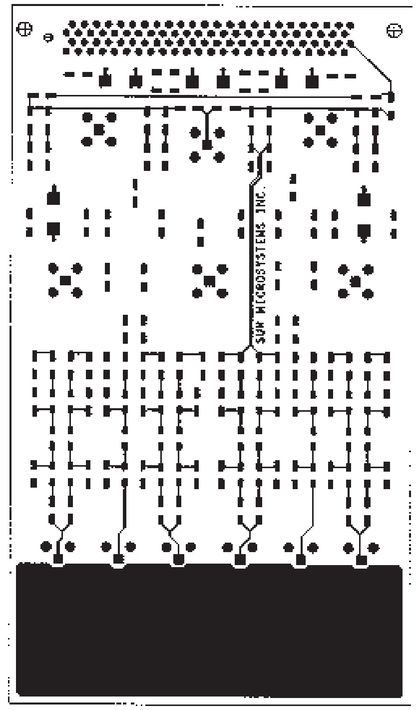

Figure 17: Layer 1 (signal layer) for the continuous groundplane test-board.

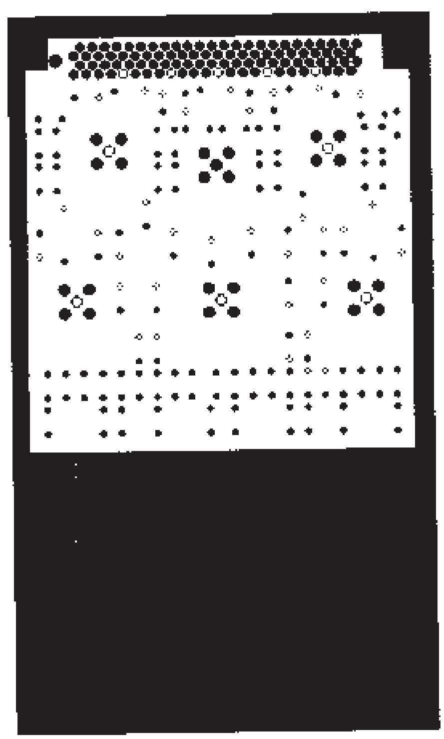

Figure 18: Layer 2 (V_{CC} layer) for the continuous groundplane test-board.

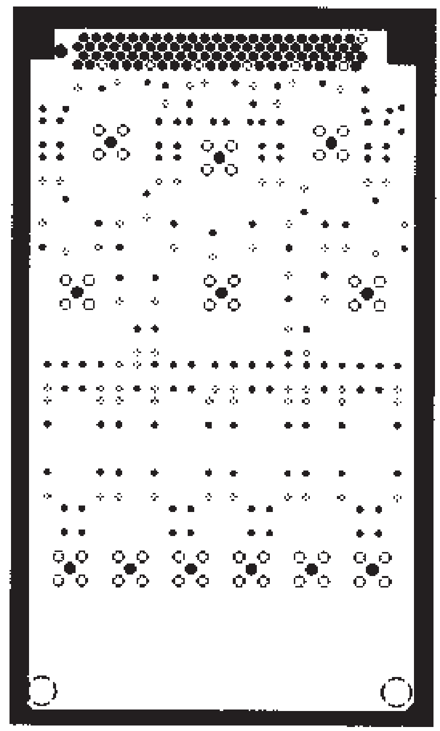

Figure 19: Layer 3 (ground layer) for the continuous groundplane test-board.

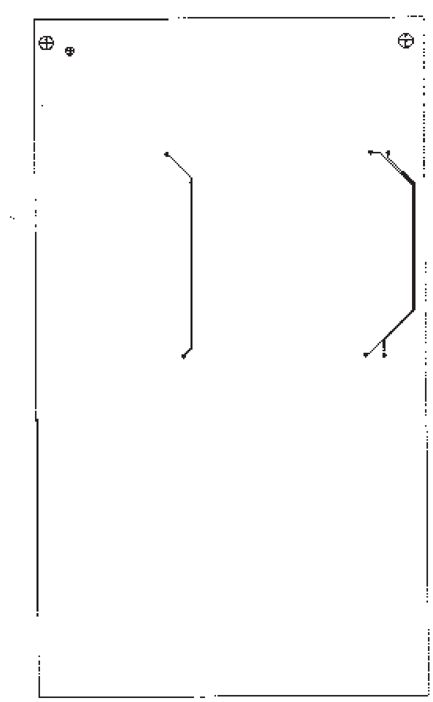

Figure 20: Layer 4 (signal layer) for the continuous groundplane test-board.

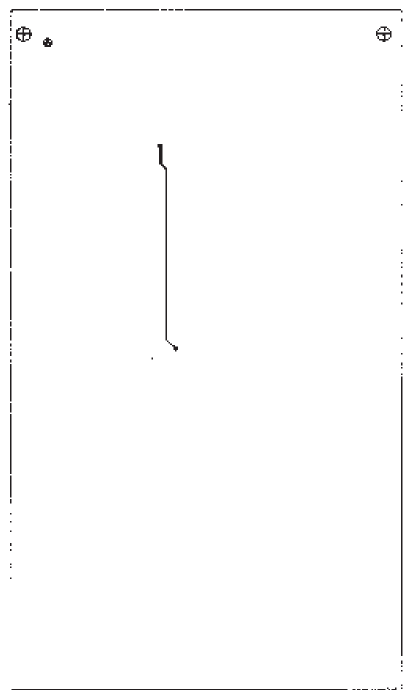

Figure 21: Layer 5 (signal layer) for the continuous groundplane test-board.

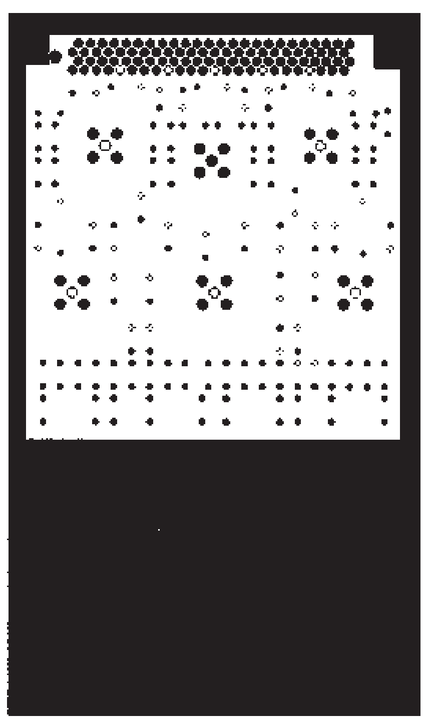

Figure 22: Layer 6 (V_{CC1} layer) for the continuous groundplane test-board.

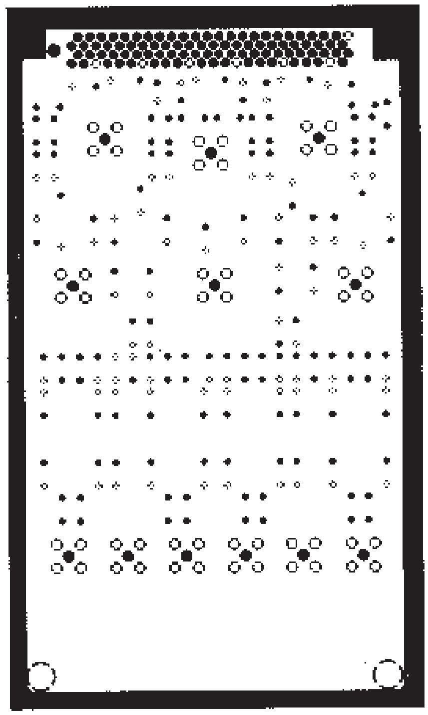

Figure 23: Layer 7 (ground layer) for the continuous groundplane test-board.

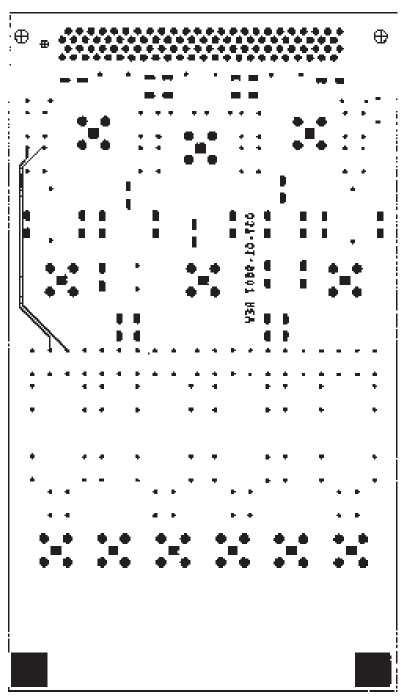

Figure 24: Layer 8 (signal layer) for the continuous groundplane test-board.

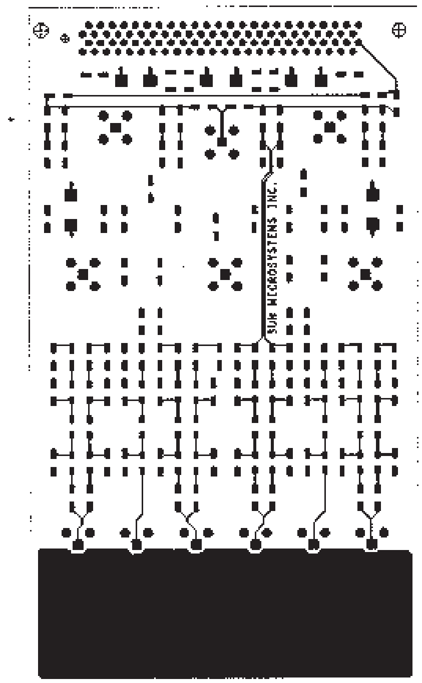

Figure 25: Layer 1 (signal layer) for the split groundplane test-board.

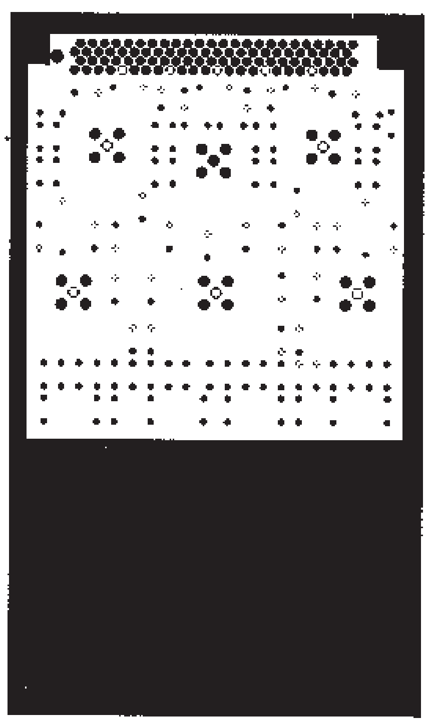

Figure 26: Layer 2 (V_{CC} layer) for the split groundplane test-board.

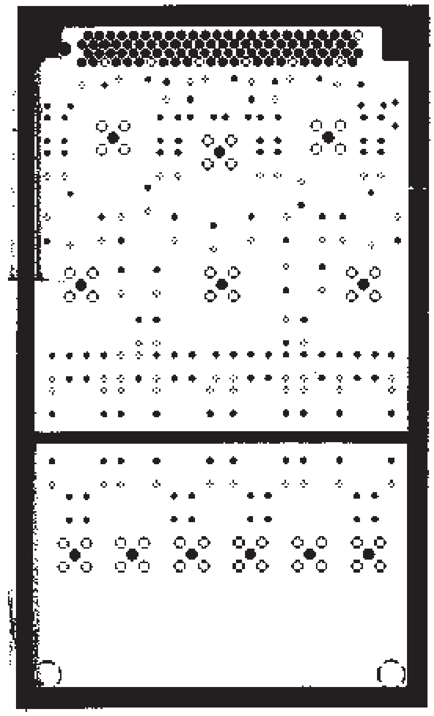

Figure 27: Layer 3 (ground layer) for the split groundplane test-board.

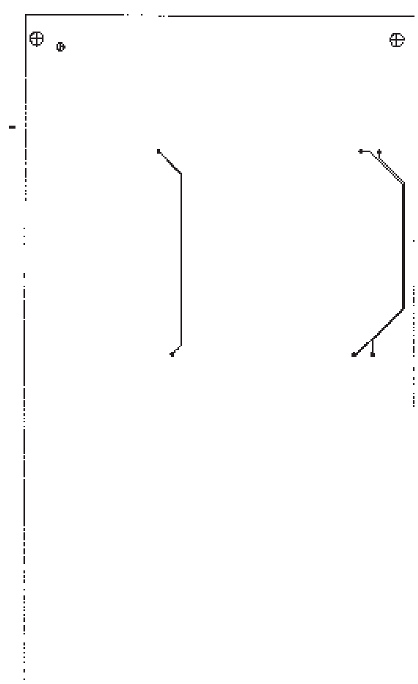

Figure 28: Layer 4 (signal layer) for the split groundplane test-board.

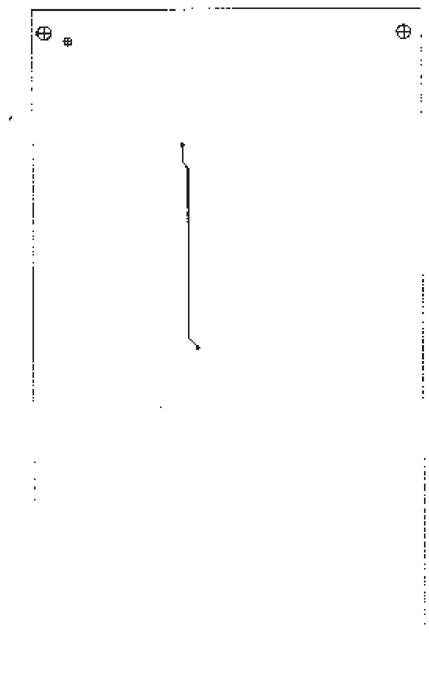

Figure 29: Layer 5 (signal layer) for the split groundplane test-board.

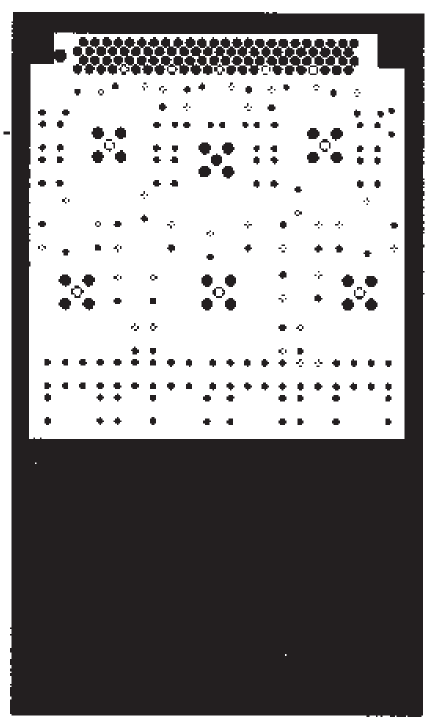

Figure 30: Layer 6 (V_{CC1} layer) for the split groundplane test-board.

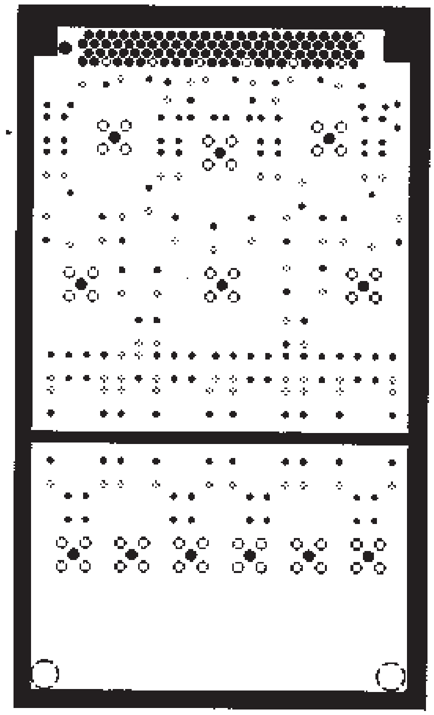

Figure 31: Layer 7 (ground layer) for the split groundplane test-board.

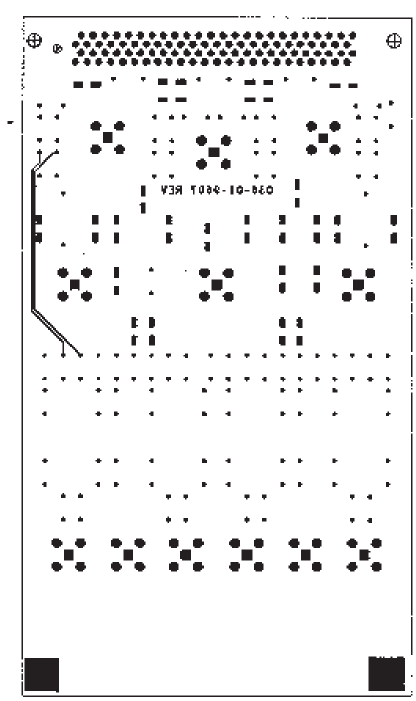

Figure 32: Layer 8 (signal layer) for the split groundplane test-board.