**University of Missouri-Rolla**
**Electromagnetic Compatibility Laboratory**

Title: Power Bus Noise Estimation Algorithm

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# Power Bus Noise Estimation Algorithm

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This algorithm estimates electromagnetic interference (EMI) problems caused by digital circuits injecting transient noise onto the DC buses that power digital devices. The frequency range for this algorithm has been expanded to include some of the power plane resonance effects. This has required a change in the order of the calculations as shown in the **Contents**. This new organization should make it simpler to incorporate future enhancements. Experimental measurements currently indicate that only the narrow-band frequency components contribute significantly to the EMI generated by digital DC power buses. Hence, the broad-band calculations have been removed from this version.

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III-A5 Narrow-Band Power Available and Radiated Electric Field
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Appendix 1 Derivation of an Approximate Expression for the Inductance of a Microstrip Trace

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Appendix 3 Derivation of the Effective Capacitance versus Time for Each DC Power Bus

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## Objectives

Experimental measurements have shown that the DC power buses for the digital circuits on printed circuit boards cause several EMI problems. These problems are associated with either the conduction of high-frequency noise between components connected to the power bus or the coupling of noise to other structures, such as cables and metal enclosures, which serve as antennas to produce far-field radiation.

For each digital DC power bus the objectives are to:

1. determine which decoupling capacitors are ineffective at high frequencies (MHz);
2. calculate the transient peak change in the bus voltage;
3. calculate the narrow-band frequency components of the bus voltage; and
4. estimate the far-field radiation produced by each power bus.

## Assumptions

1. Only digital circuits are considered. This algorithm is concerned with estimating the noise produced on DC power buses at frequencies above 30 MHz. The major sources for this noise are digital integrated circuits. Switch-mode power supplies are another possible source, but they are not considered in this algorithm.

2. At least one pair of power and ground (return) planes are assumed to exist for each digital DC voltage. The majority of high-speed digital circuit boards have power and ground planes. Adequate amounts of high-frequency switching current cannot normally be supplied by a power distribution bus with one or both of the conductors in the form of long, narrow traces.

3. Only capacitors smaller than 200 nF are considered. Capacitors with values greater than about 200 nF usually have a physical size and mounting configuration that results in significant series inductance. This series inductance causes these capacitors to be ineffective for the

suppression of MHz noise. If capacitors larger than 200 nF are considered, then the associated series inductance must not be underestimated. If the series inductance is incorrectly estimated as a small value, then all of the power bus noise levels might be calculated as insignificant, when they could actually be major causes of EMI problems. To avoid the possibility of grossly overestimating the noise reduction of large capacitor values, it is recommended that only capacitors smaller than 200 nF be considered.

4. Only surface mounted capacitors are considered. Thru-hole mounted capacitors are usually not effective above 30 MHz because of excessive series inductance.

5. All of the capacitors connected to an entire power plane are assumed to be usable by any integrated circuit (IC) connected to that plane. This assumption will not be correct for capacitors whose distance from an IC causes a one-way propagation delay that exceeds about one-half of the switching time of the IC. For a total transient current switching time (rise + fall) of 1 ns on a circuit board with a relative dielectric constant of 4.5, the capacitors at a distance greater than 7 cm would not be able to supply charge directly to this IC during switching. However, these capacitors would be able to contribute to the recharging of those capacitors which did supply charge during the switching interval.

6. All HIGH utilization outputs of one IC are assumed to switch simultaneously. The HIGH utilization outputs of different ICs usually switch at times separated by more than the typical switching duration. The varying delays in the initiation of switching are caused by different propagation delays along conductors and within ICs. The HIGH utilization outputs from the same IC are all assumed to switch at the same time. This is not always true, so this does represent a worst case situation. This assumption partially compensates for the previous assumption that all decoupling capacitors on a specific power bus are available to all of the ICs connected to that bus.

7. At each narrow-band frequency, only the largest contribution is used in the EMI estimate. Other contributors are stored for possible future use. If the contributors to the far field at a given frequency were all in time phase, then the total field would be the sum of the individual contributions. If a very large number of contributors had random amplitudes and phases, then the total field would be zero. For circuit boards, a relatively small number of contributors have known amplitudes, but unknown phases. The largest single contributor at each frequency has been assumed to dominate the measured field, current, or voltage.

**General Comments**

A specific digital DC power bus consists of a DC voltage net and a ground (return) net. The integrated circuits (ICs) and lumped decoupling capacitors are always connected between these two nets. Even though two nets are involved, a power bus is often referred to only by the DC voltage net involved. This can cause confusion if more than one ground net is present on the

circuit board. The following algorithms should be thought of as applying to a specific voltage-net/ground-net pair. For brevity in notation voltage-net/ground-net will be referred to as Vnet/Gnet. The ground net should actually be called the return net, but that misconception will not be corrected in this document.

When the term "clock frequency" is used, it generally refers to the fundamental frequency of a clock. This fundamental frequency is usually denoted by $f_o$. There can be several clocks with different fundamental frequencies, so a precise notation or naming scheme may be required to determine exactly which clock $f_o$ is being referenced. When all of the frequencies created by a specific clock are intended, they will be referred to as the clock "harmonic frequencies" and designated by $nf_o$. The harmonic frequencies are assumed to include the fundamental frequency $f_o$.

The maximum frequency for which calculations should be performed depends, of course, on the maximum frequency of the appropriate EMI specification. No specific maximum frequency limit is given in the algorithms.

For each DC bus, there are geometrical dimensions and numerous ICs, capacitors, and clock harmonic frequencies involved. Each algorithm indicates the various parameter values that are to be calculated and stored as algorithm outputs. The preferred method for organizing and storing this data is left to the individual people writing the software based on these algorithms. The grouping of parameters suggested for each algorithm may not be adequate or efficient for numerical computations or reducing memory requirements.

All units are to be in the International System of units. Examples are meter, second, Ampere, Volt, Farad, Henry, Ohm, etc.

## Part I: Power Bus Inductance and Capacitance Algorithms

### I-A1: Locating Decoupling Capacitors

This algorithm determines which capacitors < 200 nF are decoupling capacitors by checking that they are connected between a voltage net and a ground net.

1. Select a digital DC voltage net (Vnet).
2. Search the Vnet for connected capacitors.
   Ignore all capacitors > 200 nF.
3. Check the other side of each capacitor for a connection to any ground net (Gnet).
   Ignore capacitors that are not connected to a ground net.
4. Store the name of each capacitor and the Vnet and Gnet between which it is connected.

**Output from Algorithm I-A1: (Vnet/Gnet, capacitor name)** for each decoupling capacitor connected to a digital DC power bus.

## I-A2: Series Inductance for Each Decoupling Capacitor

For each capacitor:

1. Determine the total trace length $d = d_1 + d_2$ as shown in the figure below. The trace lengths $d_1$ and $d_2$ connect the capacitor solder pads to vias that connect to either the power plane (Vnet) or the ground plane (Gnet).

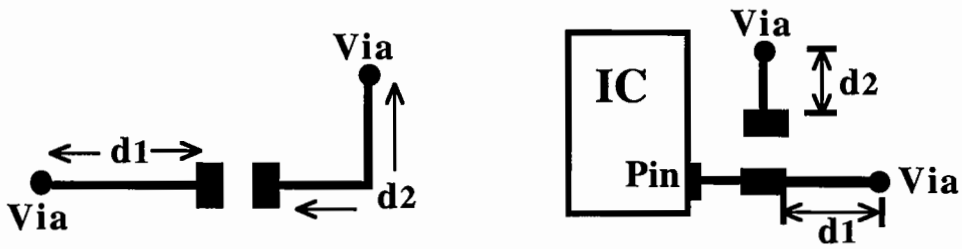


Figure I-A2.1 Identification of the trace length $d = d_1 + d_2$ between capacitor solder pads and the vias to the power and ground (return) planes.

2. Determine the trace width w.
3. Determine the distance to the nearest plane h.
4. Calculate the trace inductance $L_t$ using the following formula for a microstrip line. The value of $L_t$ is in Henries (H), if d is in meters.

$$L_t = 200d[2 + \ln(h/w)]x10^{-9}\ H$$

(See Appendix 1 for a derivation of this expression.)

5. Add 1 nH to account for via, solder pad, and capacitor inductance.

$$L = L_t + 1\ nH$$

6. Store the paired values of series inductance L and capacitance C for each capacitor.

**Output from Algorithm I-A2: (Vnet/Gnet, capacitor name, L, C)** for each capacitor.

## I-A3: Lumped Capacitance and Inductance of Each Set of Digital Power Bus Planes

Background

The power and ground (return) planes are represented by two rectangular parallel planes of length $d_1$, width $d_2$, and separation h. Only areas of the planes which overlap one another are considered. The length $d_1$ is the maximum distance between edges of the rectangular shape that approximates the overlapping area of the planes, as shown in Figure I-A3.1. The solid line represents the boundary of the power plane and the dotted line represents the boundary of the ground (return) plane. If there are multiple power and ground planes, then $d_1$ is determined for each of the overlapping planar areas.

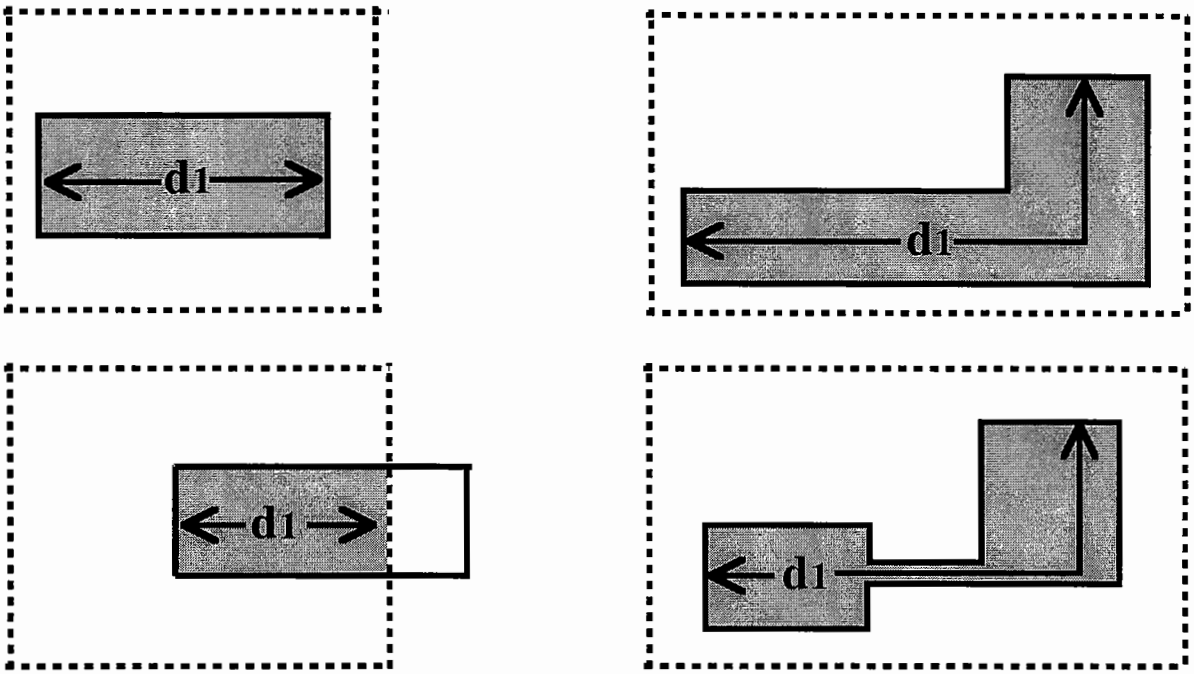

Figure I-A3.1 Examples illustrating the maximum dimension $d_1$ of a rectangular shaped power bus area.

The effective width $d_2$ is determined from the area and $d_1$ by

$$d_2 = \text{Area}/d_1.$$

The distance between the planes is denoted by h.

Multiple power and ground planes operating at the same DC voltage and with similar shaped overlapping areas can be represented by one pair of planes of rectangular dimensions $d_1$ and $d_2$, with an effective separation distance h given by

$$\frac{1}{h} = \frac{1}{h_1} + \frac{1}{h_2} + \ldots + \frac{1}{h_i},$$

where $h_i$ is the distance between the $i^{th}$ pair of planes.

The effective lumped capacitance of the power planes is approximated using the parallel plate capacitance formula as

$$C_p = \frac{\varepsilon_r \varepsilon_o d_1 d_2}{h}.$$

For a one-dimensional transmission line of length d,

$$LC = \mu\varepsilon d^2;$$

where, L and C are the total inductance and capacitance of the line. For the two dimensional geometry of power planes it seems reasonable to let $d^2 = d_1 d_2$, then the effective lumped inductance of the power planes $L_p$ is given by

$$L_p = \mu_o h.$$

This approximation becomes less accurate as the aspect ratio $d_1/d_2$ increases. Most circuit board power planes have $1 < d_1/d_2 < 3$, so the approximation for $L_p$ should apply. This method of calculating $L_p$ uses the geometric mean of two possible values, as shown below.

$$L_p = \sqrt{L_1 L_2} = \sqrt{\left(\frac{\mu_o h d_1}{d_2}\right)\left(\frac{\mu_o h d_2}{d_1}\right)} = \mu_o h$$

Algorithm

1. Select a digital DC power bus Vnet/Gnet.
2. Estimate the area of the planes that overlap.
3. Determine $d_1$, the maximum distance between edges of the rectangular shaped area.
4. Determine h, the separation between the planes.
5. Calculate
   $d_2 = \text{Area}/d_1$.
6. Calculate
   $$C_p = \frac{\varepsilon_r \varepsilon_o d_1 d_2}{h}.$$
7. Calculate
   $L_p = \mu_o h$.
8. Store Vnet/Gnet, $d_1$, $d_2$, h, $C_p$, and $L_p$.
9. Repeat steps 1-8 for each digital DC power bus.

**Output from Algorithm I-A3: (Vnet/Gnet, $d_1$, $d_2$, h, $C_p$, $L_p$)** for each digital DC power bus.

## Part II: Time Domain Calculations

### II-A1 Periodic and Maximum Transient Currents Drawn by Each IC

Background

This algorithm estimates the periodic transient current (Figure II-A1.1) and the maximum single-event transient current (Figure II-A1.2) drawn by each IC from each DC bus supplying power to that IC. The HIGH utilization outputs switch during every clock cycle and contribute to both the periodic and maximum transient currents. A fraction of the MEDIUM utilization outputs also switch every clock cycle and contribute to the periodic transient current. A different fraction of the MEDIUM utilization outputs occasionally switch simultaneously and contribute to the maximum transient current.

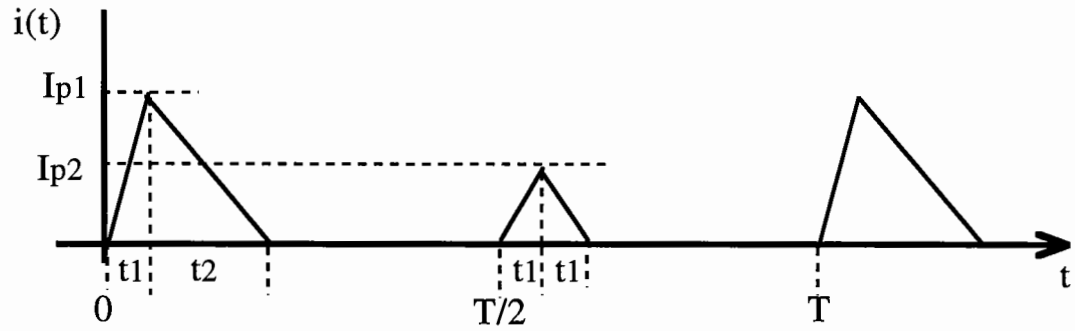

Figure II-A1.1 A triangular approximation to the transient current drawn from the power bus.

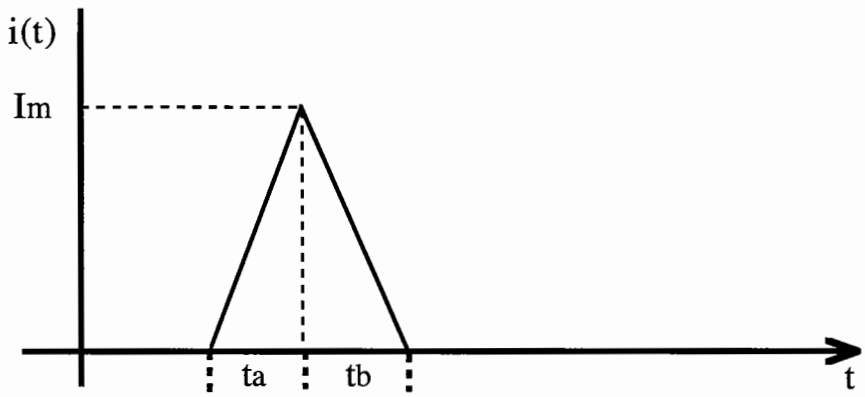

Figure II-A1.2 The triangular approximation to the maximum single-event transient current drawn from the power bus.

The transient current $I_{p2}$ is caused by totem pole transistors both being on briefly during switching. This is sometimes called the "shoot-thru" current and is most noticeable in CMOS devices. The shoot-thru current has a nearly linear rise and fall of approximately equal time intervals $t_1$. The total interval $2t_1 = \Delta t$ is the switching time for that family of IC device.

The transient current $I_{p1}$ is a combination of the internal shoot-thru current and the current required to drive external loads. Many external loads can be approximated as a lumped capacitance $C_L$. In this case the charging current has a waveform that consists of a linear rise and an exponential fall. The exponential fall can be approximated as a linear fall.

For CMOS devices, the periodic peak current $I_{p2}$ can be estimated from the power dissipation capacitance $C_{PD}$. The $C_{PD}$/output value is related to the average power dissipated (P) within the IC due to switching of one output. The typical values for the switching time interval $\Delta t$ and $C_{PD}$ are available for most CMOS devices. For one output switching

$$P = \frac{dW}{dt} = \frac{2(C_{PD}V_{CC}^2/2)}{T} = \frac{2(I_{p2}\Delta t/2)V_{cc}}{T},$$

$I_{p2} = C_{PD}V_{CC}/\Delta t$, and

$t_1 = \Delta t/2$.

The total value of $I_{p2}$ depends on the number of outputs that effectively switch simultaneously every clock cycle.

The periodic peak current $I_{p1}$ is related to both the $C_{PD}$ per output and the capacitive load $C_L$ per output. Experimental measurements have shown that $I_{p1}$ per output can be estimated by

$$I_{p1} = \frac{(C_{PD} + C_L)V_{cc}}{(t_1 + t_2)}.$$

The time interval $t_2$ increases with load capacitance $C_L$, and can be approximated by

$$t_2 = t_1(1 + \frac{C_L}{C_{PD}}).$$

The expressions used to estimate $I_{p1}$, $I_{p2}$, $t_1$ and $t_2$ are expected to change as more experimental measurements are made on a wider array of CMOS devices.

Each output pin of an IC is:

1. associated with a specific DC bus voltage (Vnet);
2. associated with a specific clock fundamental frequency $f_o$; and
3. classified as either HIGH, MEDIUM or LOW utilization.

All output pins of an IC may be grouped according to DC voltage, clock frequency, and utilization. Assume that the outputs have been grouped such that H is the total number of HIGH utilization outputs and M is the total number of MEDIUM utilization outputs associated with a specific DC bus voltage and clock frequency.

A method is needed to estimate the effective number of outputs $H_{eff}$ that switch simultaneously every clock cycle and the maximum number of outputs $N_{max}$ that occasionally switch simultaneously.

The various outputs of an IC can be listed as HIGH utilization clock-like timing outputs, MEDIUM utilization data and address outputs, and LOW utilization control outputs. All LOW utilization outputs are neglected for the transient current calculations.

Most address outputs identify sequentially located groups of machine instruction code. As a result, the lowest order address bit switches nearly every clock cycle and can be treated effectively as one additional HIGH utilization output. The remaining address outputs typically switch every 2, 4, 8, 16, etc. clock cycles. Hence, these outputs collectively represent another HIGH utilization output. The total number of address outputs effectively create two additional HIGH utilization outputs.

Because data outputs are more likely random values rather than sequential values, typically one-half of the data bits switch simultaneously. Since most data pins can be either inputs or outputs, the output function may be active only about one-half of the time.

If the total number of MEDIUM utilization pins is $M < 16$, then it is likely that only data outputs are present with no address outputs. For this situation

$$H_{eff} = H + M/4,$$

where H is the total number of HIGH utilization outputs, M is the total number of MEDIUM utilization outputs, and 1/4 = (1/2)(1/2) comes from 1/2 of the data lines switching 1/2 of the time.

If the total number of MEDIUM utilization pins is $M \geq 16$, then it is likely that an equal number of data outputs and address outputs are present. For this situation

$$H_{eff} = H + 2 + M/8,$$

where the 2 accounts for the effective HIGH utilization of the address outputs and 1/8 = (1/2)(1/2)(1/2) comes from 1/2 of the M outputs being data, 1/2 of which are switching, 1/2 of the time.

The values for $I_m$, $t_a$, and $t_b$ of the maximum transient current waveform shown in Figure II-A1.2 can be determined from $I_{p1}$, $t_1$, and $t_2$ of the periodic transient current waveform. The maximum number of outputs $N_{max}$ that occasionally switch simultaneously is approximately

$$N_{max} = H + M/2.$$

It is assumed that all of the HIGH utilization outputs switch simultaneously, but only a maximum of 1/2 of the MEDIUM utilization outputs might switch simultaneously. The MEDIUM utilization outputs often contain about equal numbers of address and data outputs. There are usually several ns of time skew between the switching of the address output group and the data output group. A time skew greater than the switching interval ($t_1 + t_2$) means that only 1/2 of the MEDIUM utilization outputs can switch simultaneously.

Figure II-A1.3 shows the effect on the maximum current wave shape caused by a random small time skew between outputs that are considered to swtich nearly simultaneously. The switching duration has been assumed to double and the maximum current has reduced by one-half. The areas under each curve are the same and equal the transient charge drawn from the power bus.

The maximum transient current $I_m$ can be related to the periodic current value $I_{p1}$ by

$$I_m = (1/2)\, N_{max} \left( \frac{I_{p1}}{H_{eff}} \right)$$

The factor 1/2 accounts for the amplitude reduction due to time skew, and $I_{p1}/H_{eff}$ is the peak transient current for one output switching.

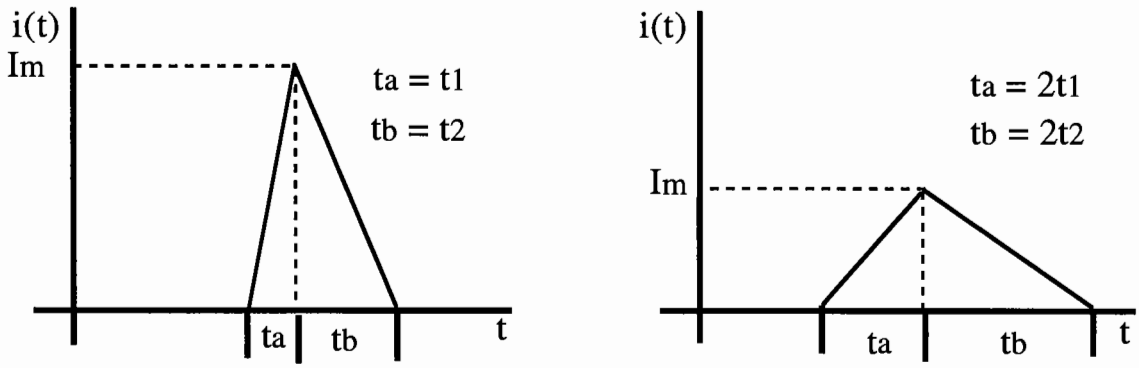


Figure II-A1.3 (a) Current wave shape for a large number of identical outputs switching simultaneously. (b) Current wave shape with a doubling of the switching duration caused by a random small time skew between the outputs.

Periodic and Maximum Transient Current Algorithm

A typical periodic transient current waveform is shown in Figure II-A1.1. This waveform consists of a period T, fundamental frequency $f_o = 1/T$, two peak current values $I_{p1}$ and $I_{p2}$, and two critical time intervals $t_1$ and $t_2$ for each power bus of each IC. For some IC types $I_{p2} = 0$.

Repeat the following for each clock frequency and DC voltage net associated with each IC.

1. Select an IC and identify the logic family type for that IC. See the standard logic types available in the table below.

| Logic Family | Parameters Critical to Transient Current Calculation |
|---|---|
| TTL | //////////////////////////////////// |
| LS | R = 110 Ω, ΔV = 0.6 V, Δt = 6 ns |
| ALS | R = 40 Ω, ΔV = 1.0 V, Δt = 3 ns |
| ABT | R = 40 Ω, ΔV = 1.0 V, Δt = 3 ns |
| FAST | R = 35 Ω, ΔV = 0.6 V, Δt = 2 ns |
| CMOS | //////////////////////////////////// |
| MG | Ignore this type (too slow) Δt > 50 ns |
| HC | $C_{PD}$, switching time Δt<br>Default $C_{PD}$ = 50 pF per output<br>Default switching time Δt = 4 ns |
| FACT | $I_{CCD}$, switching time Δt<br>Default $I_{CCD}$ = 0.31 mA/MHz per output<br>= 310 pC per output<br>Default switching time Δt = 2 ns |
| LVC & LCX | $C_{PD}$, switching time Δt<br>Default $C_{PD}$ = 50 pF per output<br>Default switching time Δt = 3 ns |
| ECL | //////////////////////////////////// |
| 10 H | Δt = 1 ns |
| 10 K | Δt = 3 ns |

| | |
|---|---|
| MECL III | $\Delta t = 1$ ns |
| 100 K | $\Delta t = 0.7$ ns |
| ECL in PS | $\Delta t = 0.5$ ns |
| E-Lite | $\Delta t = 0.25$ ns |

2. Determine the number H of HIGH utilization output pins and the number M of MEDIUM utilization output pins associated with this DC voltage and clock frequency.

3. Calculate the effective number $H_{eff}$ of HIGH utilization outputs.

(a) If $M < 16$, then $H_{eff} = H + M/4$.

(b) If $M \geq 16$, then $H_{eff} = H + 2 + M/8$.

4. If TTL, then obtain R, $\Delta V$, and $\Delta t$ from the table above.

$I_{p1} = H_{eff}(V_{CC} - \Delta V)/R$

$I_{p2} = 0$

$t_1 = \Delta t/2$

$t_2 = 2RC_L = 2R(10\text{ pF})$.

5. If CMOS, then obtain $\Delta t$ and $C_{PD}$ or $I_{CCD}$ for **each output** from the table above. If the logic family is known to be CMOS but is not listed in the table, then use $\Delta t = 3$ ns and $C_{PD}$/output = 30 pF.

a. For $C_{PD}$,

$I_{p2} = H_{eff}C_{PD}V_{CC}/\Delta t$

$t_1 = \Delta t/2$

b. For $I_{CCD}$ (note that the units are mA/MHz),

$C_{PD} = I_{CCD}/V_{CC}$

$I_{p2} = H_{eff}C_{PD}V_{CC}/\Delta t$

$t_1 = \Delta t/2$

c. Estimate the average capacitive load $C_L$ on each output. If no value is available, then assume a default value of $C_L = 15$ pF per output.

d. Calculate $t_2$ and $I_{p1}$

$$t_2 = t_1\left(1 + \frac{C_L}{C_{PD}}\right)$$

$$I_{p1} = \frac{H_{eff}(C_{PD} + C_L)V_{CC}}{(t_1 + t_2)}$$

6. Calculate

$t_a = 2t_1$

$t_b = 2t_2$.

7. Calculate the maximum number of outputs $N_{max}$ that occasionally switch simultaneously.

$$N_{max} = H + M/2$$

8. Calculate

$$I_m = \frac{N_{max} I_{p1}}{2H_{eff}}$$

9. Repeat steps 1-8 for each IC.

**Output from Algorithm II-A1 (Vnet/Gnet, IC#, clock frequency $f_o$, $I_{p1}$, $I_{p2}$, $t_1$, $t_2$, $I_m$, $t_a$, $t_b$)** for each IC, DC bus voltage and clock fundamental frequency.

### II-A2: Transient Peak Change in the Bus Voltage

1. Select the IC with the largest value of $I_m(t_a + t_b)$ for a DC bus Vnet/Gnet.
2. Calculate the effective transient bus capacitance.

   (See Appendix 3 for an explanation of this concept.)

   a. Recall the capacitance $C_p$ and the inductance $L_p$ for the planes of this power bus. Set

$$C(t_a) = \frac{C_p}{1 + 2L_pC_p/t_a^2}$$

   b. Obtain L and C for a decoupling capacitor connected to this bus.

   c. Calculate

$$\Delta C = \frac{C}{1 + 2LC/t_a^2}$$

   d. Increment $C(t_a)$

$$C(t_a) = C(t_a) + \Delta C$$

   e. Repeat steps b, c, and d for each decoupling capacitor and store the final value of $C(t_a)$.

   f. Repeat steps a through e with $t_a$ replaced by $t_b$.

3. Calculate the transient peak change in the bus voltage $\Delta v$ using

$$\Delta v = \frac{I_m t_a}{2C(t_a)} + \frac{I_m t_b}{2C(t_b)}$$

4. Repeat steps 1-3 for each Vnet/Gnet.

**Output from Algorithm II-A2: (Vnet/Gnet, IC#, $\Delta v$)** for each DC bus voltage.

# Part III: Frequency Domain Algorithms

## III-A1 Ineffective Capacitors and the Total Effective Value of the Decoupling Capacitors for Each DC Power Bus

1. For this DC power bus, recall the interplane capacitance $C_p$ from I-A3 and determine all clock fundamental frequencies associated with ICs attached to this bus.
2. Initialize $C_{eff}(nf_o) = 0$ at all of the clock harmonic frequencies.
3. Select a decoupling capacitor described by (C, L) from I-A2 and calculate $C_{test}$ at 30 MHz.

$$C_{test} = \left| \frac{C}{1 - \omega^2 LC} \right|$$

4. If $C_{test} < C_p/10$, then flag this capacitor as ineffective and add this capacitor to the "list of ineffective capacitors".
5. Calculate $\Delta C_{eff}(nf_o)$ at each clock harmonic frequency using the **smaller** of $\left| \frac{C}{1 - \omega^2 LC} \right|$ or 2C. (See Appendix 2 for a derivation of this expression)
6. Increment the values of $C_{eff}$ at each clock harmonic frequency using

$$C_{eff}(nf_o) = C_{eff}(nf_o) + \Delta C_{eff}(nf_o).$$

7. Repeat steps 3-6 for all remaining decoupling capacitors connected to this Vnet/Gnet bus.
8. Repeat steps 1-7 for each Vnet/Gnet.

**Output from Algorithm I-A4: (Vnet/Gnet, $nf_o$, $C_{eff}(nf_o)$, List of Ineffective Capacitors)** for each DC Power bus.

## III-A2 Magnitude of the Bus Impedance

Background

The bus impedance $Z(nf_o)$ is used with the current spectrum $I(nf_o)$ generated by each digital IC to estimate the noise voltage spectrum $V(nf_o)$ produced by that IC on a specific DC power bus. The output of this algorithm is the magnitude of the bus impedance at each clock harmonic frequency. If the ICs connected to a specific DC bus operate at more than one fundamental clock frequency, then the impedance at all of the various clock harmonic frequencies must be calculated and stored.

It may be useful to display the impedance magnitude versus frequency for each digital bus. This data could be used to evaluate the effectiveness of the lumped decoupling capacitors and to show power plane resonances.

The power bus impedance consists of several lumped parallel decoupling capacitors, each

with a lumped series inductance, and a distributed two-dimensional pair of planes. The power and return planes have been previously approximated by a rectangular area of dimensions $d_1$ by $d_2$. The distributed inductance and capacitance of this area can be represented by the two parallel transmission lines shown in Figure III-A2.1. The resistive loading on each line represents the high-frequency power losses produced by the devices connected to the power bus. The total quality factor $Q_T$ for each DC bus determines the extent of the resistive loading. A $Z_L = 2Q_TZ_o = KZ_o$ produces a reasonable loading for each transmission line. Most

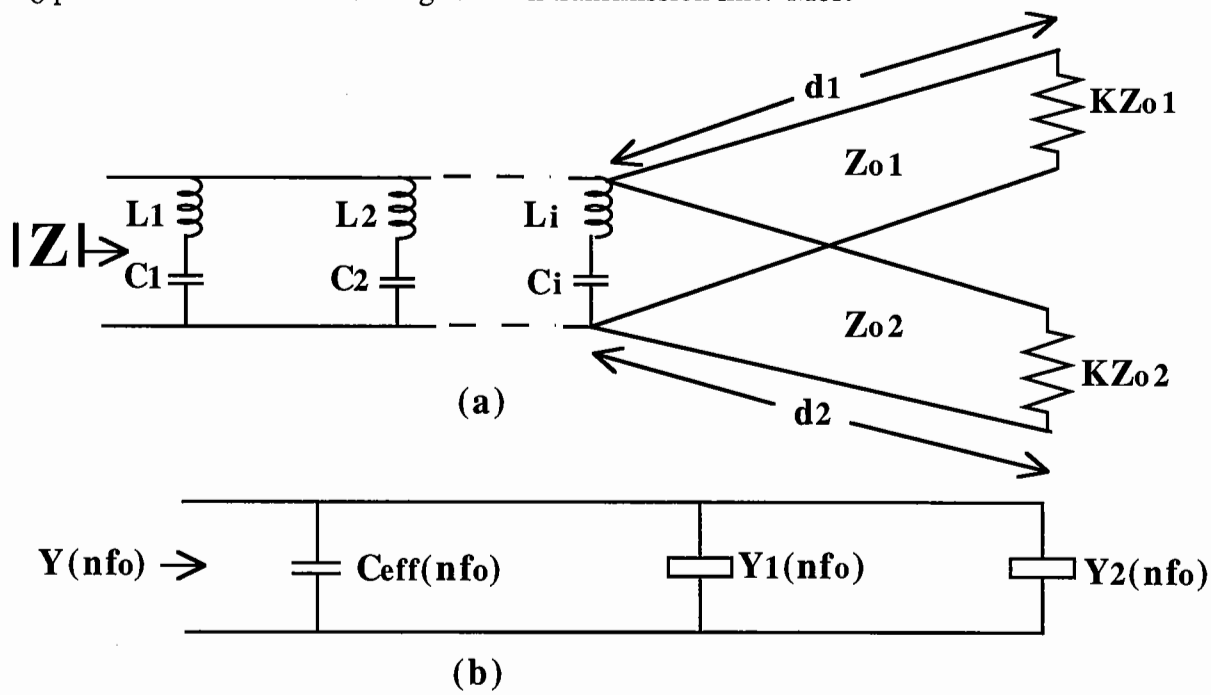


Figure III-A2.1 (a) A combination lumped and distributed model to represent the power bus impedance magnitude. (b) The simplified admittance representation of the power bus.

fully populated digital circuit boards have a $Q_T \approx 10$. So the default value to be used for K is 20. The maximum range for $Q_T$ found experimentally is $3 < Q_T < 100$. A $Q_T = 100$ might correspond to a circuit board without any components attached.

This model is intended to provide only an approximate representation of the variation of bus impedance with frequency. The exact impedance would depend on the detailed shape of the power planes and the precise location of the observation port. The approximate representation should be adequate for power bus noise estimation.

The impedance or admittance of each parallel branch in Figure III-A2.1 will be represented by a magnitude only. The total admittance magnitude will be written as the sum of the admittance magnitudes of each parallel branch. This calculation is not exactly correct, but it should represent a lower bound on the admittance magnitude, since parallel resonances are not included. A lower

bound on the admittance means an upper bound on the impedance. An upper bound on the impedance means that power bus noise voltages and the noise power delivered to the bus will be overestimated. It is best to overestimate rather than underestimate these parameters. The total bus impedance is the parallel combination of the lumped capacitors and the two transmission lines. These three components are shown in the following equation. The vertical pair of bars || stands for "in parallel with".

$$Z(nf_o) = \left[\frac{1}{2\pi nf_o C_{eff}(nf_o)}\right] \| \left[\sqrt{2}Z_{o1}\sqrt{\frac{K^2 + (\tan\beta d_1)^2}{1 + K^2(\tan\beta d_1)^2}}\right] \| \left[\sqrt{2}Z_{o2}\sqrt{\frac{K^2 + (\tan\beta d_2)^2}{1 + K^2(\tan\beta d_2)^2}}\right]$$

$$Y(nf_o) = 2\pi nf_o C_{eff}(nf_o) + 0.5\left[Y_1(nf_o) + Y_2(nf_o)\right] = \frac{1}{Z(nf_o)}$$

where

$$C_{eff}(nf_o) = \Sigma C_{ieff} \quad \text{(from algorithm III-A1)}$$

$$Y_1(nf_o) = Y_{o1}\sqrt{\frac{1 + K^2(\tan n\theta_1)^2}{K^2 + (\tan n\theta_1)^2}}$$

$$Y_2(nf_o) = Y_{o2}\sqrt{\frac{1 + K^2(\tan n\theta_2)^2}{K^2 + (\tan n\theta_2)^2}}$$

$$Y_{o1} = \frac{\sqrt{\varepsilon_r}d_2}{377h} \qquad Y_{o2} = \frac{\sqrt{\varepsilon_r}d_1}{377h}$$

The parameters $d_1$, $d_2$ and h are the effective length, width, and separation of the planes that represent this particular power bus. These values are available from algorithm I-A3. The two $\sqrt{2}$ s in the expression for $Z(nf_o)$ and the value of 0.5 in the expression for $Y(nf_o)$ reflect the fact that the two transmission lines account for the interplane capacitance twice. Hence, the admittance would be too large by a factor of 2 without the multiplier of 0.5.

$$K = 2Q_T = 20$$

$$n\theta_1 = \beta d_1 \qquad n\theta_2 = \beta d_2$$

$$\theta_1 = 2\pi\sqrt{\varepsilon_r\varepsilon_o\mu_o}f_o d_1 \qquad \theta_2 = 2\pi\sqrt{\varepsilon_r\varepsilon_o\mu_o}f_o d_2$$

Algorithm

1. Select a clock frequency $f = nf_o$.
2. Recall $C_{eff}(nf_o)$ for this power bus from algorithm III-A1.

3. Calculate $Y_1(nf_o)$ and $Y_2(nf_o)$.

4. Calculate $Y(nf_o)$

5. Calculate $Z(nf_o) = \frac{1}{Y(nf_o)}$.

6. Store $Z(nf_o)$ and $nf_o$.

7. Repeat steps 1-6 for each clock harmonic frequency $nf_o$.

**Output from Algorithm III-A2: (Vnet/Gnet, $nf_o$, $Z(nf_o)$)** for each power bus.

### III-A3 Narrow Band Frequency Components of the Bus Current

Background

This algorithm calculates the narrow band frequency components of the currents $I(nf_o)$ on each digital DC power bus at the harmonic frequencies of all of the clocks associated with ICs connected to a specific bus. The largest three values at each frequency $nf_o$ and the ICs (IC#) that produce those values are stored for use in other algorithms. Only the largest current produced at each frequency by a single IC is used for EMI calculations. The root-mean-square (RMS) sum of all of the currents produced by all of the ICs would yield a significant overestimate of the current amplitudes.

Three current amplitudes should be stored so that the EMI effects of the second and third largest contributors can be calculated and compared with the largest contributor. If the second largest current amplitude is only slightly less than the largest amplitude, then it can be determined that eliminating the largest contributor will not significantly reduce the EMI.

Algorithm

1. Select a DC power bus Vnet/Gnet.

2. Initialize to zero all elements of three arrays to store the top three current amplitudes at each clock harmonic frequency. $I_1(nf_o, IC\#)$ should contain the largest amplitudes, $I_2(nf_o, IC\#)$ the second largest amplitudes, and $I_3(nf_o, IC\#)$ the third largest amplitudes.

3. Select an IC

4. Recall (IC#, Vnet/Gnet, $f_o$, $I_{p1}$, $I_{p2}$, $t_1$, $t_2$) from algorithm II-A1.

5. Assign $t_{r1} = t_1$, $t_{F1} = t_2$, $t_{r2} = t_1$ and $t_{F2} = t_1$.

6. Calculate $I(nf_o)$ for $nf_o \leq$ the maximum frequency of concern.

Using the notation $f_n = nf = nf_o = n/T$, and $\omega_n = 2\pi f_n$, the amplitude of each harmonic of the Fourier series for the transient current drawn from the power bus is

$$I(nf_o) = \sqrt{a_n^2 + b_n^2},$$

where

$$a_n = -\frac{I_{p1}T}{n^2\pi^2}\left[\frac{\sin^2(\pi f_n t_{r1})}{t_{r1}} - \frac{\sin(\beta_{n1})\sin(\omega_n t_{r1} + \beta_{n1})}{t_{F1}}\right]$$

$$-\frac{I_{p2}T}{n^2\pi^2}\left[\frac{\sin^2(\pi f_n t_{r2})}{t_{r2}} - \frac{\sin(\beta_{n2})\sin(\omega_n t_{r2} + \beta_{n2})}{t_{F2}}\right](-1)^n$$

, and

$$b_n = \frac{I_{p1}T}{n^2\pi^2}\left[\frac{\sin(\pi f_n t_{r1})\cos(\pi f_n t_{r1})}{t_{r1}} - \frac{\sin(\beta_{n1})\cos(\omega_n t_{r1} + \beta_{n1})}{t_{F1}}\right]$$

$$+\frac{I_{p2}T}{n^2\pi^2}\left[\frac{\sin(\pi f_n t_{r2})\cos(\pi f_n t_{r2})}{t_{r2}} - \frac{\sin(\beta_{n2})\cos(\omega_n t_{r2} + \beta_{n2})}{t_{F2}}\right](-1)^n .$$

The following definitions are used.

$$\beta_{n1} = \arctan(\pi f_n t_{F1}) \qquad \beta_{n2} = \arctan(\pi f_n t_{F2})$$

$$\sin(\beta_{n1}) = \frac{\pi f_n t_{F1}}{\sqrt{1 + (\pi f_n t_{F1})^2}} \qquad \sin(\beta_{n2}) = \frac{\pi f_n t_{F2}}{\sqrt{1 + (\pi f_n t_{F2})^2}}$$

$$\cos(\beta_{n1}) = \frac{1}{\sqrt{1 + (\pi f_n t_{F1})^2}} \qquad \cos(\beta_{n2}) = \frac{1}{\sqrt{1 + (\pi f_n t_{F2})^2}}$$

7. Check the arrays storing the three largest values at each frequency to see if any values need to be replaced by the values from $I(nf_o)$ calculated in step 6.
8. Repeat steps 3-7 for each IC.
9. Repeat steps 1-8 for each DC power bus.

**Output from Algorithm III-A3: (Vnet/Gnet, $nf_o$, $I_1(nf_o$, IC#), $I_2(nf_o$, IC#), $I_3(nf_o$, IC#))** for each DC power bus.

### III-A4 Narrow Band Frequency Components of the Bus Voltage

Background

The algorithm uses the largest value of bus current $I_1(nf_o$, IC#) at each clock harmonic

frequency and the magnitude of the bus impedance $Z(nf_o)$ to calculate the magnitude of the narrow band (sinusoidal) bus voltage $V(nf_o, IC\#)$ at each frequency. The bus voltage can be used to estimate EMI conducted and/or radiated from the power bus.

Algorithm

1. Select a DC power bus Vnet/Gnet.
2. Initialize three arrays $V_1(nf_o, IC\#)$, $V_2(nf_o, IC\#)$, and $V_3(nf_o, IC\#)$.
3. Recall (Vnet/Gnet, $I_1(nf_o, IC\#)$, $I_2(nf_o, IC\#)$, $I_3(nf_o, IC\#)$) from III-A3.
4. Recall (Vnet/Gnet, $nf_o$, $Z(nf_o)$) from III-A2.
5. Calculate at each frequency $nf_o$:

   $V_1(nf_o, IC\#) = I_1(nf_o, IC\#)\ Z(nf_o)$;

   $V_2(nf_o, IC\#) = I_2(nf_o, IC\#)\ Z(nf_o)$; and,

   $V_3(nf_o, IC\#) = I_3(nf_o, IC\#)\ Z(nf_o)$.
6. Repeat steps 1-5 for each Vnet/Gnet.

**Output from Algorithm III-A4: (Vnet/Gnet, $nf_o$, $V_1(nf_o, IC\#)$, $V_2(nf_o, IC\#)$, $V_3(nf_o, IC\#)$)** for each DC power bus.

### III-A5 Narrow Band Power Available and Radiated Electric Field

Background

This algorithm calculates and stores the power spectrum available from each digital DC power bus. This power might contribute to either near-field or far-field radiation. The algorithm then calculates the maximum power available for far-field radiation at each frequency $nf_o$ from any one of the power buses. The radiated electric field is calculated from the maximum power available. No summation of noise power from all DC buses is performed. Only the largest value at each frequency from any bus is used in the radiated electric-field calculation.

The following summarizes the procedure and describes some of the key parameters used in the algorithm.

One of the digital DC power buses is selected for evaluation. The effective power bus dimensions of length $d_1$, width $d_2$, and plane separation h are recalled from algorithm I-A3.

The largest values of the bus current spectra $I_1(nf_o, IC\#)$ and voltage spectra $V_1(nf_o, IC\#)$ are recalled.

The ratio of total loaded power bus quality factor $Q_T$ to the bus radiation quality factor $Q_R$ is calculated from

$$Q_T/Q_R = 100h[|\sin(\beta d_1/2)| + |\sin(\beta d_2/2)|].$$

The factor of 100 has been determined from experimental measurements. Experimental measurements also showed that $Q_T/Q_R$ varied with the plane separation h. The plane separation h should be in meters. For example, $Q_T/Q_R = 0.1$ at resonance for h = 1 mm. The $\sin(\beta d/2)$ terms

partially account for resonance effects associated with the bus dimensions $d_1$ and $d_2$.

A shielding effectiveness factor S is used to account for the added self shielding produced by 3 or more planes in a stripline Ground-Power-Ground configuration as compared to only 2 planes in a microstrip Ground-Power configuration. Use S = 1 as a default value, or S = 0.3 for 4 or more overlapping planes. Four planes are required instead of just 3 to avoid the possibility of a Ground-Ground-Power stackup which would not produce the stripline configuration.

The power available is calculated by

$$P_a(nf_o, IC\#) = I_1(nf_o, IC\#)V_1(nf_o, IC\#)(Q_T/Q_R)S.$$

The current-voltage product does not include the phase angle as in normal power calculations. It is assumed that all of the power delivered by the switching ICs to the power bus, even the reactive power which represents energy storage, is eventually dissipated as heat or radiated from the bus. The calculated power available spectrum is stored for each bus.

The maximum power available $P_m(nf_o, IC\#)$ at each frequency is calculated by selecting the largest value from any one of the various DC power buses. No RMS sum of values from all buses is used.

The radiated electric field is calculated assuming isotropic radiation into a hemisphere. The hemisphere, instead of a full sphere, accounts for the ground plane present in all far field measurements.

$$E^2/Z_o = P_m/2\pi R^2$$

$$Z_o = 120\pi\ \Omega$$

$$E = 7.75\sqrt{P_m}/R$$

If R = 3m, then

$$E = 2.6\sqrt{P_m}.$$

The radiation into the hemisphere has been assumed to be isotropic. No additional antenna gain, other than that caused by the ground plane, has been assumed.

Algorithm

1. Select a DC power bus Vnet/Gnet.
2. Recall $d_1$, $d_2$, and h for that power bus from algorithm I-A3.
3. Recall the peak current spectra $I_1(nf_o, IC\#)$ from algorithm III-A3.
4. Recall the peak voltage spectra $V_1(nf_o, IC\#)$ from algorithm III-A4.
5. Calculate

$$\frac{Q_T}{Q_R} = 100h\left[\left|\sin\left(\frac{\beta d_1}{2}\right)\right| + \left|\sin\left(\frac{\beta d_2}{2}\right)\right|\right],$$

where $\beta = 2\pi\sqrt{\varepsilon_r\varepsilon_o\mu_o}\,(nf_o)$.

6. Set

S = 1, as a default

or

$S = 0.3$, if the power bus consists of 4 or more overlapping planes.

7. Calculate

$$P_a(nf_o, IC\#) = I_1(nf_o, IC\#)V_1(nf_o, IC\#)(Q_T/Q_R)S.$$

8. Store $P_a(nf_o, IC\#)$ and Vnet/Gnet for each bus.

9. Select the largest value of $P_a(nf_o, IC\#)$ and store as $P_m(nf_o, IC\#, Vnet/Gnet)$.

10. Repeat steps 1-9 for each digital DC power bus Vnet/Gnet.

11. Calculate

$$E(nf_o, IC\#, Vnet/Gnet) = 2.6\sqrt{P_m(nf_o, IC\#, Vnet/Gnet)}$$

**Output from Algorithm III-A5: $P_a(nf_o, IC\#)$ for each power bus, plus $P_m(nf_o, IC\#, Vnet/Gnet)$ and $E(nf_o, IC\#, Vnet/Gnet)$.**

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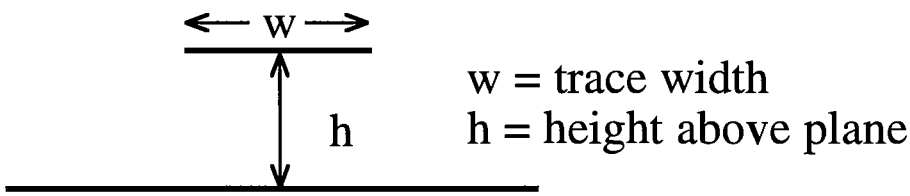
## Appendix 1. Derivation of an Approximate Expression for the Inductance of a Microstrip Trace.

The cross-sectional view of a microstrip line, a trace above a plane, is shown below.




For $h/w < 0.1$, the self inductance $L = (\mu d)(\frac{h}{w})$, (1-1)

where $\mu$ is the permeability of the medium and d is the trace length.

For $h/w > 10$, $L = (\mu d)\left[\frac{\ln\left(\frac{2h}{a}\right)}{2\pi}\right] = (\mu d)\left[\frac{\ln\left(\frac{2\pi h}{w}\right)}{2\pi}\right]$. (1-2)

In this expression the circumference of the trace has been set equal to the circumference of an equivalent round conductor of radius a. That is $2w = 2\pi a$. This equivalence assumes that the current is uniformly distributed around the perimeter of the flat trace. This is not exactly true, but is a reasonable approximation for $h/w > 10$.

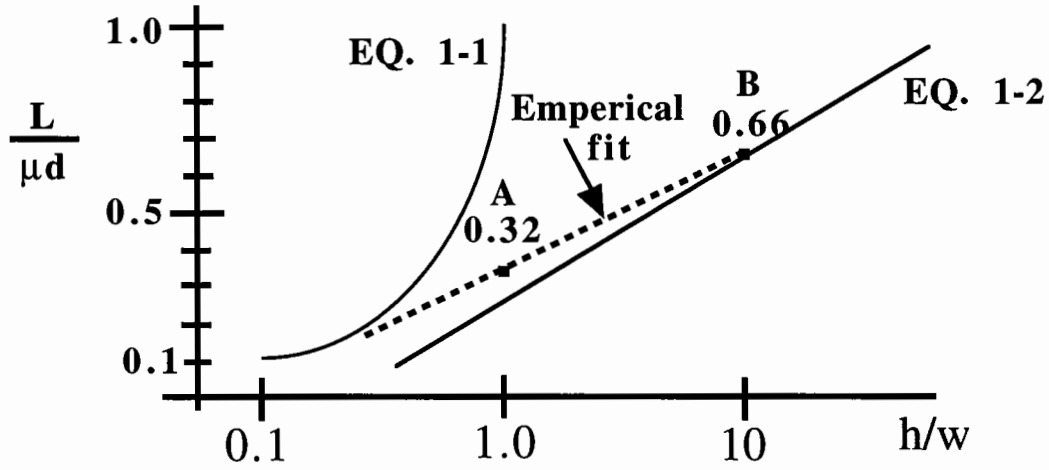
For printed circuit boards $h/w \approx 1$, and neither of the above formulas is a good approximation for the self inductance. Both formulas are plotted on the following graph. An empirical formula has been selected for the range $0.5 < h/w < 10$ that fits the two points A and B.

Point B was determined from Equation 1-2. Point A was determined from a graphical solution. The empirical formula for the inductance of a microstrip trace with $0.5 < h/w < 10$ is

$$L_t = (\mu d)[0.32 + 0.16\ln(h/w)].$$

Using $\mu = \mu_o = 4\pi x10^{-7}$ H/m, the trace inductance becomes

$$L_t = 200d[2 + \ln(h/w)]x10^{-9} \text{ H}.$$




## Appendix 2. Derivation of the Effective Capacitance Versus Frequency for Each DC Power Bus

A series L-C circuit has an impedance magnitude

$$|Z| = |j\omega L - j/\omega C|.$$

For this algorithm only the magnitude of the impedance is important. This impedance magnitude expression can be rearranged into the equivalent form

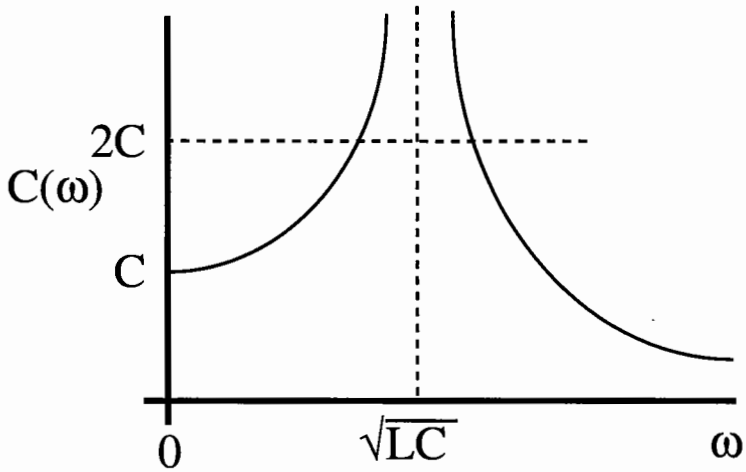
$$|Z| = \left| \frac{-j}{\omega\left[\frac{C}{1-\omega^2 LC}\right]} \right| = \frac{1}{\omega C(\omega)},$$

where

$$C(\omega) = \left| \frac{C}{1-\omega^2 LC} \right|.$$

$C(\omega)$ is the effective value of capacitance that produces the same impedance magnitude variation with frequency as the original L-C series circuit. A sketch of $C(\omega)$ versus $\omega$ is shown in the next

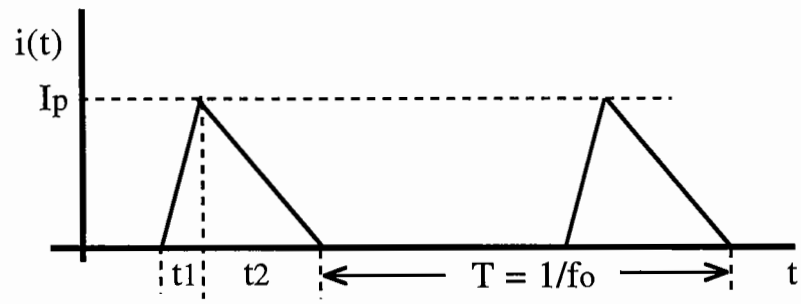
figure.




If series resistance had been included, then the pole in C(ω) at $\omega = \sqrt{LC}$ would have a finite maximum. For this algorithm the effective capacitance is limited to the smaller of $\left|C/(1-\omega^2 LC)\right|$ or 2C.

## Appendix 3. Derivation of the Effective Capacitance versus Time for Each DC Power Bus

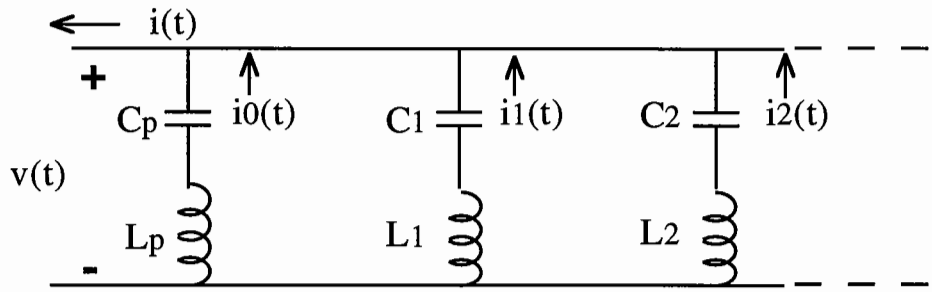
When an integrated circuit output switches, the typical transient current drawn from the DC power bus has the waveform shown below. The total switching time is composed of two time intervals $t_1$ and $t_2$ over which the transient current is assumed to vary linearly with time.




An estimate is required for the peak change in DC bus voltage produced by the transient switching current. If the DC bus were an ideal lumped capacitor C, then the change in bus voltage could be calculated from

$$\Delta v = v(t+\Delta t) - v(t) = \frac{1}{C}\int_t^{t+\Delta t} i(t)dt = \frac{\Delta Q}{C}.$$

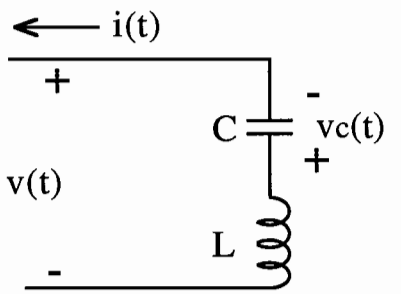
An actual DC power bus usually consists of a distributed capacitance and inductance formed by two or more conducting planes, plus numerous lumped decoupling capacitors each with a series inductance, as shown below. $C_p$ and $L_p$ are a lumped approximation to the distributed capacitance and inductance of the power planes. The subscript p refers to planes. This model of the power bus is not exact, but is reasonable for switching times ($t_1 + t_2$) that are greater than or approximately equal to the propagation delay along the largest dimension of the power bus.




The following describes a method for approximating the time-**in**dependent power bus L-C network as a collection of time-**de**pendent transient capacitances. The total effective transient capacitance that represents the entire bus is determined, and the transient change in the bus voltage is calculated from

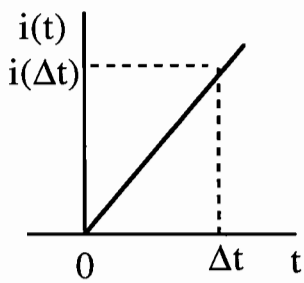
$$\Delta v = \frac{I_p t_1}{2C(t_1)} + \frac{I_p t_2}{2C(t_2)}.$$

Consider the following individual L-C series circuit for which i(t) is known and v(t) is to be determined.




$i(0) = 0$

$v_c(0) = -V_o$




The differential equation relating v(t) to i(t) is

$$v(t) + L\frac{di(t)}{dt} + v_c(0) + \frac{1}{C}\int_0^t i(\alpha)d\alpha = 0.$$

Replacing t with $\Delta t$ yields

$$v(\Delta t) + L\frac{di(\Delta t)}{dt} + v_c(0) + \frac{1}{C}\int_0^{\Delta t} i(\alpha)d\alpha = 0.$$

Assuming that $\Delta t$ is small and that i(t) varies linearly with time over the interval $0 \le t \le \Delta t$, the above equation can be approximated by

$$v(\Delta t) + L\left[\frac{i(\Delta t) - i(0)}{\Delta t}\right] + v_c(0) + \frac{1}{C}\left[\frac{[i(\Delta t) + i(0)]\Delta t}{2}\right] = 0.$$

Substituting $i(0) = 0$ and $v_c(0) = -V_o$ and rearranging yields

$$\Delta v = V_o - v(\Delta t) = \left[\frac{L}{\Delta t} + \frac{\Delta t}{2C}\right] i(\Delta t).$$

Further rearranging yields

$$\frac{i(\Delta t)\Delta t}{2} = \Delta Q = \left[\frac{C}{1 + 2LC/\Delta t^2}\right]\Delta v = C(\Delta t)\Delta v,$$

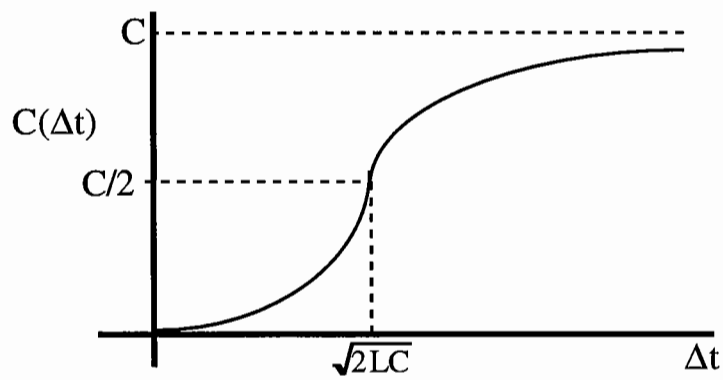
where,

$$C(\Delta t) = \frac{C}{1 + 2LC/\Delta t^2}.$$

$C(\Delta t)$ is the effective time-dependent capacitance that relates $i(\Delta t)$ to $\Delta v = V_o - v(\Delta t)$. If $i(\Delta t)$ is known, then the change in voltage $\Delta v$ can be estimated by

$$\Delta v = \frac{i(\Delta t)\,\Delta t}{2C(\Delta t)}.$$

A sketch of $C(\Delta t)$ versus $\Delta t$ is shown below.



For $\Delta t \rightarrow 0$, $C(\Delta t) = \Delta t^2/(2L)$. This suggests that for a short transient time interval (small $\Delta t$ and high frequencies) the effective time-dependent capacitance value is totally determined by the series inductance L. For a long transient time interval (large $\Delta t$, slowly changing waveform and low frequencies), the effective capacitance value is equal to the actual capacitance value.

For the entire power bus

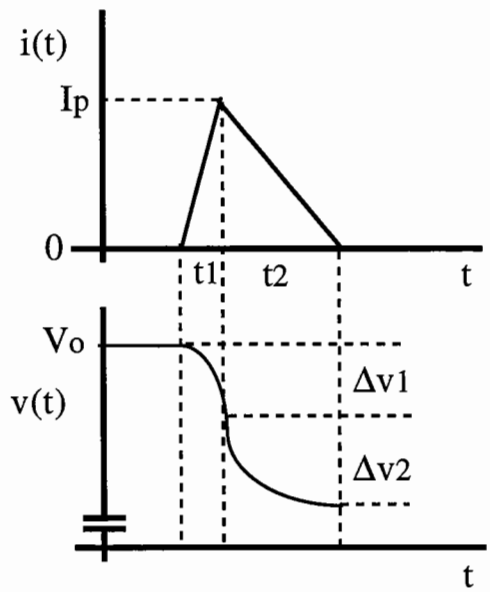
$$\Delta Q = \Delta Q_o + \Delta Q_1 + \Delta Q_2 + \ldots,$$

$$\Delta Q = C(\Delta t)\Delta v = [C_o(\Delta t) + C_1(\Delta t) + C_2(\Delta t) + \ldots]\Delta v,$$

$$C(\Delta t) = \frac{Cp}{1 + 2LpCp/\Delta t^2} + \frac{C_1}{1 + 2L_1C_1/\Delta t^2} + \frac{C_2}{1 + 2L_2C_2/\Delta t^2} + \ldots$$

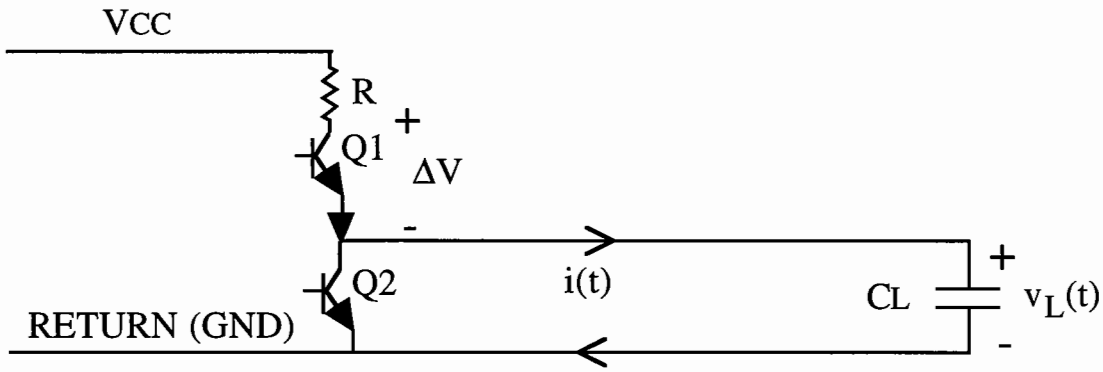
The transient current waveform i(t) shown below, will produce the approximate transient voltage waveform v(t) shown below. The total peak change in the power bus voltage can be estimated from

$$\Delta v_{total} = \Delta v_1 + \Delta v_2 = \frac{I_p t_1}{2C(t_1)} + \frac{I_p t_2}{2C(t_2)}.$$

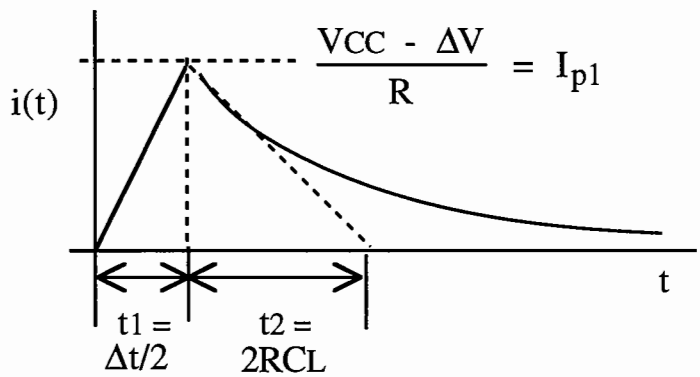


## Appendix 4. Derivation of the Transient Current Waveshape for TTL Outputs

The following circuit represents a TTL "totem pole" output with a load capacitance $C_L$.




Assume that Q1 is turning on, Q2 is turning off, and $v_L(t) = 0$ at $t = 0$. Assume that the time required for Q1 to turn on, $t_1$, is one-half of the rated switching time, $\Delta t$, for this TTL logic family. Then $t_1 = \Delta t/2$. The collector-to-emitter voltage for Q1 at saturation (turned on) plus the diode forward voltage drop is represented by $\Delta V$. The transient current i(t) is given by the following approximate waveform.




For an exponential waveform, the fall time between 90% and 10% values is 2.2x(time constant). Hence, the fall time $t_2$ is approximated by $t_2 = 2RC_L$. The voltage $\Delta V$ varies between about 0.6V and 1.0V for different TTL logic families. The series resistance R varies between 35 Ω $\leq R \leq$ 110 Ω. The TTL families with the smaller values of R naturally have the shorter switching times $\Delta t$.