UNIVERSITY OF MISSOURI-ROLLA
ELECTROMAGNETIC COMPATIBILITY LABORATORY

Title: Experimental Results for Power Bus Decoupling In 4-Layer Printed Circuit Boards

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ABSTRACT

This report presents experimental results for the study of high frequency decoupling capacitors in 4-layer printed circuit boards. The test boards, test setup and test procedure are described in detail. All experimental results (plots) are included without drawing general conclusions.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

1. Test Boards Layout

Three test boards were employed in this study. Board 1 was a 4-layer personal computer motherboard provided by a chip manufacturer. It was fully populated with a large number of components. Figure 1.1 shows the geometry of this board. The power plane was divided into two power islands, Region1 and Region 2. On Region 1, 7 bulk decoupling capacitors and 29 local decoupling capacitors connected to the power and return planes were identified. On Region 2, 4 bulk decoupling capacitors and 24 local decoupling capacitors were identified. The values of the bulk decoupling capacitors were 100 μF, 22 μF, or 10 μF. The values of the local decoupling capacitors were 1 μF or 0.47 μF. The measured inter-plane capacitance of the power bus was 1.4 nF in Region 1 and 1.2 nF in Region 2. The bonding pads of the decoupling capacitors used in the experiments are also labeled in Figure 1.1. Board 2 was an unpopulated version of Board 1.

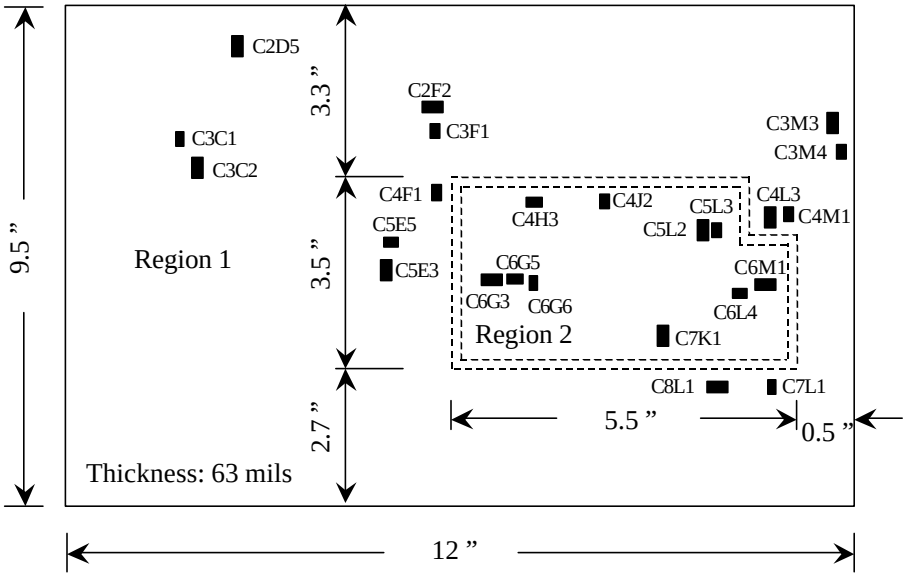

Figure 1.1. Layout of Boards 1 and 2

Board 3 was a mock-up of Board 2. As shown in Figure 1.2, the 2-layer mock up board has the same width and length as Board 2. The shapes of the power islands are also similar, but the spacing between the power and return layers is about 50 mils instead of 40 mils for the motherboard. There is a 100-mil gap between Region 1 and Region 2. Three short 85-mil diameter semi-rigid probes were attached between power and return planes at locations L1, L2, and L3 to make the S-parameter measurements. Figure 1.3 is a photo of Board 3 showing the gapped power plane.

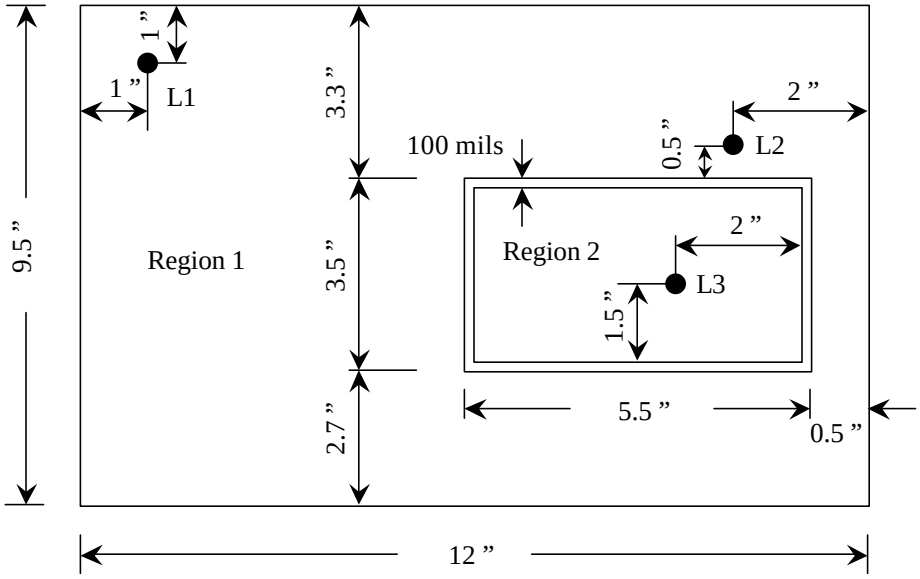

Figure 1.2. Mock-Up Board Layout

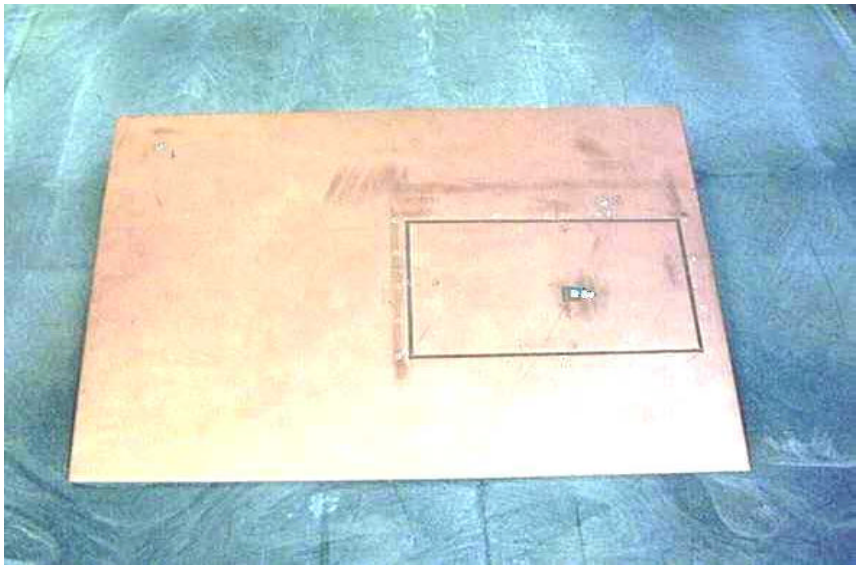

Figure 1.3. Board 3

2. Experimental Setup

Low impedance 85-mil diameter semi-rigid probes were attached to the power and return planes at two locations through the bonding pads of the existing decoupling capacitors. An HP8753D network analyzer was connected to the probes through two low-loss precision cables as illustrated in Figure 2.1. A 12-term error correction model using open, short, and matched loads was used in the calibration. Port extension was performed to move the measurement plane to the coax feed terminals. $|S_{21}|$, the ratio of the transmitted signal at Port 2 to the injected signal at Port 1, was measured. Figure 2.2 shows an $|S_{21}|$ measurement being made using the network analyzer. Figure 2.3 shows a close-up of the probe soldered to the board and connected to the cable. The procedure of S-parameter measurement is described in detail in the appendix..

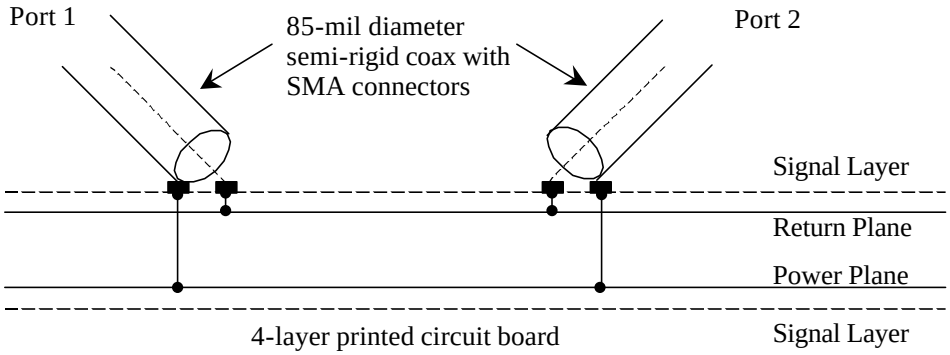

Figure 2.1. Test Configuration for Measuring $|S_{21}|$

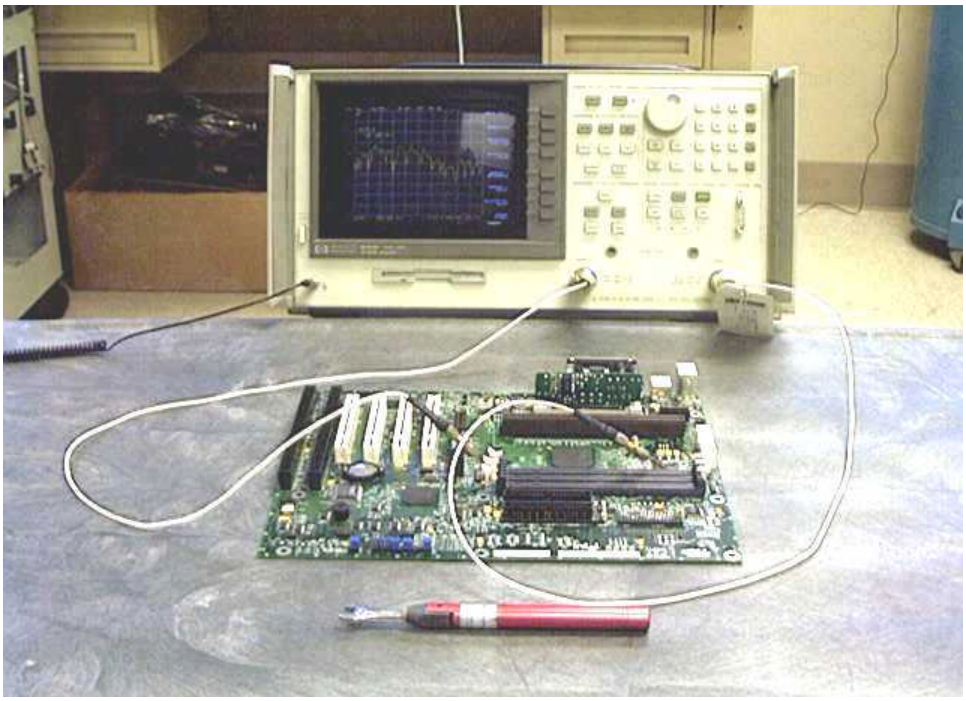

Figure 2.2. Measuring $|S_{21}|$ Using HP8753D Network Analyzer

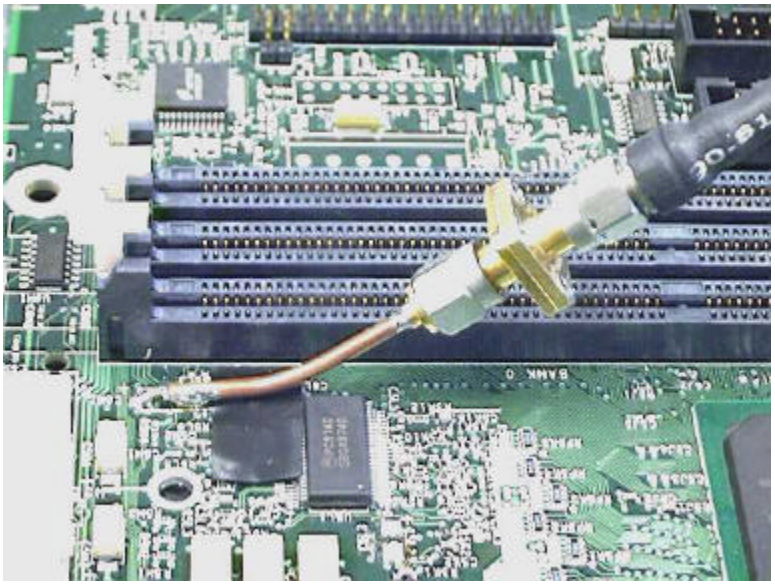

Figure 2.3. A Close-Up of Probe Connected to Board and Cable

3. Decoupling in Board 1

Board 1 was a populated computer motherboard. Figure 3.1 shows the board decoupling when decoupling capacitors were removed from Board 1. Ports were located at C5L2 and C2D5. For the blue curve, two capacitors at C2D5 and C5L2 were removed to attach the probes. For the red curve, another six capacitors at C3C2, C8L1, C7K1, C5L3, C4L3, and C4M1 were removed from the board.

Figure 3.2 shows the effect of the existing bulk and local decoupling capacitors on Region 2 of Board 1. The two ports were located at C6G3 and C6M1. The measured $|S_{21}|$ with all decoupling capacitors in place are shown by the blue curve. Three 100 nF high frequency decoupling capacitors at C6G5, C6G6, and C6L4 were then removed from the board (see the red curve). Next, another 21 decoupling capacitors distant from both ports on Region 2 were removed from the board (see the green curve).

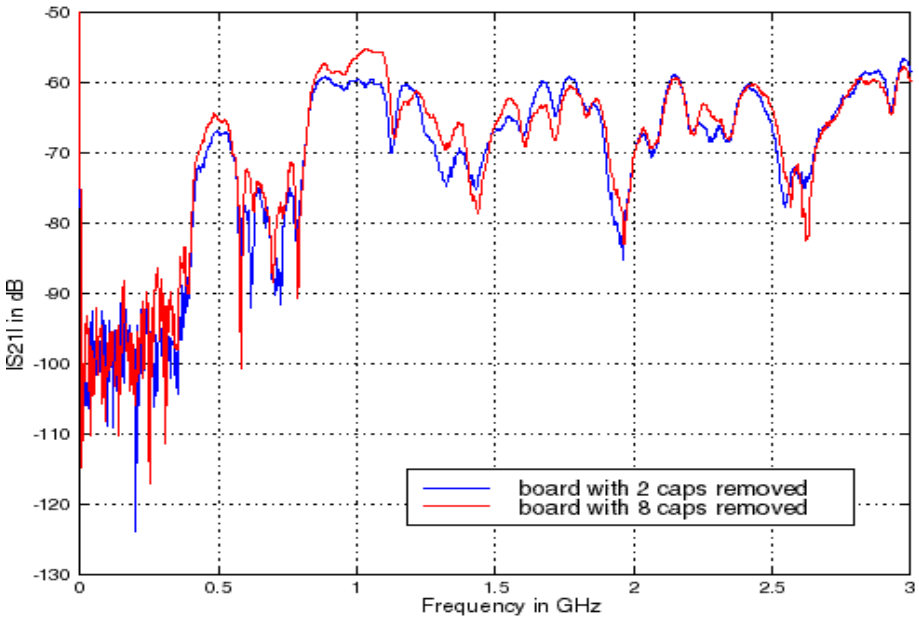

Figure 3.1. Effect of Existing Decoupling Capacitors on Board 1

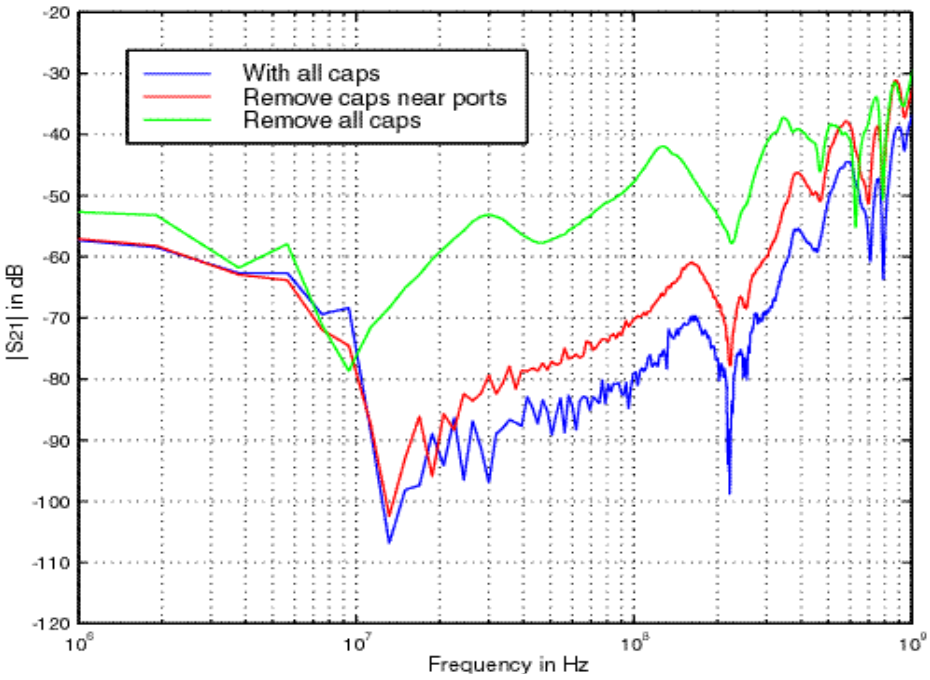

Figure 3.2. Effect of Existing Decoupling Capacitors on Region 2 of Board 1

4. Decoupling in Board 2

Board 2 was an unpopulated version of Board 1. Figure 4.1 shows the effect of a 100 nF capacitor attached to Board 2. The two ports were located at C3F2 and C5E3 on Region 1. The 100nF capacitor was attached to the board at C3F1, C5E5 and C3C1. Among these locations, C3F1 is close to Port 1, C5E5 is close to Port 2, and C3C1 is distant from both ports.

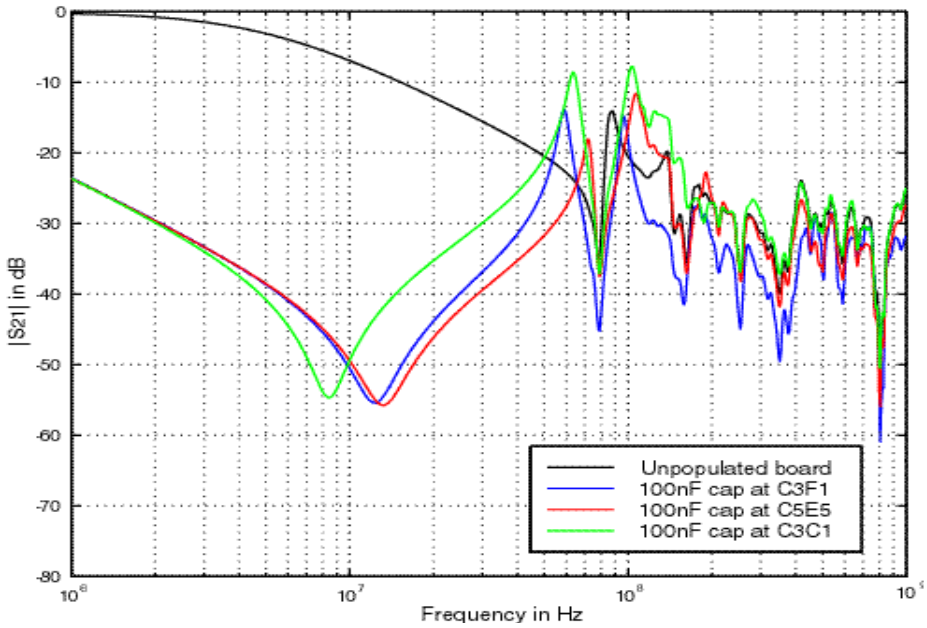

Figure 4.1. Effect of Attached Decoupling Capacitor on Board 2

Figure 4.2 compares the interconnection inductance of the three locations used in the previous experiment. A wide strip of copper tape was used to short the bonding pads and the $|S_{21}|$ parameters were measured.

Figure 4.3 demonstrates the effect of mutual inductance on power bus decoupling. Linear frequency is used to show the decoupling at high frequency band. Port 1 was located at C6G3 and Port 2 was located at C6M1. A 100 nF capacitor was attached at C6G5 and C4J2.

Figure 4.4 illustrates the effect of a 100 nF decoupling capacitor as a function of the distance from one port. The ports were located at C5E3 and C3C2. The capacitor was attached at four locations from the closest location C5E5 to the farthest location C4F1.

Figure 4.5 and Figure 4.6 show the effect of the decoupling capacitors near one or both ports. For Figure 4.5, the ports were located at C3C2 and C5E3 on Region 1. The 100 nF capacitors were attached at C3C1 near port 1 and C5E5 near port 2. For Figure 4.6, the ports were located at C6G3 and C5L2 on Region 2. The capacitors were attached at C6G5 near port 1 and C5L3 near port 2.

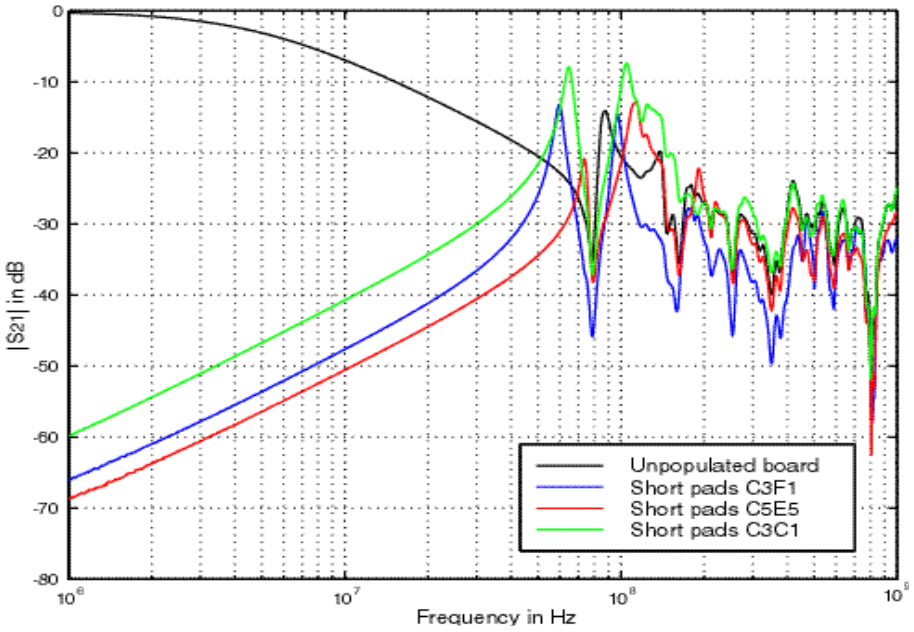

Figure 4.2. Comparison of Interconnection Inductances

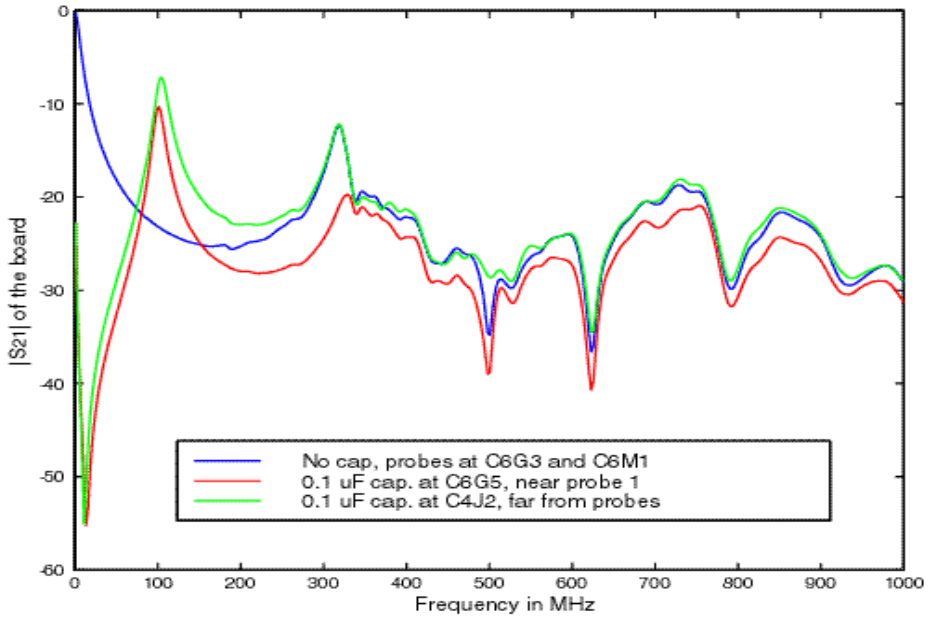

Figure 4.3. Effect of Capacitor Distant to or in Proximity With Ports

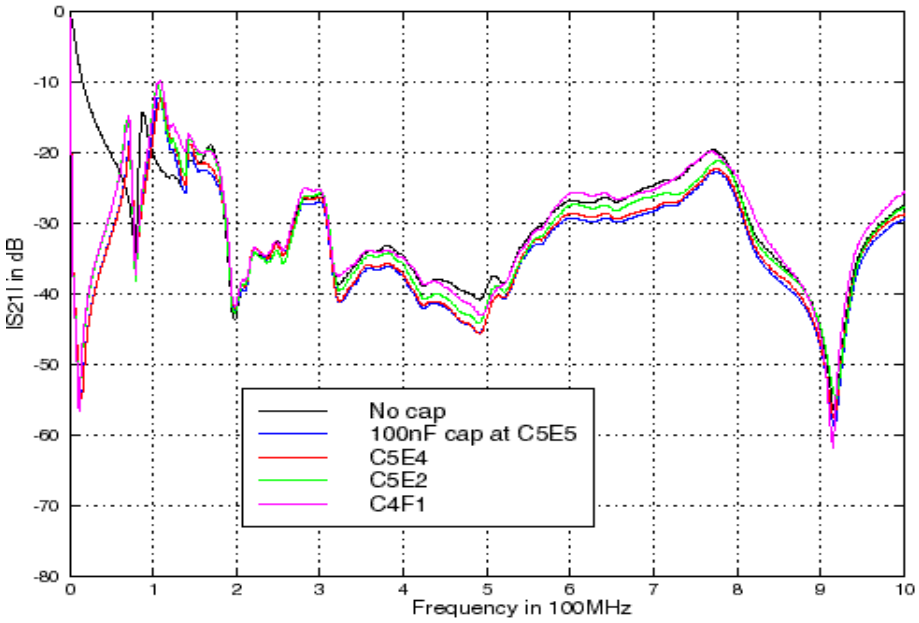

Figure 4.4. Effect of Decoupling Capacitor as a Function of Distance

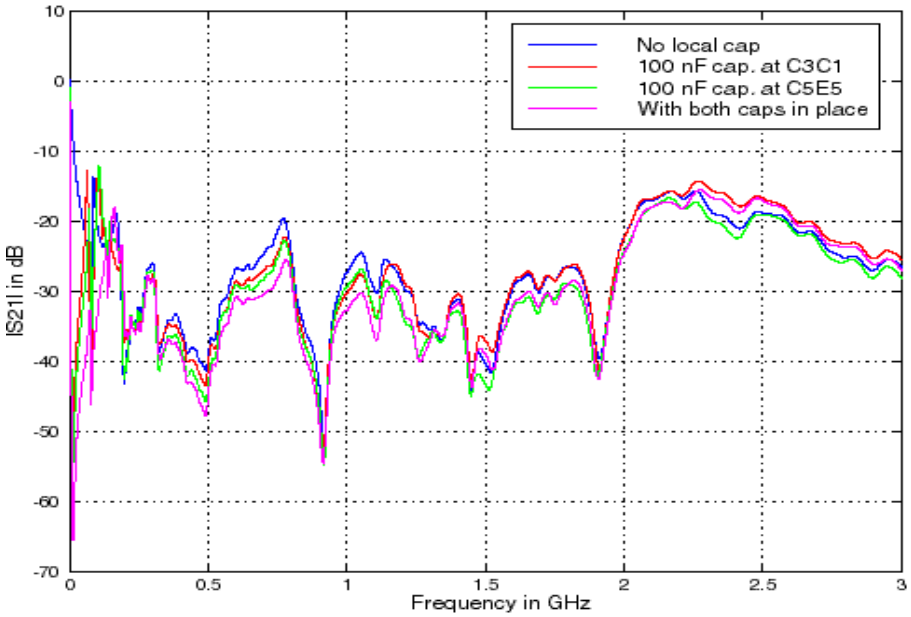

Figure 4.5. Effect of Decoupling Capacitors Close to Ports on Region 1

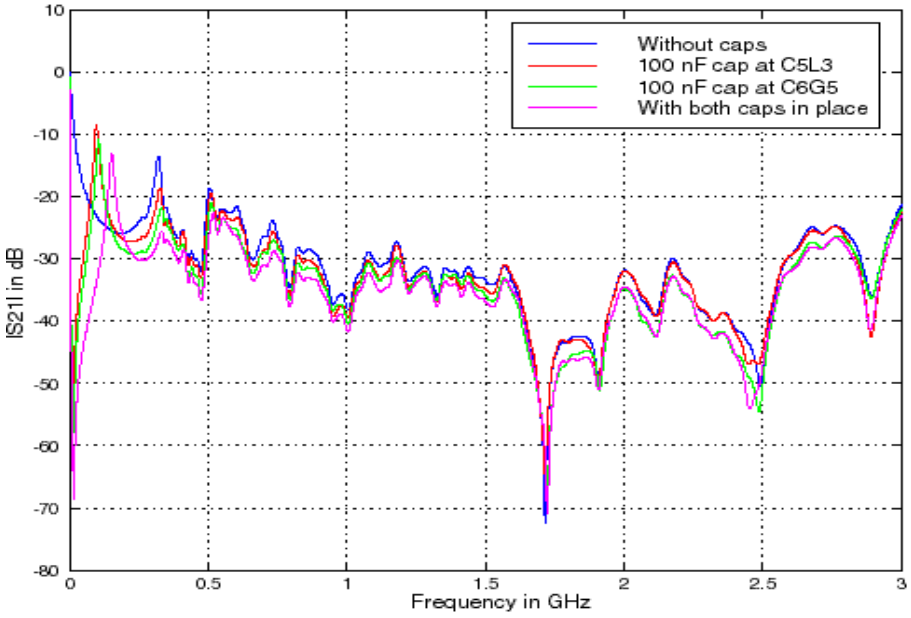

Figure 4.6. Effect of Decoupling Capacitors Close to Ports on Region 2

Figure 4.7 and Figure 4.8 compares the effect of decoupling capacitors on solid plane or on gapped plane. For Figure 4.7, the two ports were located at C6G3 and C5L2 on Region 2. Two 100 nF capacitors were attached at location C6G5 near Port 1 and C5L3 near Port 2. For Figure 4.8, the two ports were located at C6G3 on Region 2 and C3C2 on Region 1, respectively. Two 100 nF capacitors were attached at positions C6G5 near Port 1 and C3C1 near Port 2.

Figure 4.9, Figure 4.10, and Figure 4.11 show the effect of decoupling capacitors when the ports were on different planes. For Figure 4.9, the ports were located at C5L2 and C3C2 and far from each other. A 1 μF capacitor was then mounted at C3C1 (see the red curve). Next, a 100 uF bulk decoupling capacitor was attached at C2D5 (see the green curve). For Figure 4.10, the ports were located at C5L2 and C8L1. A 100 nF capacitor was attached at C5L3. For Figure 4.11, the ports were located at C5L2 and C4L3, which were on opposite sides of the gap and in close proximity. The 100 nF capacitors were mounted at C5L3 and C4M1.

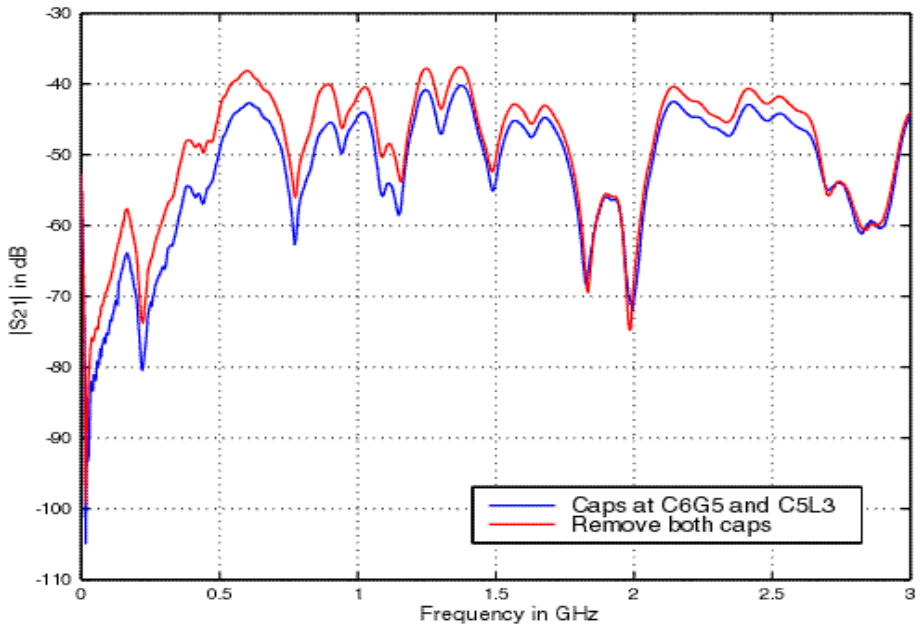

Figure 4.7. Effect of Decoupling Capacitor on the Same Power Plane

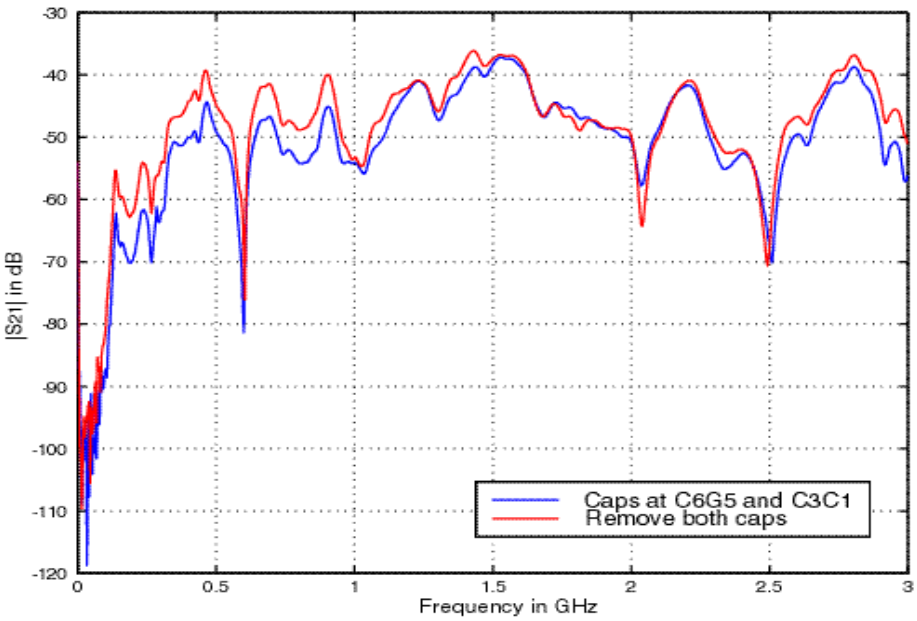

Figure 4.8. Effect of Decoupling Capacitor on Different Power Planes

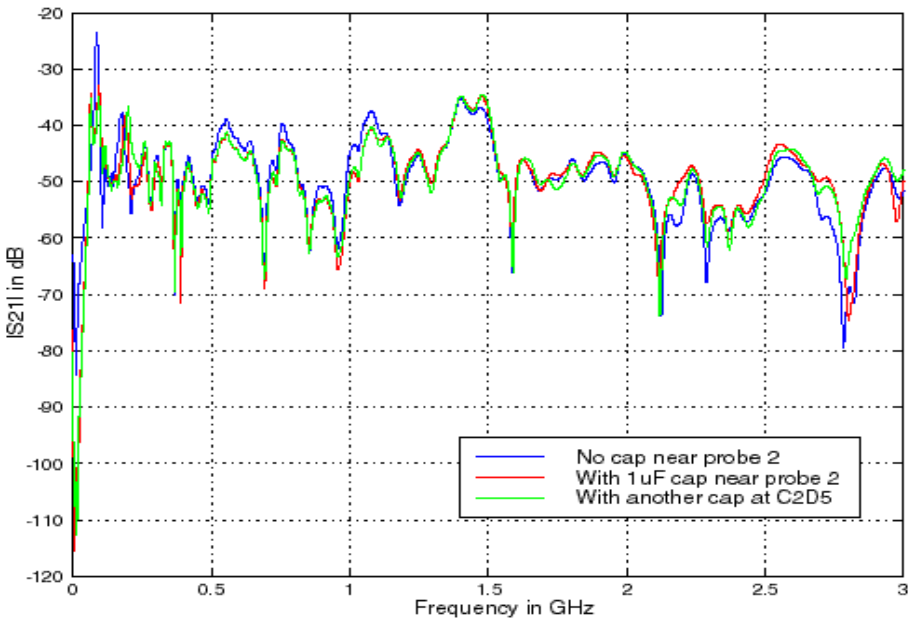

Figure 4.9. Effect of Decoupling Capacitors with Distant Ports on Different Regions

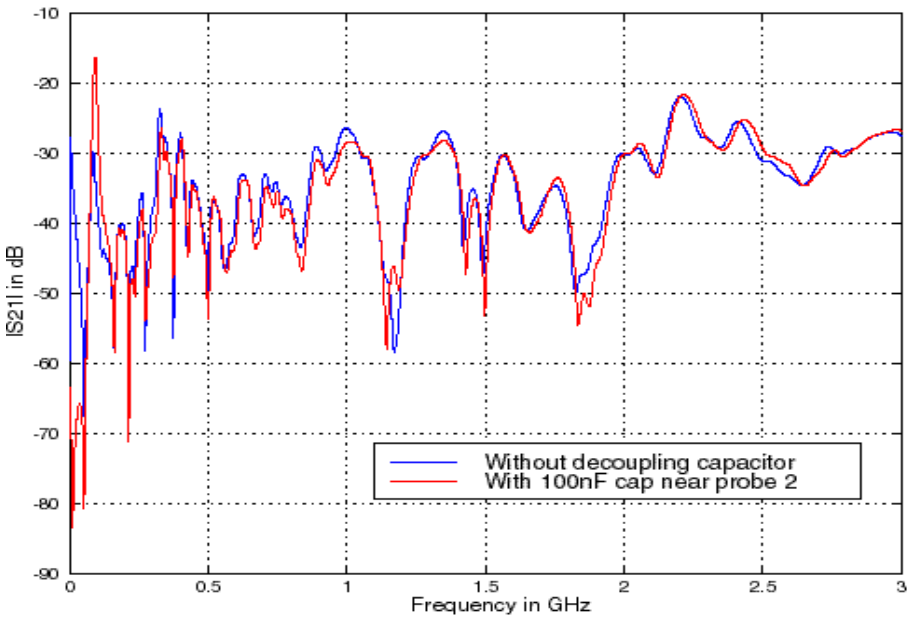

Figure 4.10. Effect of Decoupling Capacitors With Medium Distance Ports on Different Regions

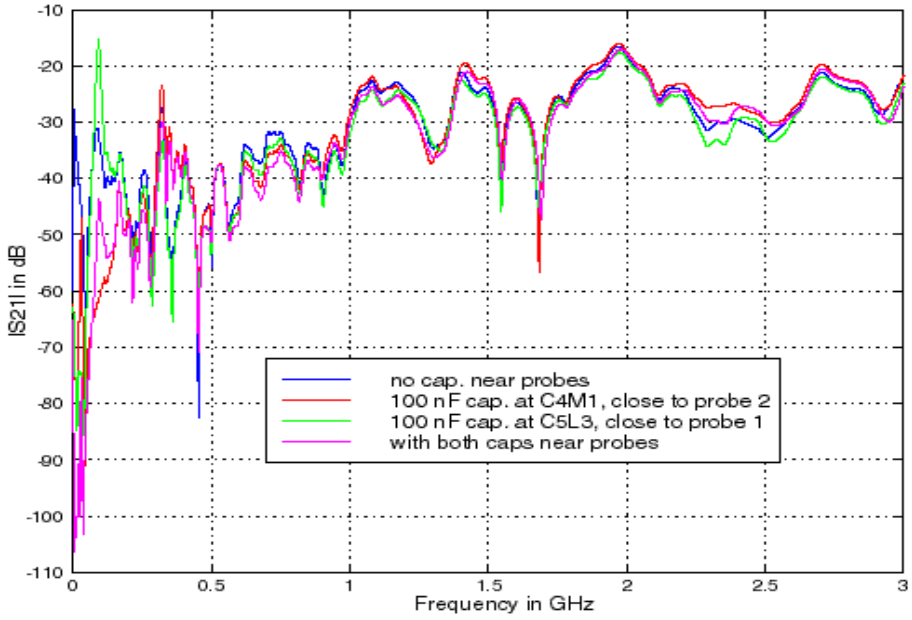

Figure 4.11. Effect of Decoupling Capacitor With Close Ports on Different Regions

Figure 4.12 shows the power bus decoupling when the decoupling capacitor shares the Vcc or the ground pad on which Port 1 was mounted. Ports were mounted at C5L2 and C6G3. For the blue curve, the 100nF decoupling capacitor was soldered between the power pad of C5L2 and return pad of C5L3. Port 1 and the decoupling capacitor share the same connection to the power plane as illustrated by Figure 4.13. Then, the capacitor was removed and re-soldered between the ground pad of C5L2 and the power pad of C5L3 and the board was measured again. Port 1 and the decoupling capacitor share the same connection to the return plane as shown in

Figure 4.14.

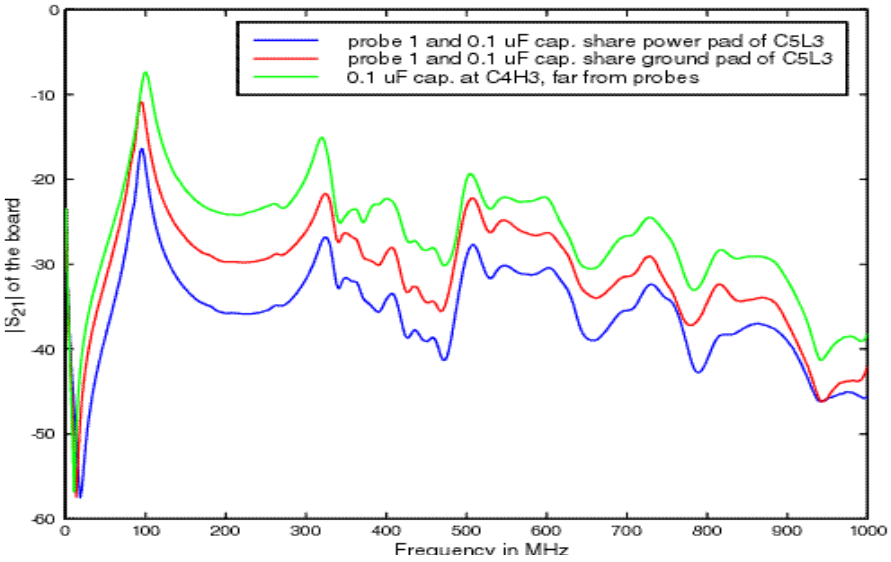

Figure 4.12. $|S_{21}|$ With Capacitor Sharing One Pad With Port 1

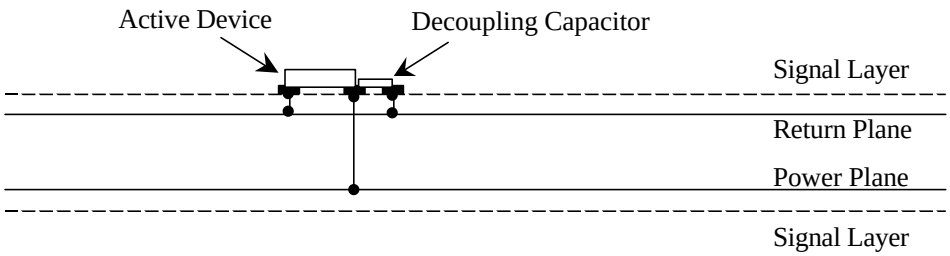

Figure 4.13. Active Device and Decoupling Capacitor Share the Same Power Pad

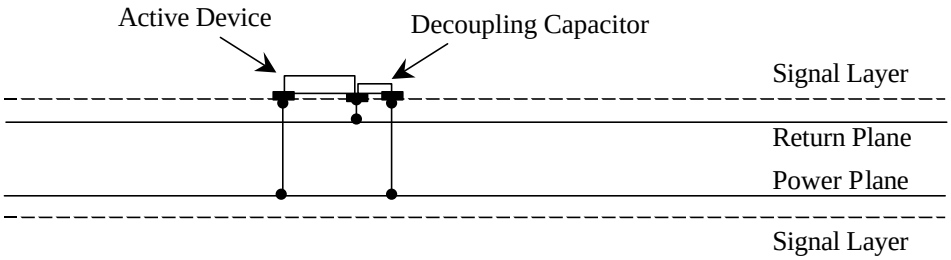

Figure 4.14. Active Device and Decoupling Capacitor Share the Same Ground Pad

Figure 4.15 corresponds to a similar experiment for the shared connections by the probe and the capacitor. The ports were located at C6G6 and C6M1. For the blue curve, the capacitor was connected between the power pad of C6G6 and the ground pad of C6G5. For the red curve, the capacitor was connected between the ground pad of C6G6 and the power pad of C6G5.

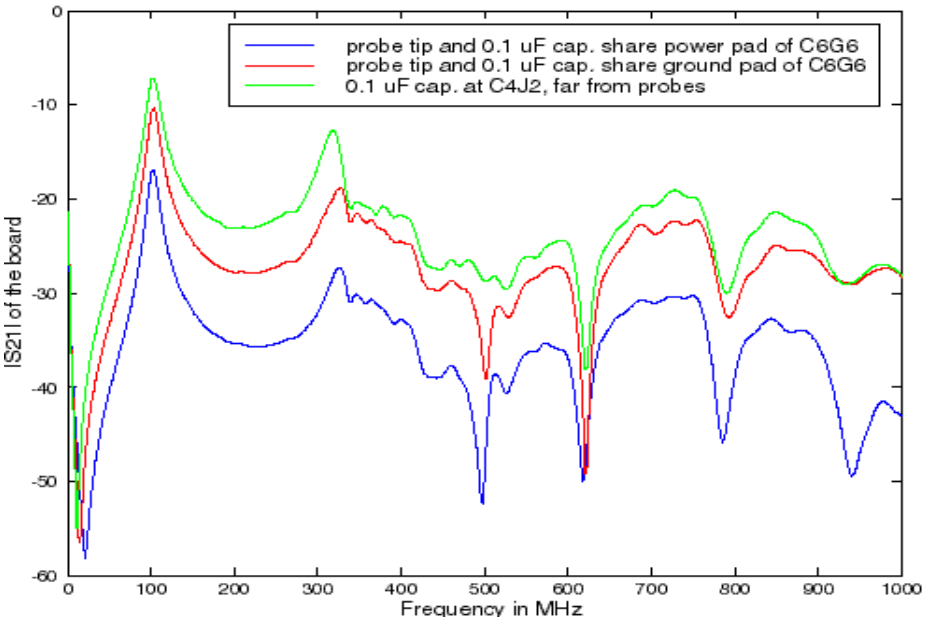

Figure 4.15. $|S_{21}|$ With Capacitor Sharing One Pad With Port 1

5. Decoupling in Board 3

Board 3 was a 2-layer mock-up of Board 2. Figure 5.1 and Figure 5.2 show the effect of a decoupling capacitor on the solid power plane. The gap in the power plane was sealed in this case. For Figure 5.1, the ports were located at L1 and L3. A 100 nF capacitor was attached near feed in probe at L3. For Figure 5.2, the ports were located at L2 and L3. The green curve corresponds to the case when the capacitor was attached on the opposite side of the probe compared to the configuration for the red curve.

Figure 5.3 and Figure 5.4 show the effect of the same capacitor on the gapped power bus structure. The seal was removed from the board in this case.

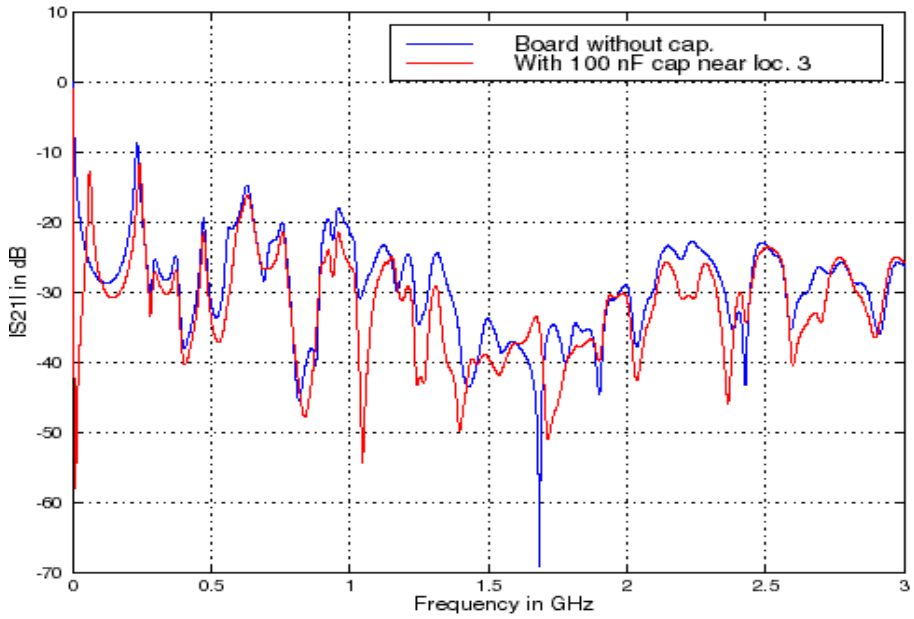

Figure 5.1. Effect of Decoupling Capacitor on Solid Plane With Ports at L1, L3

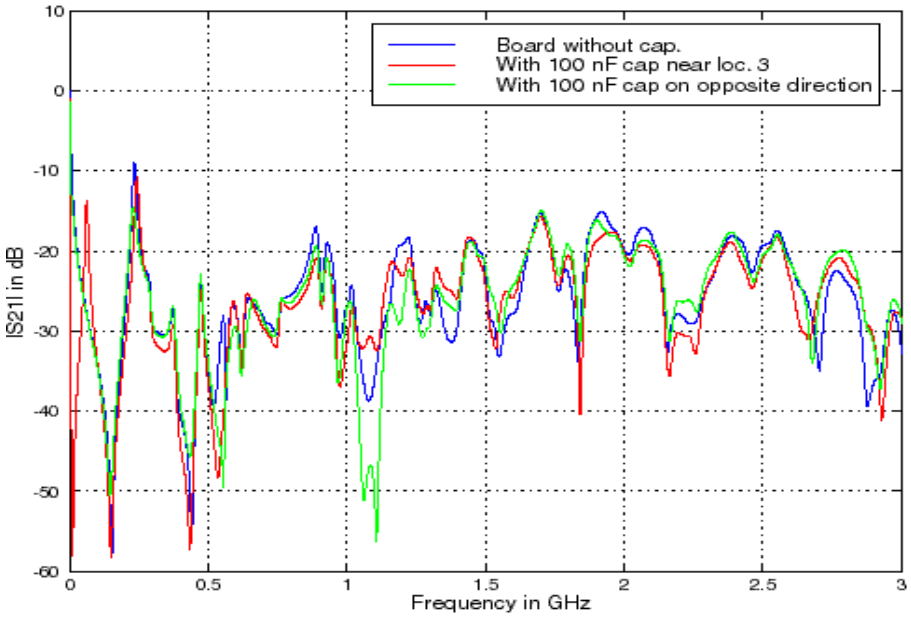

Figure 5.2. Effect of Decoupling Capacitor on Solid Plane With Ports at L2, L3

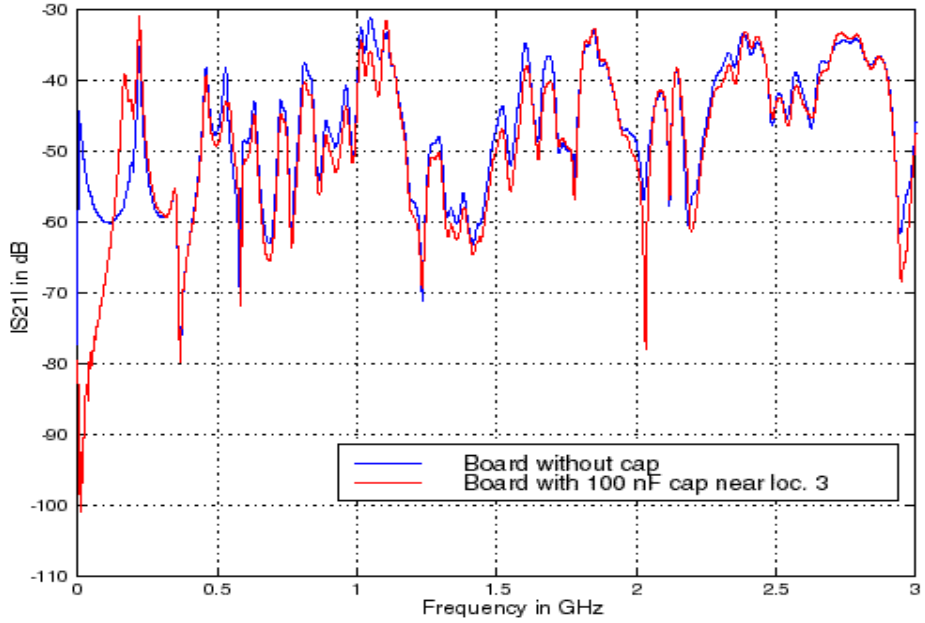

Figure 5.3. Effect of Decoupling Capacitor on Gapped Plane With Ports at L1, L3

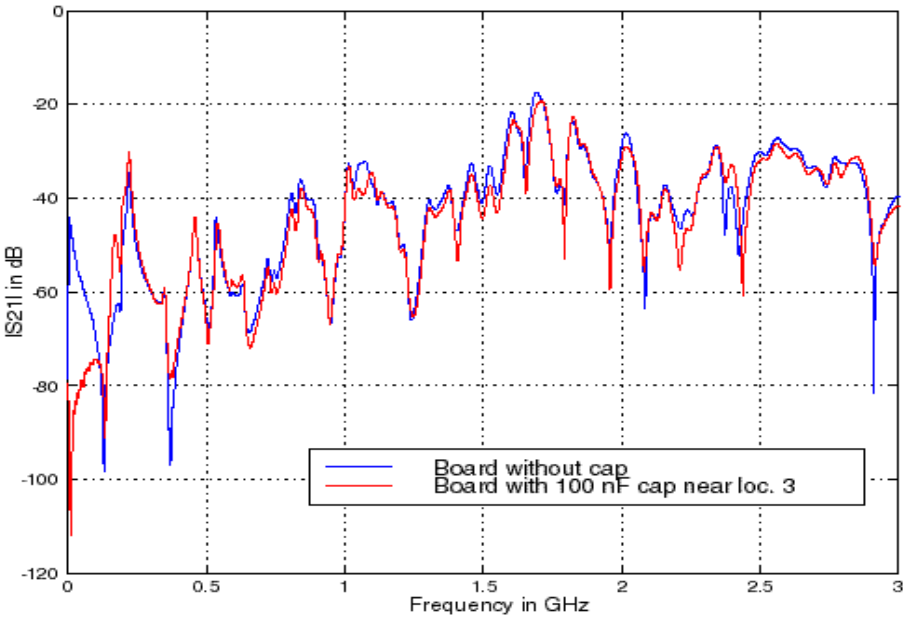

Figure 5.4. Effect of Decoupling Capacitor on Gapped Plane With Ports at L2, L3

APPENDIX

Test Procedure for Measuring S Parameters Using HP8753D Network Analyzer

The test procedure for measuring the input impedance of the power bus structures is described below. The words in **bold** face indicate a button on the front panel, the words in *italics* indicate a submenu on the display screen.

1. Turn on the network analyzer, warm up 45 minutes.

2. Connect two precision cables to Ports 1 and 2.

3. Set up measurements: (This step must be done before calibration, since the settings cannot be changed after calibration.)

a). Set frequency range: Press **START**, then press **1**+**M/u** to set the start frequency to 1 MHz. Press **STOP** and **3**+**G/n** to set the stop frequency to 3 GHz.

b). Set the number of sampling points: Press **MENU**, select *NUMBER OF POINTS* in the submenu, then use the up arrow button below the knob to increase this number to 1601 points.

c). Reduce the IF bandwidth to get a stable curve: Press **AVG**, select *IF BW* in the submenu, then use the down arrow button below the knob to decrease the bandwidth to 1000 Hz.

4. Calibration:

a). Change the model of calibration kit: Press **CAL**, then press *CAL KIT[7mm]* in the submenu, select *3.5mmD* as the model of the calibration kit. ("7mm" is the default model.) Press *RETURN*.

b). Set calibration type: Press *CALIBRATE MENU*, then select *FULL 2-PORT* submenu, since S_{11}, S_{22}, and S_{21} will all be measured.

c). Calibrate: Press *REFLECTION*, connect the open termination to Port 1 and press *OPEN* in the *FORWARD* panel in the display. Do the same with the short and matched load terminations to Port 1. Disconnect the standards from Port 1 and connect it to Port 2. Do the same to calibrate Port 2. After calibration, press *STANDARDS DONE*.

Use an f-f connector to connect the two cables to form a through connection. Press *TRANSMISSION*, then press all its submenus in turn.

Press *ISOLATION*, then *OMIT ISOLATION*, then *ISOLATION DONE*.

Complete calibration: press *DONE 2-PORT CAL*. A "Cor" sign will appear at the left side of the screen.

d). Save the calibration: Press **SAVE/RECALL**, choose the first submenu *SAVE STATE* to save the settings and calibrations to the internal memory of the network analyzer.

5. Port extension:

a). Extend Port 1: Press **MEAS**, select *Refl: FWD S11 (A/R)*. Press **FORMAT**, then select *SMITH CHART*. Connect to Port 1 an open or short probe that has the same length as the probe used in DUT. Press **CAL**, select *MORE* in the submenu, then select *PORT EXTENSIONS*. Next, press *EXTENSIONS* submenu on the top to turn the extension on, then press *EXTENSION PORT 1.* Use the knob to increase the delay until the line in the Smith chart turn into a dot in the open or short position. Press *RETURN*, a "Del" sign will appear in the left side of the screen.

b). Extend Port 2: Press **MEAS**, select *Refl: REV S22 (B/R)*. Press **FORMAT**, then select *SMITH CHART*. Connect to Port 2 the same probe, press **CAL**, select *MORE* in the submenu, then select *PORT EXTENSIONS*. Next, press *EXTENSION PORT 2*. Use the knob to adjust the delay as before.

6. Display the results:

a). Remove the probe from the cable, connect the test board.

b). Press **FORMAT**, select *LOG MAG*. Press **MEASURE**, select *Refl: FWD S11 (A/R)* to measure $|S_{11}|$, or select *Trans: FWD S21(B/R)* to measure $|S_{21}|$, or select *Refl: REV S22(B/R)* to measure $|S_{22}|$.

c). Press **SCALE REF** then *AUTO SCALE* to get a good display.

d). Use LabVIEW® to record data.

For more information on how to use the HP8753D network analyzer, refer to the user's guide [1].

REFERENCES

[1] *HP 8753D Network Analyzer User's Guide*, Hewlett Packard, HP Part No. 08753-90257, September, 1995.