UNIVERSITY OF MISSOURI-ROLLA
ELECTROMAGNETIC COMPATIBILITY LABORATORY

Title: **Experimental Results for Power Bus Noise Reduction Using Power Islands**

Report Number: TR99-6-027

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Date: September, 1999

ABSTRACT

This report presents experimental results for the study of power bus noise reduction using segmented power planes in printed circuit boards. The test boards, test setup and test procedure are described in detail. All experimental results (plots) are included without drawing general conclusions.

TABLE OF CONTENTS

Page

ABSTRACT ... ii

LIST OF ILLUSTRATIONS ... iv

SECTIONS

1. TEST BOARDS ... 1
2. EXPERIMENTAL SETUP ... 4
3. ISOLATION WITH VARIOUS GAP WIDTHS ... 5
4. POWER BUS RESONANCE ... 11
5. CONNECTIONS BRIDGING THE GAP ... 15
6. REDUNDANT RETURN PLANE ... 19
7. POWER BUS ISOLATION IN REAL CIRCUIT BOARDS ... 22
   - 7.1. Isolation in Populated Board (Board 1) ... 22
   - 7.2. Isolation in Unpopulated Board (Board 2) ... 25
   - 7.3. Isolation in Mock-Up Board (Board 3) ... 27
   - 7.4. Comparison of Isolation in Unpopulated and Populated Boards ... 32

APPENDIX ... 36

REFERENCES ... 38

LIST OF ILLUSTRATIONS

Figure Page

Figure 1.1. Layout of Boards 1 and 2 1

Figure 1.2. Mock-Up Board Layout 2

Figure 1.3. Boards 4 and 5 Layout 3

Figure 2.1. Measuring $|S_{21}|$ Using HP8753D Network Analyzer 4

Figure 3.1. $|S_{21}|$ of Board with or without Gap 5

Figure 3.2. Isolation Versus Gap Width in Board 4 6

Figure 3.3. Isolation Versus Gap Width in Board 5 7

Figure 3.4. Isolation Versus Plane Spacing for Boards 4 and 5 7

Figure 3.5. Linear Curve Fit for Board 4 9

Figure 3.6. Linear Curve Fit for Board 5 9

Figure 3.7. Logarithmic Curve Fitfor Board 4 10

Figure 3.8. Logarithmic Curve Fit for Board 5 10

Figure 4.1. S Parameters of a Symmetric Power Bus Structure 11

Figure 4.2. $|S_{21}|$ When Varying the Size of One Power Island 12

Figure 4.3. An Asymmetric Power Bus Structure 13

Figure 4.4. $|S_{21}|$ When Varying the Size of One Power Island 13

Figure 4.5. Layout of an Asymmetric Power Bus Structure 14

Figure 4.6. S Parameters of an Asymmetric Power Bus Structure 14

Figure 5.1. $|S_{21}|$ of Gapped Plane with Different Connections 15

Figure 5.2. S Parameters of Board 4 with a Copper Bridge at Location 4 16

Figure 5.3. S Parame ters of Board 4 with a Ferrite Bead Bridge at Location 4 16

Figure 5.4. $|S_{21}|$ Versus Bridge Widths 17

Figure 5.5. $|S_{21}|$ Versus Bridge Locations 18

Figure 5.6. $|S_{21}|$ Versus Ferrite Bead Locations 18

Figure 6.1. 3-Layer Board Configuration 19

Figure 6.2. Edge and Via Connections of the 3-Layer Board 19

Figure 6.3. $|S_{21}|$ with a Floating Return Plane 20

Figure 6.4. $|S_{21}|$ with Edge Sealed or Vias Connected 21
Figure 6.5. $|S_{21}|$ with Edges Sealed and Vias Connected 21
Figure 7.1. Port Locations Used in Experiments 22
Figure 7.2. Effect of Gap in Populated Board with Distant Ports 23
Figure 7.3. Effect of Gap in Populated Board with Close Ports 23
Figure 7.4. S Parameters of Populated Board with Distant Ports 24
Figure 7.5. S Parameters of Populated Board with Close Ports 24
Figure 7.6. S Parameters of Populated Board with Medium Distance Ports 25
Figure 7.7. S Parameters of Unpopulated Board with Distant Ports 26
Figure 7.8. S Parameters of Unpopulated Board with Close Ports 26
Figure 7.9. S Parameters of Unpopulated Board with Medium Distance Ports 27
Figure 7.10. Effect of Gap in Mock-Up Board with Ports at L1 and L3 28
Figure 7.11. Effect of Gap in Mock-Up Board with Ports at L2 and L3 28
Figure 7.12. S Parameters of Gapped Board 3 with Ports at L1 and L3 29
Figure 7.13. S Parameters of Gapped Board 3 with Ports at L2 and L3 29
Figure 7.14. S Parameters of Solid Board 3 with Ports at L2 and L3 30
Figure 7.15. Board Isolation with a Copper Bridge at Location 3 30
Figure 7.16. Board Isolation with a Ferrite Bead at Location 1 31
Figure 7.17. Board Isolation with One or Two Ferrite Beads at Locations 1, 3 31
Figure 7.18. Isolation of Unpopulated and Populated Boards with Distant Ports 32
Figure 7.19. Isolation of Unpopulated and Populated Boards with Close Ports 33
Figure 7.20. Isolation of Unpopulated and Populated Boards with Moderately-Spaced Ports 33
Figure 7.21. Effect of IC Component on Isolation 34
Figure 7.22. Effect of IC Component on Isolation 35

1. Test Boards

Five test boards were employed in this study. Board 1 was a 4-layer personal computer motherboard provided by a chip manufacturer. It was fully populated with a large number of components. Figure 1.1 shows the geometry of this board. The power plane was divided into two power islands, Region1 and Region 2. On Region 1, 7 bulk decoupling capacitors and 29 local decoupling capacitors connected to the power and return planes were identified. On Region 2, 4 bulk decoupling capacitors and 24 local decoupling capacitors were identified. The values of the bulk decoupling capacitors were 100 µF, 22 µF, or 10 µF. The values of the local decoupling capacitors were 1 µF or 0.47 µF. The measured inter-plane capacitance of the power bus was 1.4 nF in Region 1 and 1.2 nF in Region 2. The bonding pads of the decoupling capacitors used in the experiments are also labeled in Figure 1.1.

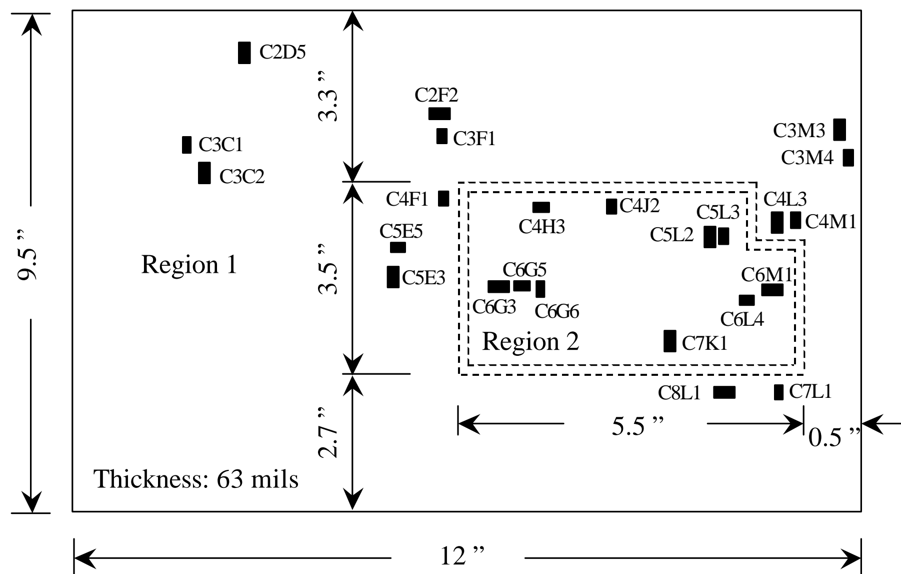


Figure 1.1. Layout of Boards 1 and 2

Board 2 was an unpopulated version of Board 1.

Board 3 was a mock-up of Board 2. As shown in Figure 1.2, the 2-layer mock up board has the same width and length as Board 2. The shapes of the power islands are also similar, but the spacing between the power and return layers is about 50 mils instead of 40 mils for the motherboard. There is a 100-mil gap between Region 1 and Region 2. Three short 85-mil diameter semi-rigid probes were attached between power and return planes at locations L1, L2, and L3 to make the S-parameter measurements.

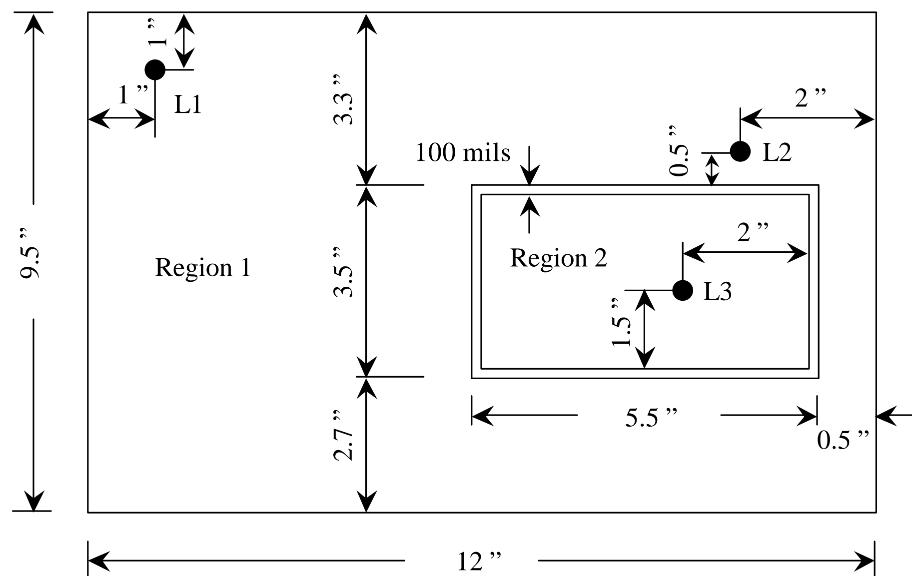


Figure 1.2. Mock-Up Board Layout

Boards 4 and 5 shown in Figure 1.3 were built to evaluate the effectiveness of power bus segmentation. They were 6 inches long and 4 inches wide. The board thickness was 63 mils for Board 4 and 95 mils for Board 5. The boards had two copper planes separated by FR-4 material. A gap was cut in the middle of the power plane. Two low impedance 85-mil diameter semi-rigid probes were attached to the center of the power islands to make measurements.

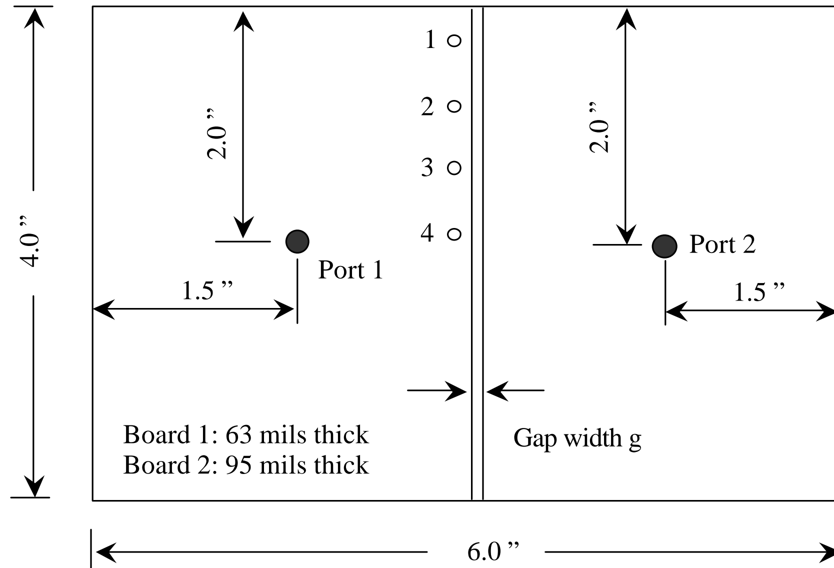


Figure 1.3. Boards 4 and 5 Layout

2. Experimental Setup

An HP8753D network analyzer was used to measure S parameters of the test board. The $|S_{11}|$ ($|S_{22}|$) parameter is the ratio of reflected signal to the incident signal at Port 1 (Port 2). The $|S_{21}|$ parameter is the ratio of transmitted signal at Port 2 to the incident signal at Port 1. Figure 2.1 shows an S-parameter measurement being made using the network analyzer. The procedure of S-parameter measurement is described in detail in the appendix.

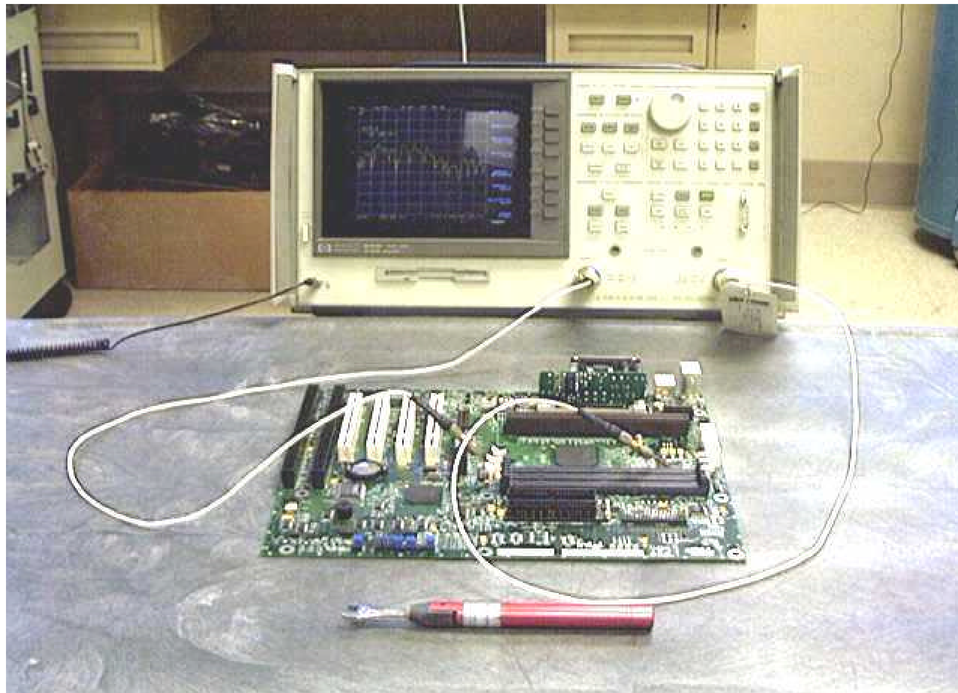


Figure 2.1. Measuring $|S_{21}|$ Using HP8753D Network Analyzer

3. Isolation with Various Gap Widths

Figure 3.1 shows how efficiently a gap isolates the two power islands compared to a solid power plane. The two ports were connected to the two probes on Board 4.

Figure 3.2 compares the measured $|S_{21}|$ for Board 4 with different gap widths.

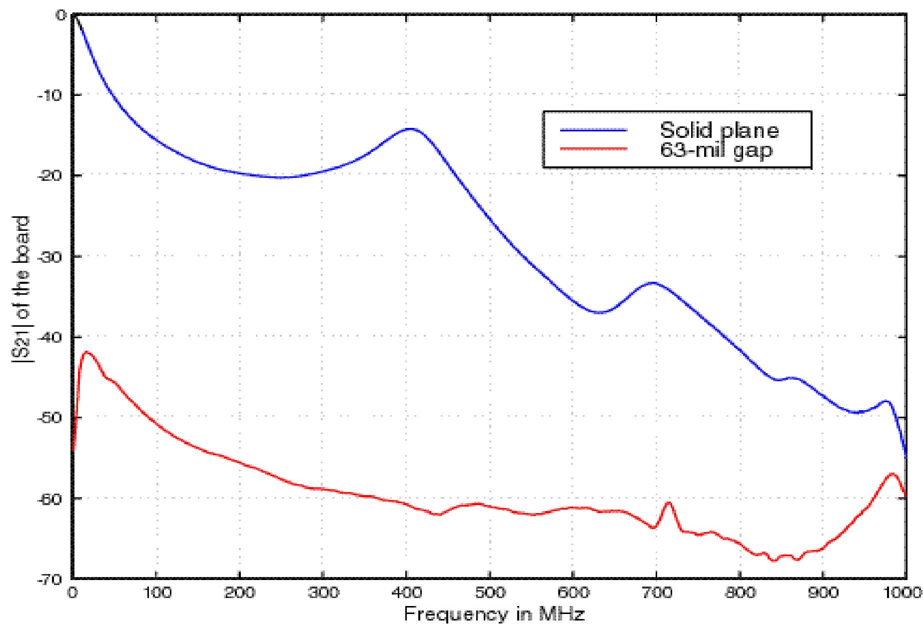


Figure 3.1. $|S_{21}|$ of Board with or without Gap

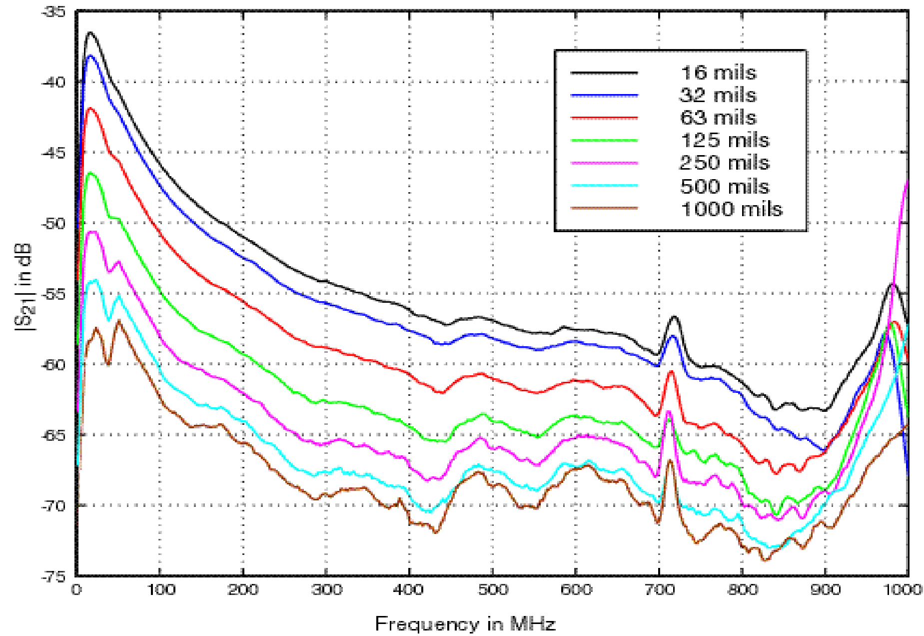


Figure 3.2. Isolation versus Gap Width in Board 4

Figure 3.3 shows similar experiment on Board 5. The board thickness was 95 mils. Figure 3.4 compares the measured $|S_{21}|$ for Boards 4 and 5 with the same gap width. It is apparent that a thinner board provides better isolation.

As Figures 1.2 and 1.3 illustrate, the measured $|S_{21}|$ have different levels, but the curves have a similar shape. The $|S_{21}|$ increases as the gap width decreases and as the board thickness increases. This indicates that $|S_{21}|$ may be a function of the ratio of gap width to plane spacing. Curve fitting method was used to investigate the relationship between $|S_{21}|$ and this ratio. The $|S_{21}|$ values in dB were converted to simple transfer ratio in order to obtain a linear plot.

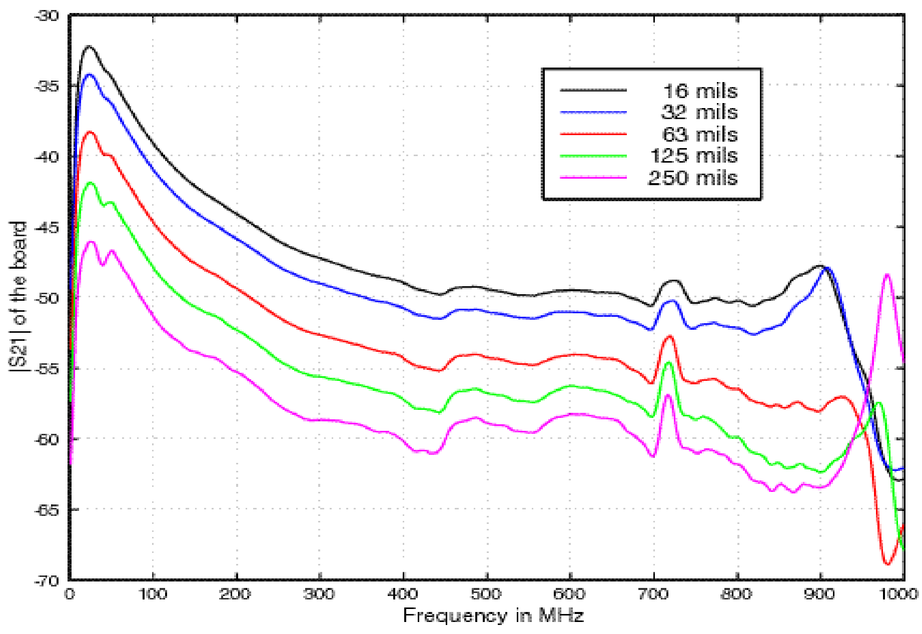


Figure 3.3. Isolation versus Gap Width in Board 5

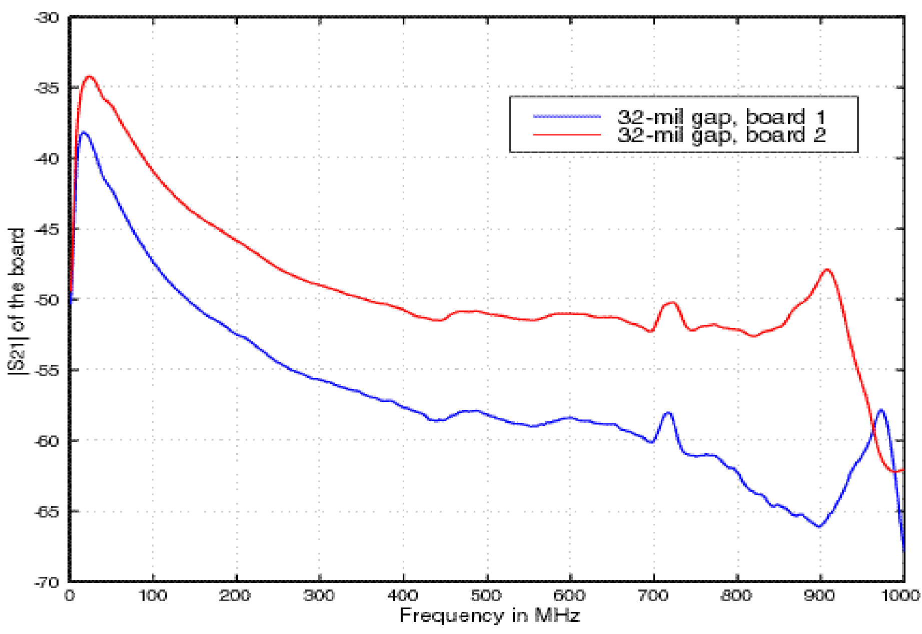


Figure 3.4. Isolation versus Plane Spacing for Boards 4 and 5

Figure 3.5 plots the measured $|S_{21}|$ as a function of gap width/plane spacing for Board 1. The plane spacing for Board 4 is 63 mils. The red dots correspond to the measured $|S_{21}|$ values for different gap widths. The blue curve is a fitting curve given by the function,

$$|S_{21}| = 0.00055 + \frac{0.0009}{(g/t + 0.25)} \tag{1}$$

where g is the gap width and t is the plane spacing.

Similarly, Figure 3.6 plots the measured $|S_{21}|$ as a function of gap width/plane spacing for Board 5, whose plane spacing is 95 mils. Again the red dots correspond to the $|S_{21}|$ values for different gap widths. The blue curve is a fitting curve given by the function,

$$|S_{21}| = 0.00055 + \frac{0.0018}{(g/t + 0.25)} \tag{2}$$

where the parameters g and t are the same as those in Equation (2.1). Equations (2.1) and (2.2) are similar, only one constant is different due to different plane spacing.

Figure 3.7 and Figure 3.8 show the algorithmic curve fitting for Boards 4 and 5. The x-axis corresponds to ln (g/t), the y-axis corresponds to $|S_{21}|$ in dB. The equation for Board 4 is,

$$|S_{21}|_{dB} = -3.9 * \ln(g/t) - 59.2 \tag{3}$$

The equation for Board 5 is,

$$|S_{21}|_{dB} = -3.9 * \ln(g/t) - 54.4 \tag{4}$$

where g and t are gap width and plane spacing, respectively.

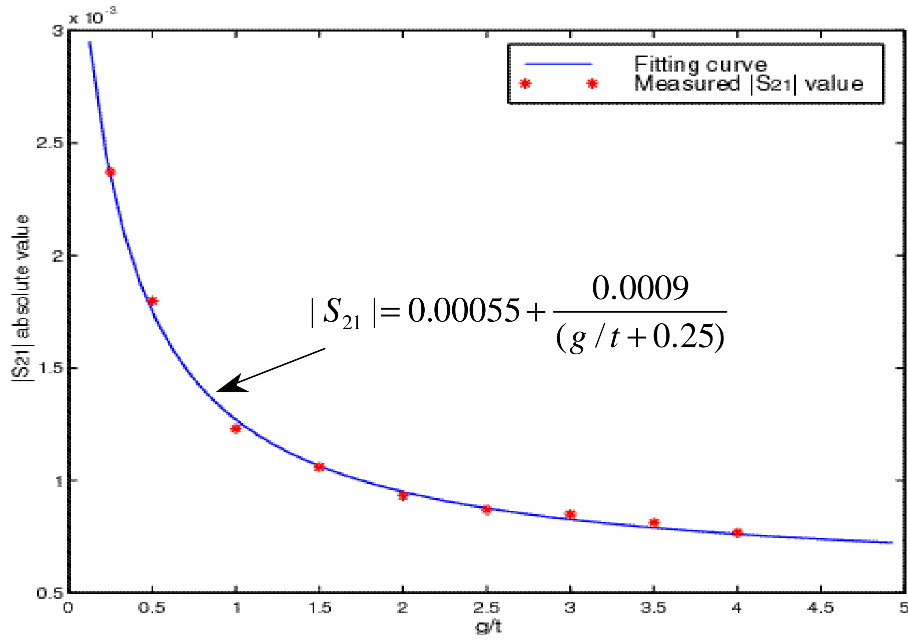


Figure 3.5. Linear Curve Fit for Board 4

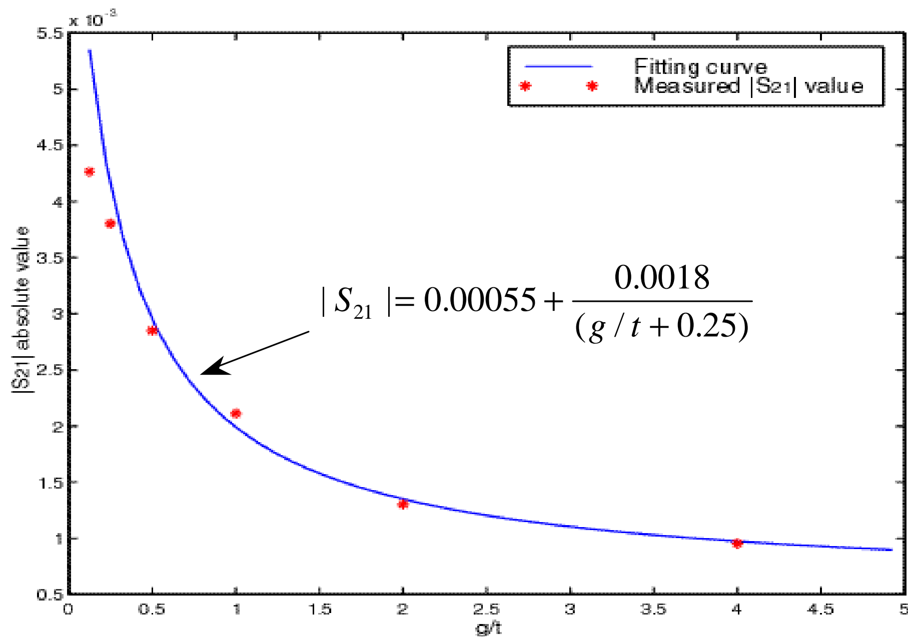


Figure 3.6. Linear Curve Fit for Board 5

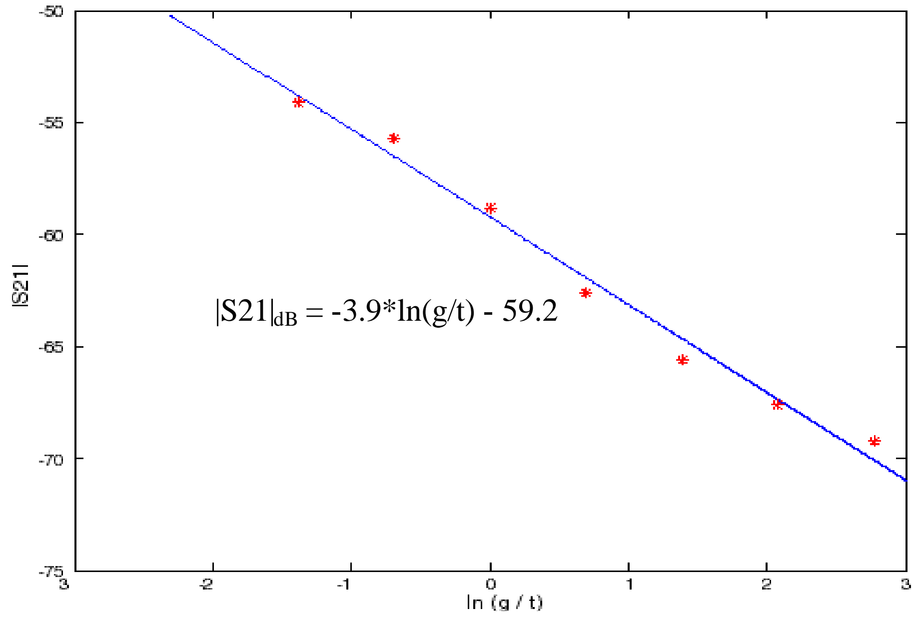


Figure 3.7. Logarithmic Curve Fit for Board 4

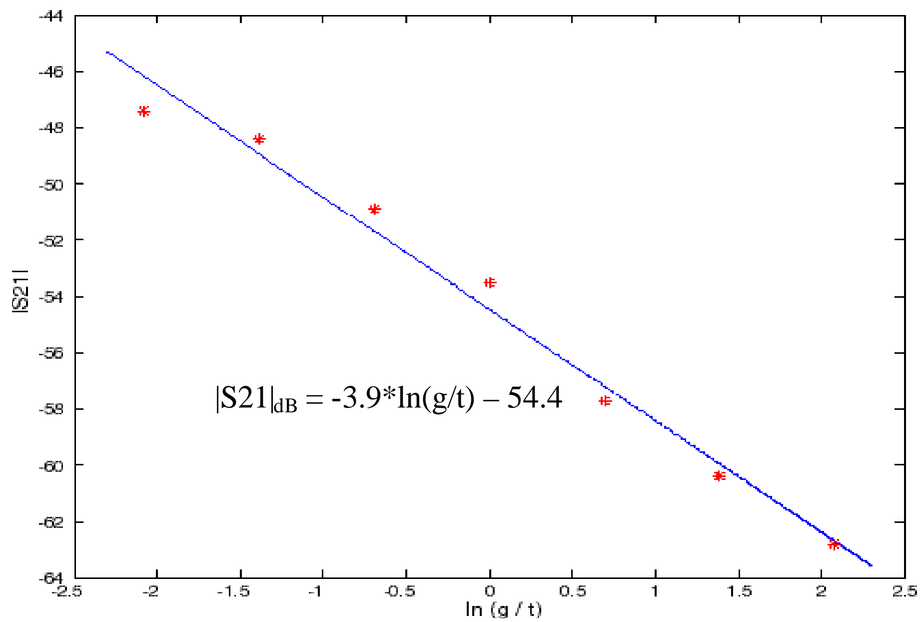


Figure 3.8. Logarithmic Curve Fit for Board 5

4. Power Bus Resonance

Figure 4.1 is a plot of measured S parameters versus frequency for the symmetric power island configuration on Board 4.

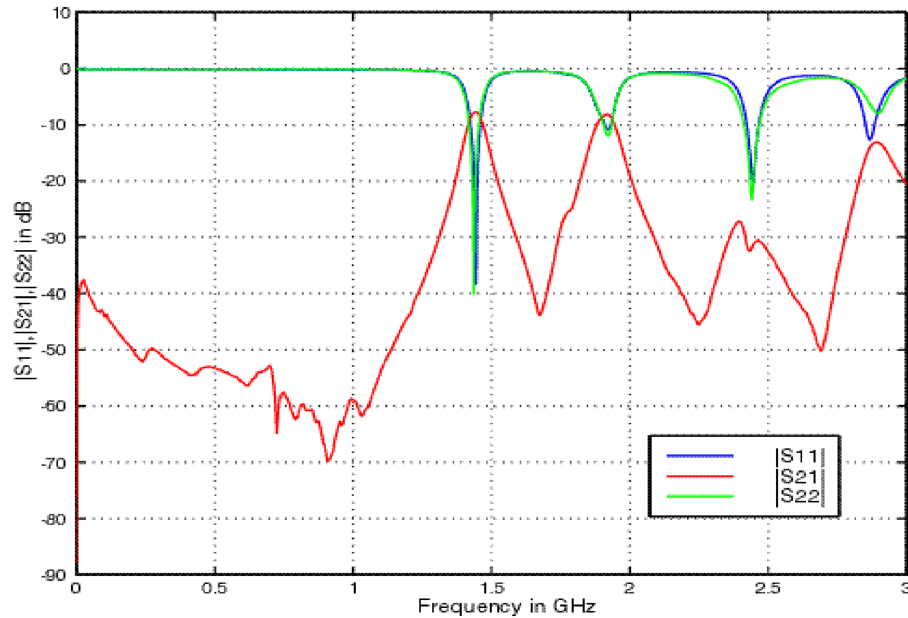


Figure 4.1. S Parameters of a Symmetric Power Bus Structure

Figure 4.2 shows the results when varying the dimensions of the driving island on Board 4. As illustrated by the green curve, reducing the width of the driving island from 4 inches to 3 inches eliminates the peak in the $|S_{21}|$ response at 1.4 GHz. Reducing the length of the driving plane from 3 inches to 2.5 inches eliminates the peak at 1.9 GHz, as shown by the red curve.

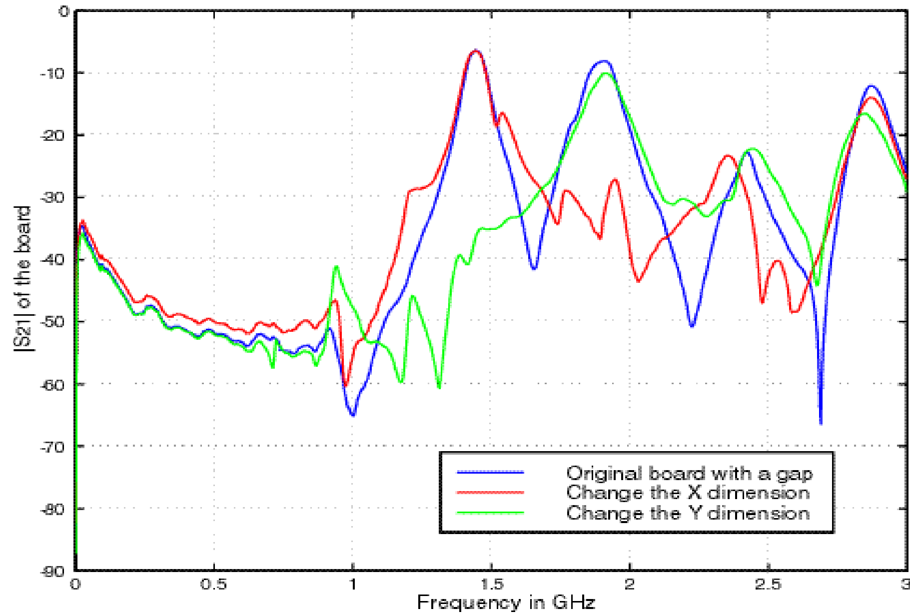


Figure 4.2. $|S_{21}|$ When Varying the Size of One Power Island

A similar experiment was made on Board 4 with asymmetric power bus structure. Figure 4.3 shows the dimensions of the power islands. Gaps were cut in the dashed line positions to reduce the dimension. Figure 4.4 shows the measured $|S_{21}|$. The red curve corresponds to the configuration when the width of one island was reduced from 2.5 inches to 1.9 inches. The green curve corresponds to the case when the length of one island was reduced from 4 inches to 3 inches.

To further illustrate the above idea, experiments were made on another asymmetric power island structure as shown in Figure 4.5. Copper on the power plane was removed to form a smaller power island while the return plane was kept intact. The measured S parameters are plotted versus frequency in Figure 4.6.

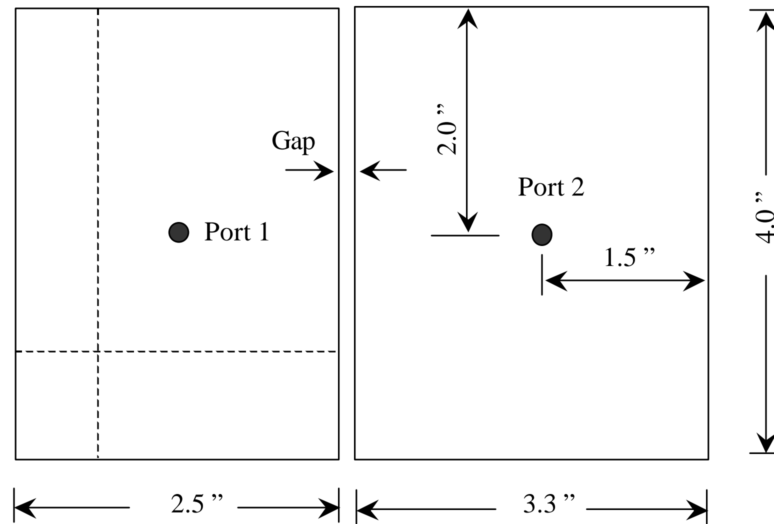


Figure 4.3. An Asymmetric Power Bus Structure

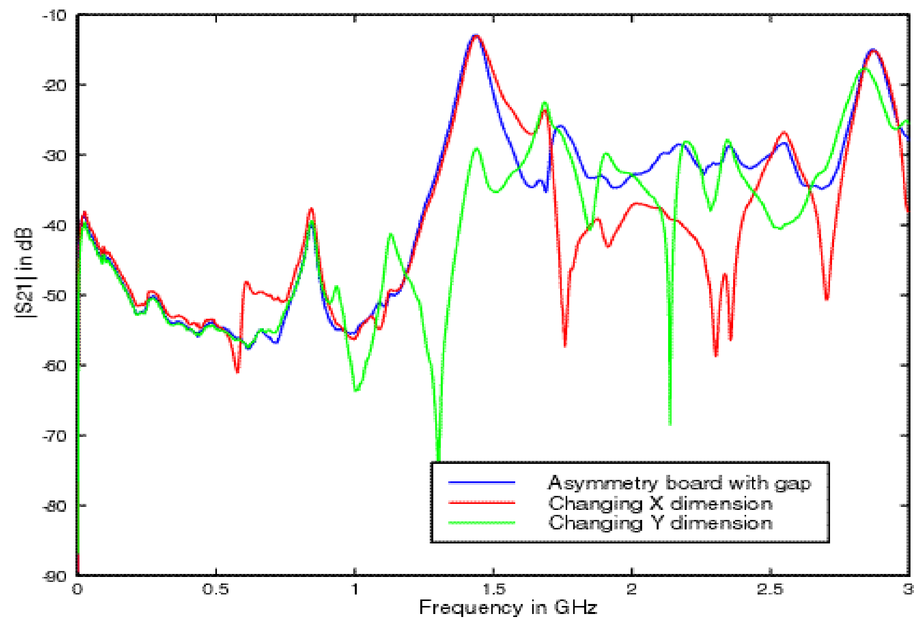


Figure 4.4. $|S_{21}|$ When Varying the Size of One Power Island

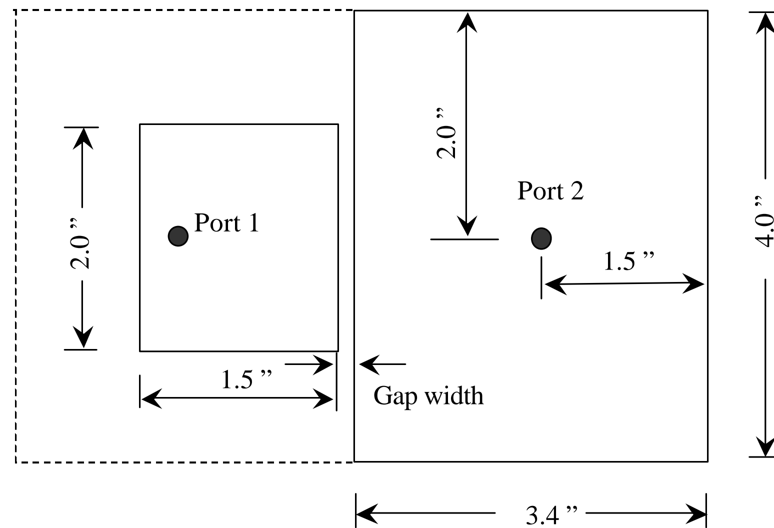


Figure 4.5. Layout of an Asymmetric Power Bus Structure

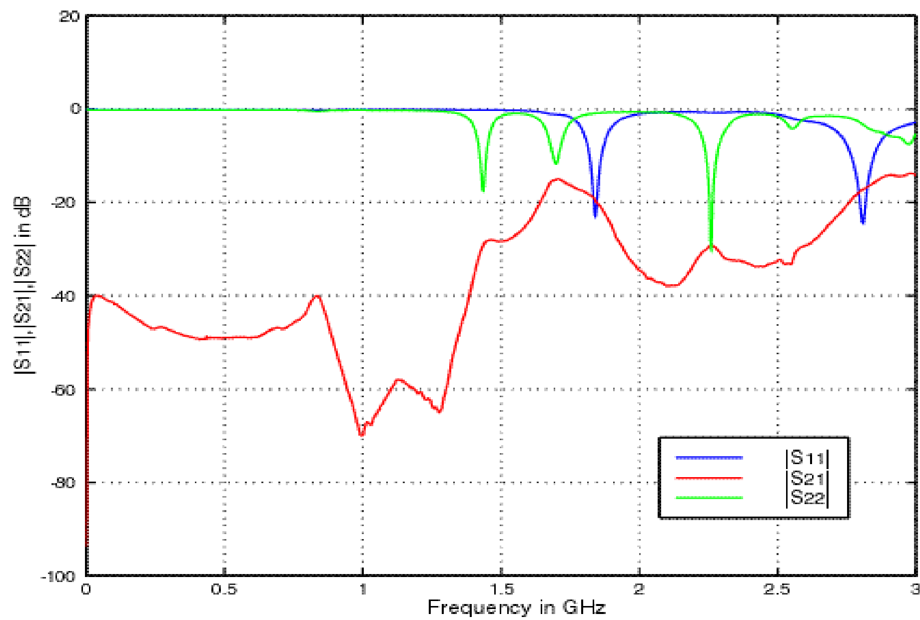


Figure 4.6. S Parameters of an Asymmetric Power Bus Structure

5. Connections Bridging the Gap

Experiments were made on Board 4 to show the effect of connections bridging the gap. A strip of copper tape was used as a conductive bridge. It was soldered to the power planes connecting it. A surface mount BLM21B471SD ferrite bead was used as a ferrite bead bridge. Its resistance was 470 ohms at 100 MHz.

Figure 5.1 compares the isolation of a gapped plane to the results obtained from a solid plane, a gapped plane with a narrow bridge over the gap and a gapped plane with a ferrite bead connecting the planes. In these measurements, a 100 nF surface mount capacitor was connected near the driving port to provide a low impedance source, which is more representative of real printed circuit board configurations.

The S parameters of Board 4 with a copper bridge or a ferrite bead bridge are shown in Figure 5.2 and Figure 5.3. The bridges were located at Location 4 (middle location) as shown in Figure 1.3.

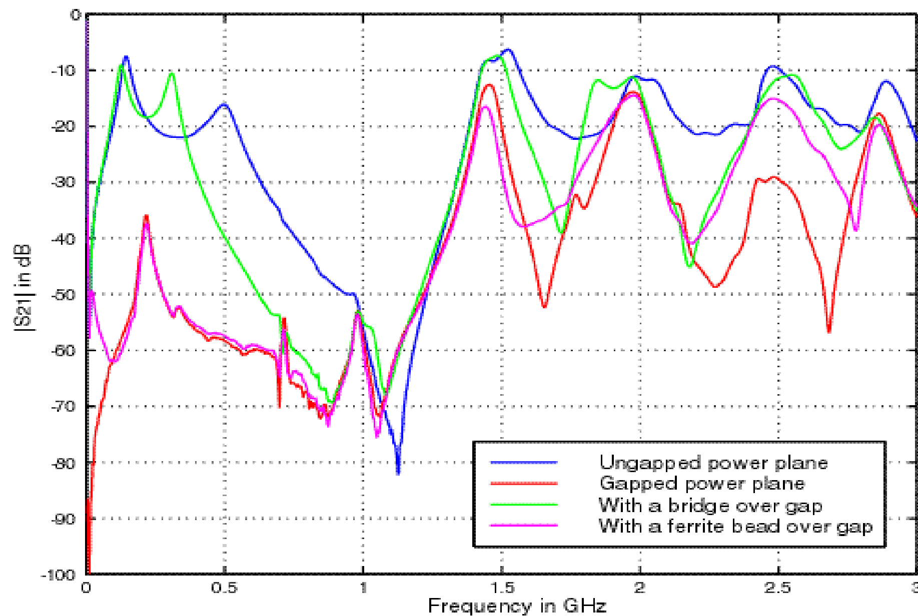


Figure 5.1. $|S_{21}|$ of Gapped Plane with Different Connections

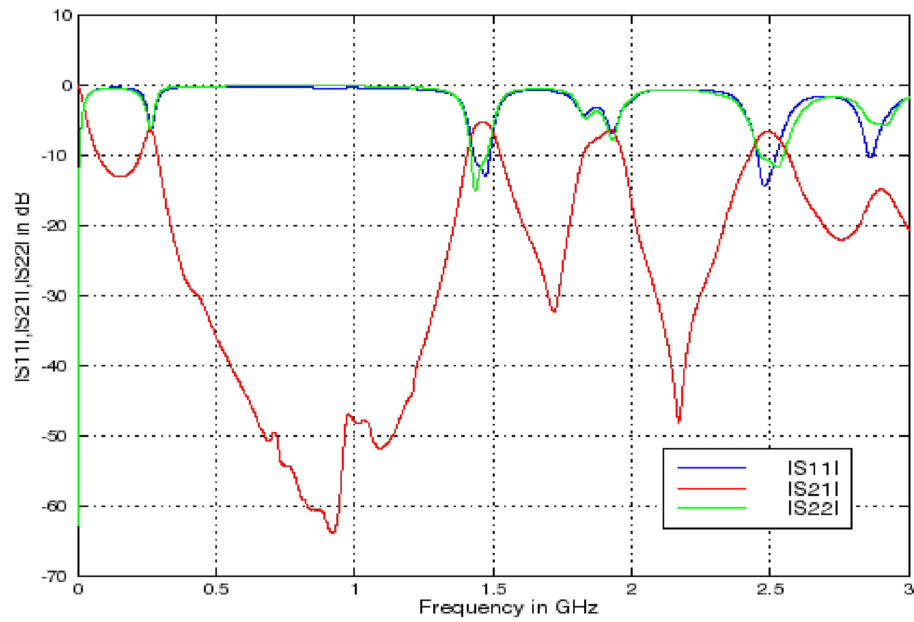


Figure 5.2. S Parameters of Board 4 with a Copper Bridge at Location 4

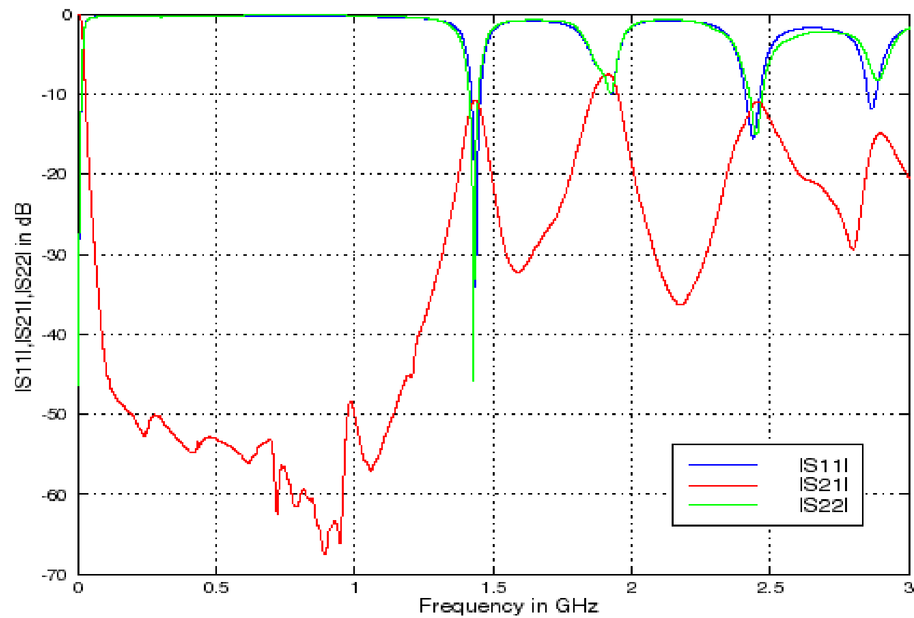


Figure 5.3. S Parameters of Board 4 with a Ferrite Bead Bridge at Location 4

Figure 5.4 illustrates the effect of bridge width on isolation. The 10-mil, 63-mil and 250-mil wide bridges were used for comparison. The bridges were located in the middle of the gap.

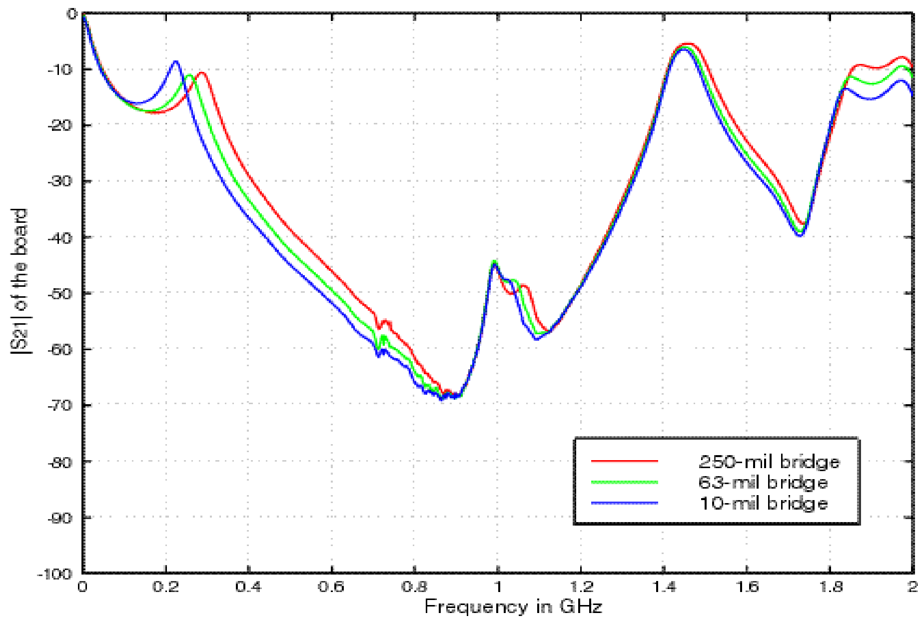


Figure 5.4. $|S_{21}|$ Versus Bridge Widths

Figure 5.5 shows the effect of bridge location on power bus isolation. The same bridge was placed at Locations 1, 2, 3 and 4 as illustrated in Figure 1.3.

Figure 5.6 is a plot of the measured $|S_{21}|$ versus the location of the ferrite bead. The ferrite bead was placed at Locations 1, 2, 3 and 4.

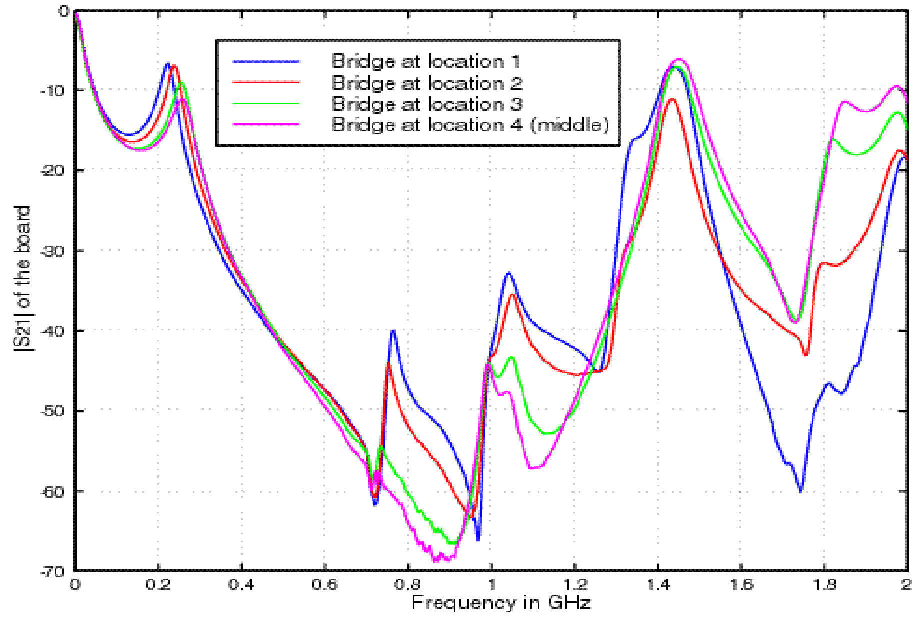


Figure 5.5. $|S_{21}|$ Versus Bridge Locations

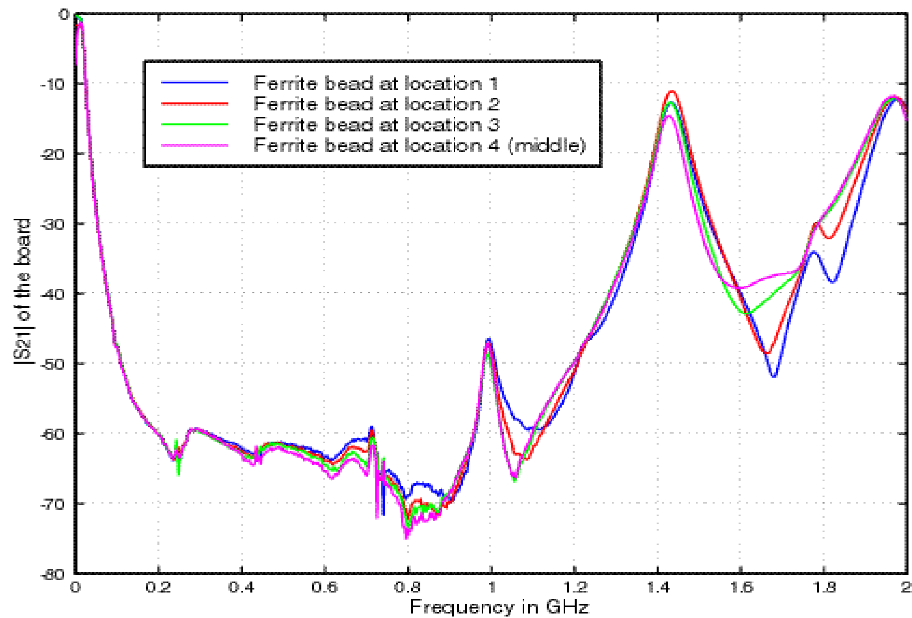


Figure 5.6. $|S_{21}|$ Versus Ferrite Bead Locations

6. Redundant Return Plane

As shown in Figure 6.1, a 63-mil 1-layer board was added to Board 4 to form a symmetric "sandwich" stack-up. The top and bottom planes were the two return planes and the middle plane was the power plane. In some experiments, the two return planes were connected by sealing their edges or by 8 vias uniformly aligned along both sides of the gap. The power plane was carefully isolated to avoid any direct connection with the two return planes. Figure 6.2 is a photo showing the edge and via connections made on Board 4.

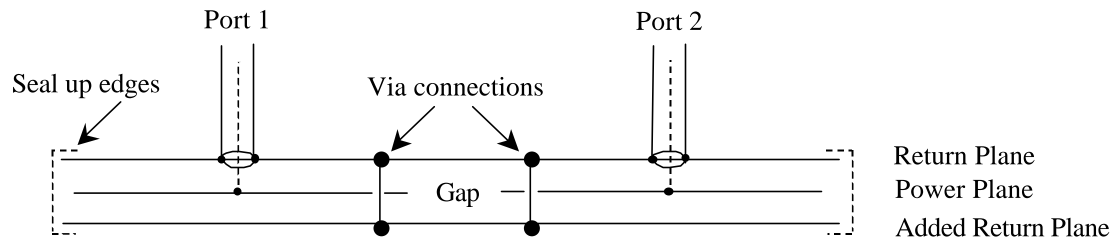


Figure 6.1. 3-Layer Board Configuration

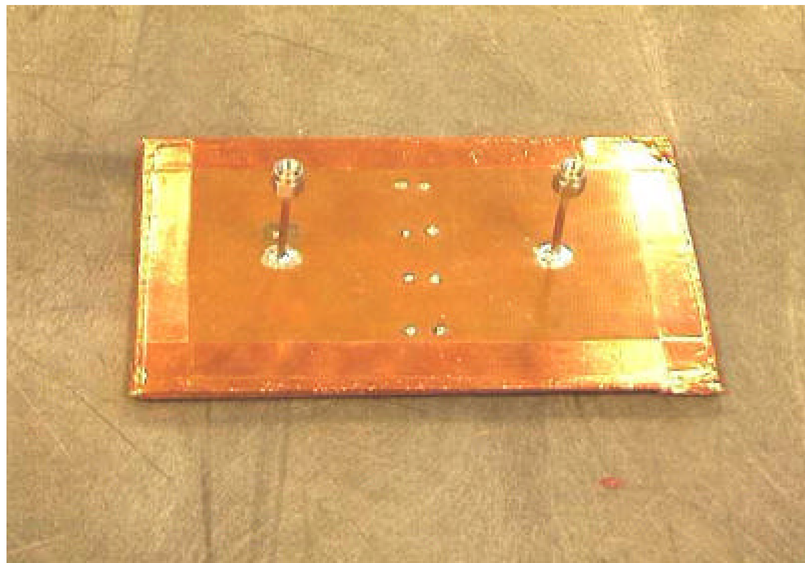


Figure 6.2. Edge and Via Connections of the 3-Layer Board

Figure 6.3 compares the measured $|S_{21}|$ for the original 2-layer board and that for the 3-layer board with a floating return plane.

Figure 6.4 shows the results when the two return planes were connected by sealing up all edges of the two return planes, or making through-hole vias connecting the two return planes. Figure 6.5 shows the measured $|S_{21}|$, the cyan curve, when the edge connections and via connections were made at the same time

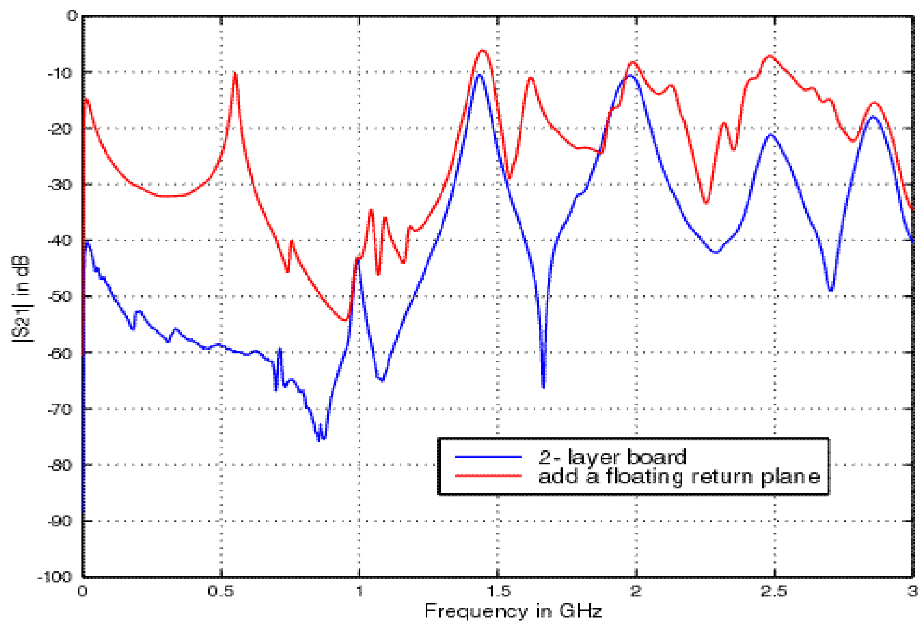


Figure 6.3. $|S_{21}|$ with a Floating Return Plane

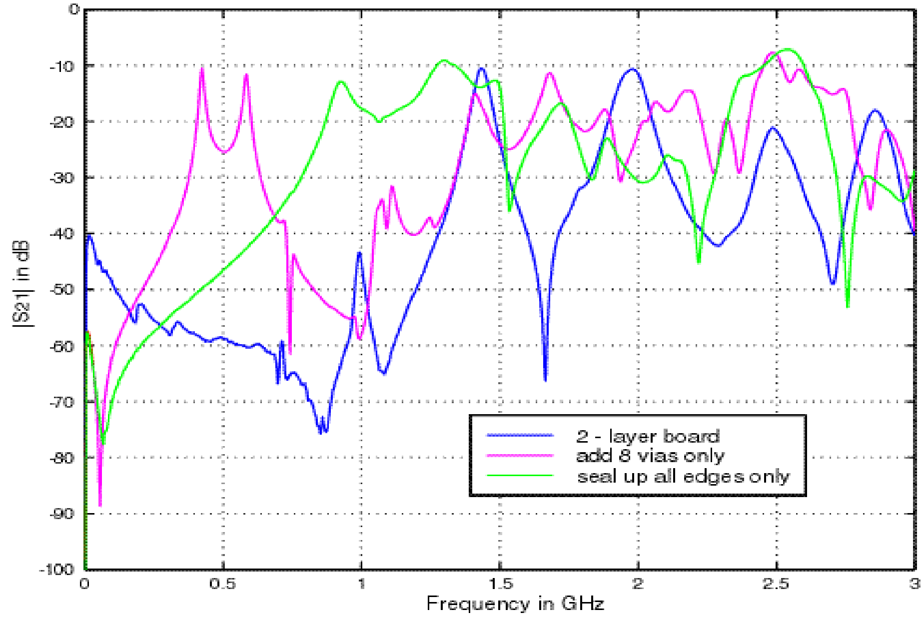


Figure 6.4. $|S_{21}|$ with Edge Sealed or Vias Connected

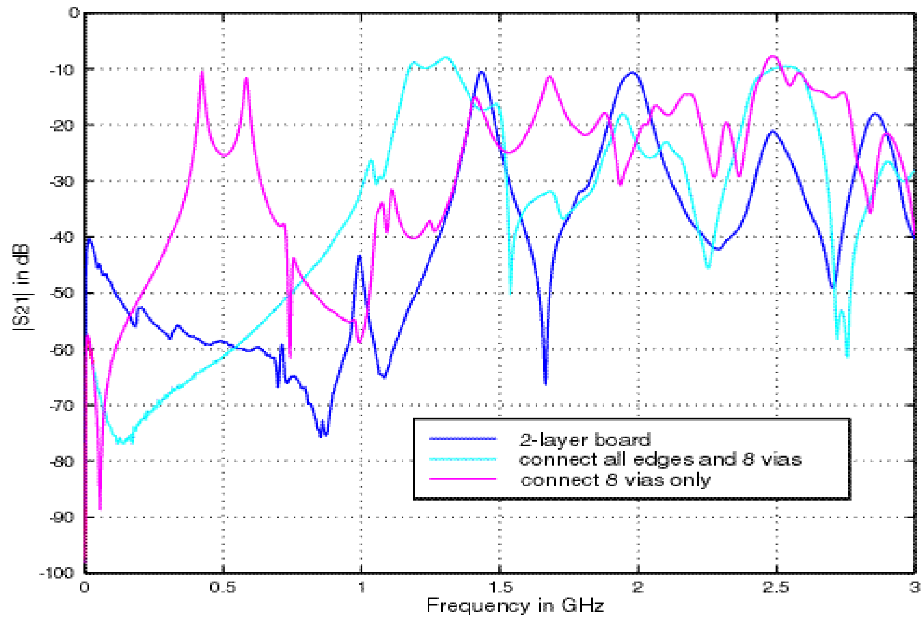


Figure 6.5. $|S_{21}|$ with Edges Sealed and Vias Connected

7. Power Bus Isolation in Real Circuit Boards

To investigate the power island isolation in real circuit boards, experiments were made on Boards 1, 2, and 3.

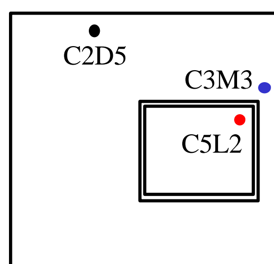
7.1. Isolation in Populated Board (Board 1)

Measurements were made in the same plane and in different planes with approximately equal port distances on the populated board. The port locations are illustrated in Figure 7.1.

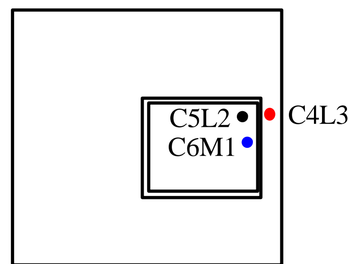
Figure 7.2 illustrates the effect of the gap in populated board with the two ports far away from each other. For the blue curve, the two ports were located at C2D5 and C3M3. For the red curve, the two ports were located at C2D5 and C5L2.

Similarly, Figure 7.3 shows the effect of gap when the two ports were in close proximity. The ports were located at C5L2 and C6M1 for the blue curve, at C5L2 and C4L3 for the red curve, respectively.

Figure 7.4, Figure 7.5, and Figure 7.6 provide more information on $|S_{11}|$ and $|S_{22}|$ measurements with large, small, and medium port distances, respectively. For Figure 7.4, the ports were located at C5L2 on Region 2 and C2D5 on Region 1. For Figure 7.5, the ports were located at C5L2 on Region 2 and C4L3 on Region 1. For Figure 7.6, the ports were located at C5L2 on Region 2 and C8L1 on Region 1.



Port locations for Figure 7.2



Port locations for Figure 7.3

Figure 7.1. Port Locations Used in Experiments

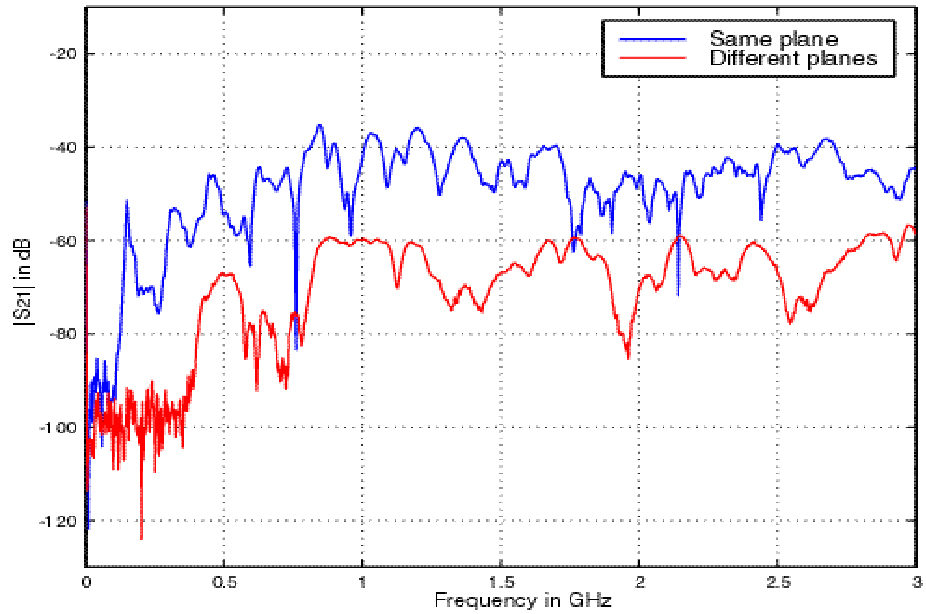


Figure 7.2. Effect of Gap in Populated Board with Distant Ports

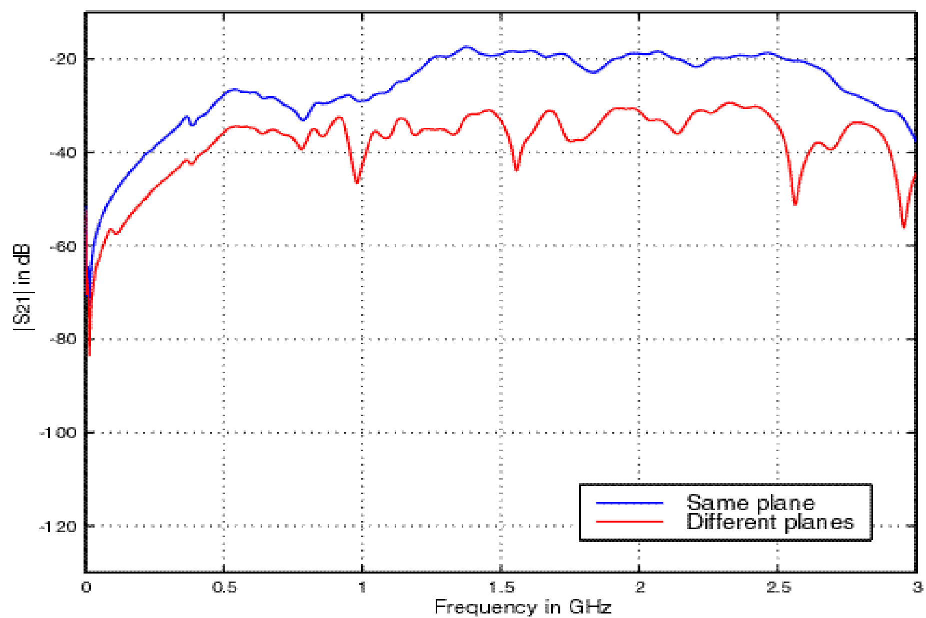


Figure 7.3. Effect of Gap in Populated Board with Close Ports

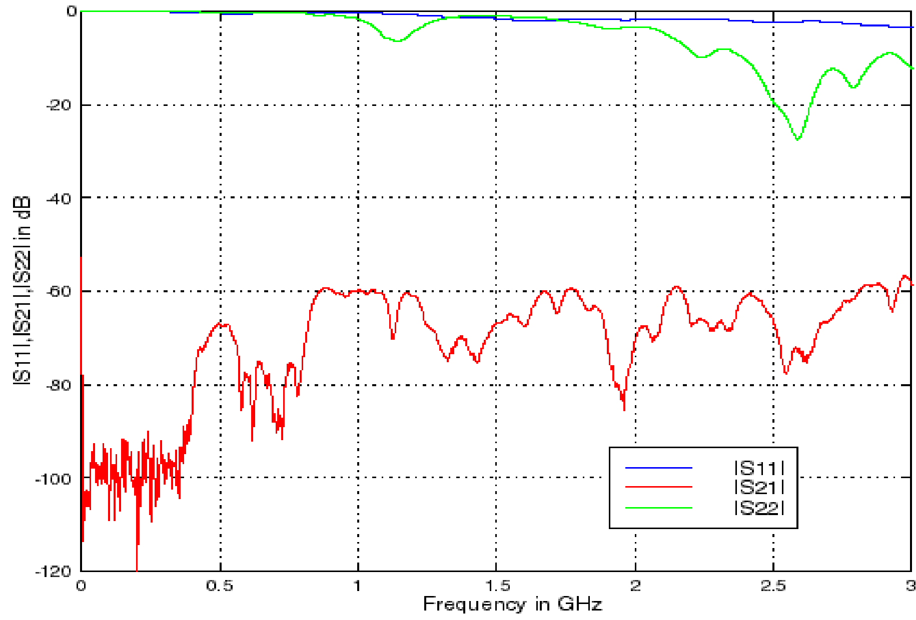


Figure 7.4. S Parameters of Populated Board with Distant Ports

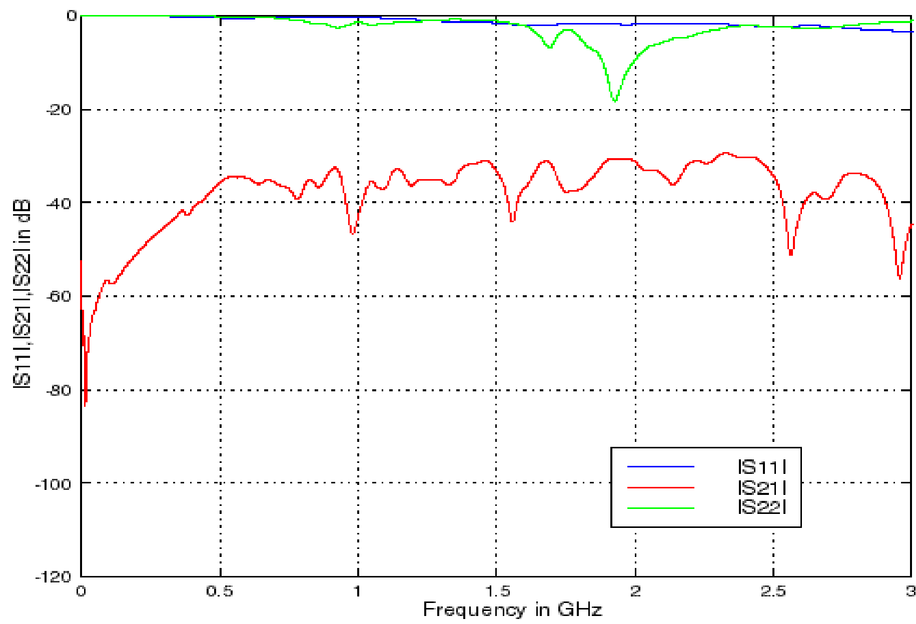


Figure 7.5. S Parameters of Populated Board with Close Ports

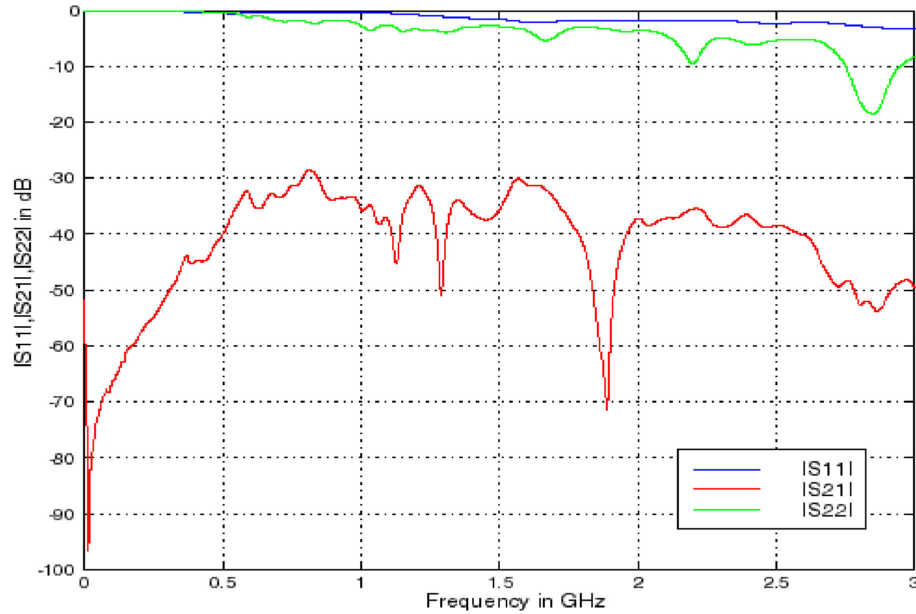


Figure 7.6. S Parameters of Populated Board with Medium Distance Ports

7.2. Isolation in Unpopulated Board (Board 2)

Figure 7.7, Figure 7.8, and Figure 7.9 show the S parameters of Board 2 with large, small, and medium port distances. For Figure 7.7, the ports were located at C5L2 on Region 2 and C2D5 on Region 1. For Figure 7.8, the ports were located at C5L2 on Region 2 and C4L3 on Region 1. For Figure 7.9, the ports were located at C5L2 on Region 2 and C8L1 on Region 1.

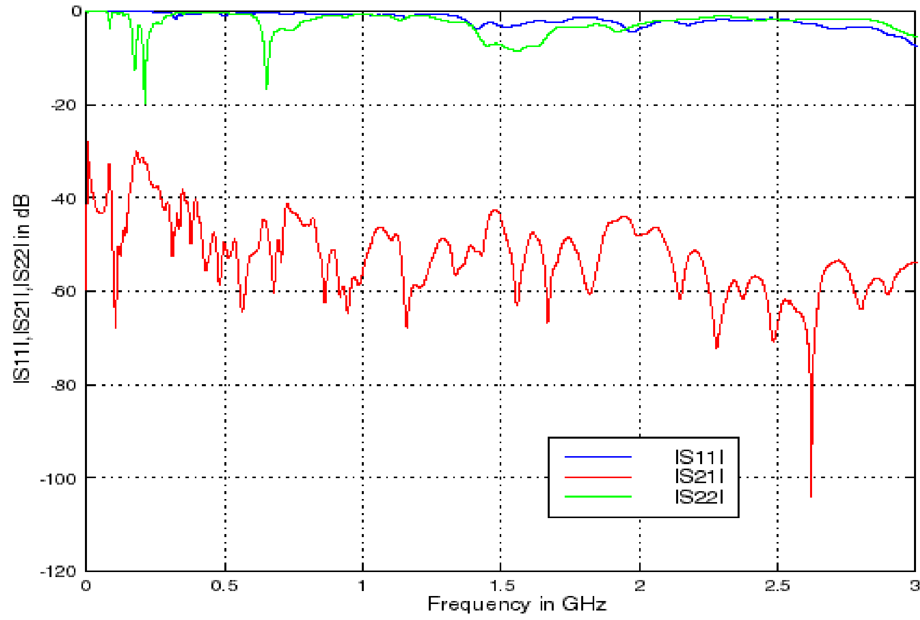


Figure 7.7. S Parameters of Unpopulated Board with Distant Ports

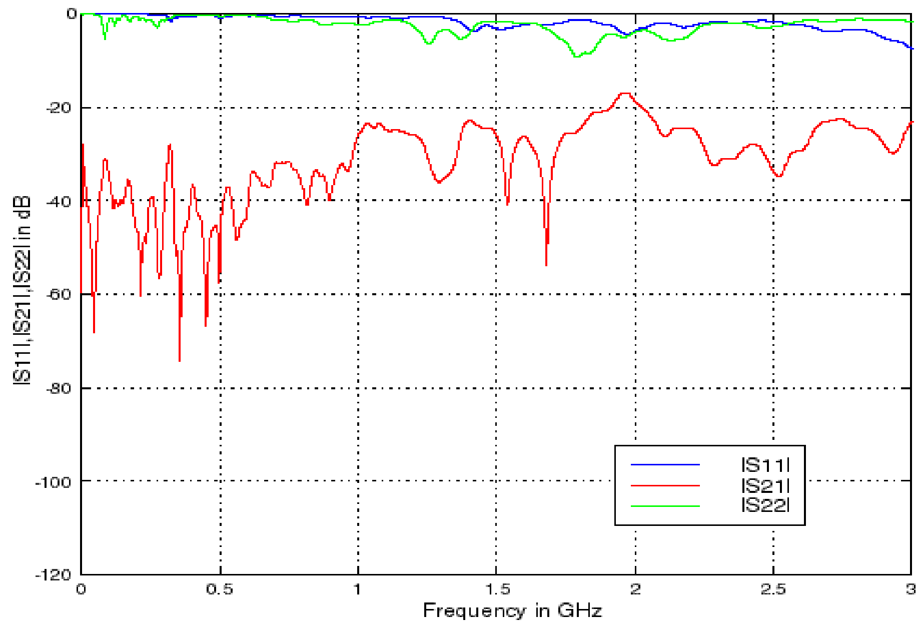


Figure 7.8. S Parameters of Unpopulated Board with Close Ports

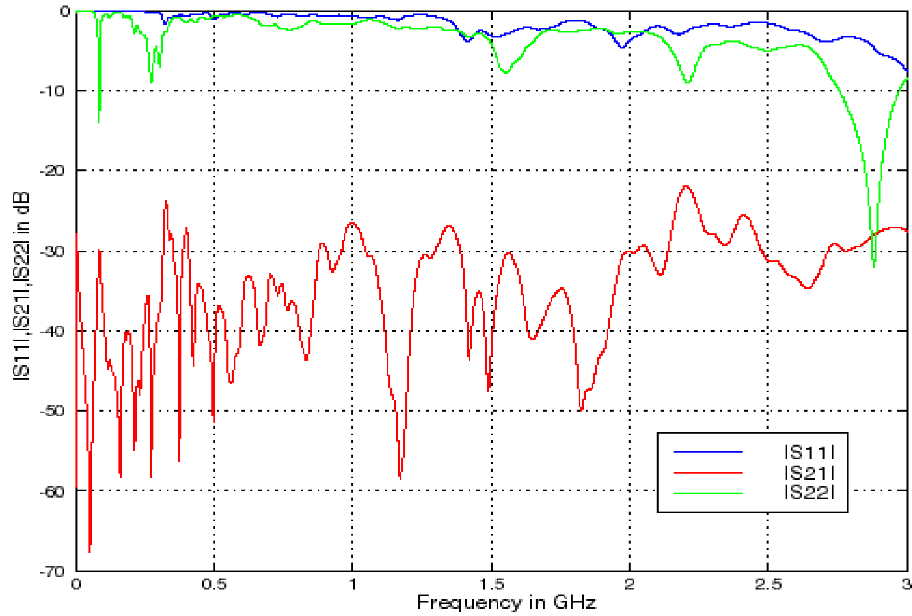


Figure 7.9. S Parameters of Unpopulated Board with Medium Distance Ports

7.3. Isolation in Mock-Up Board (Board 3)

Figure 7.10 compares the measured $|S_{21}|$ between port locations 1 and 3, which were far from each other. Figure 7.11 compares the measured $|S_{21}|$ between port locations 2 and 3.

Figure 7.12, Figure 7.13, and Figure 7.14 provide information of $|S_{11}|$ and $|S_{22}|$ parameters and the correlation between $|S_{11}|$, $|S_{22}|$ and $|S_{21}|$.

Figure 7.15, Figure 7.16 and Figure 7.17 show the effect of copper bridge and ferrite bead bridges over the gap.

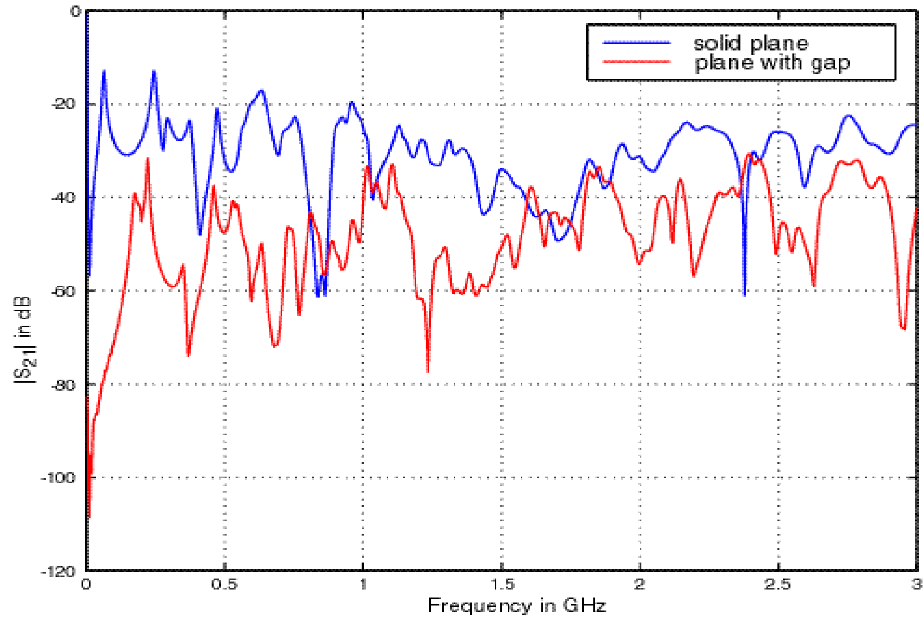


Figure 7.10. Effect of Gap in Mock-Up Board with Ports at L1 and L3

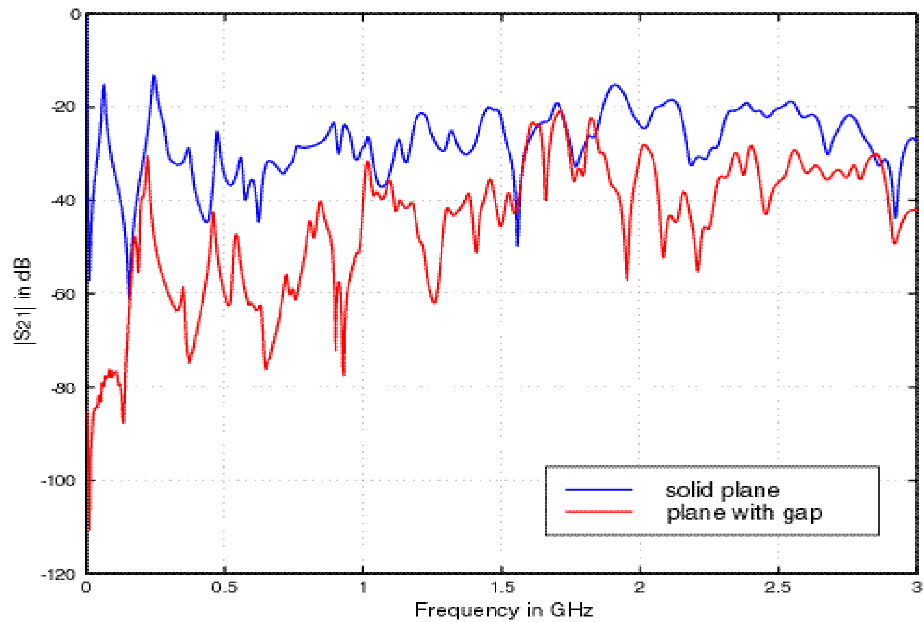


Figure 7.11. Effect of Gap in Mock-Up Board with Ports at L2 and L3

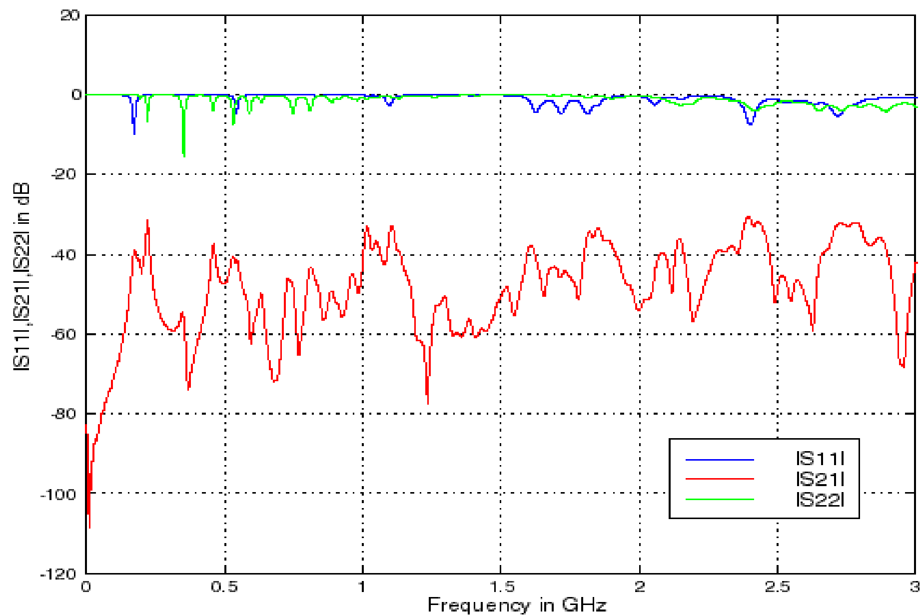


Figure 7.12. S Parameters of Gapped Board 3 with Ports at L1 and L3

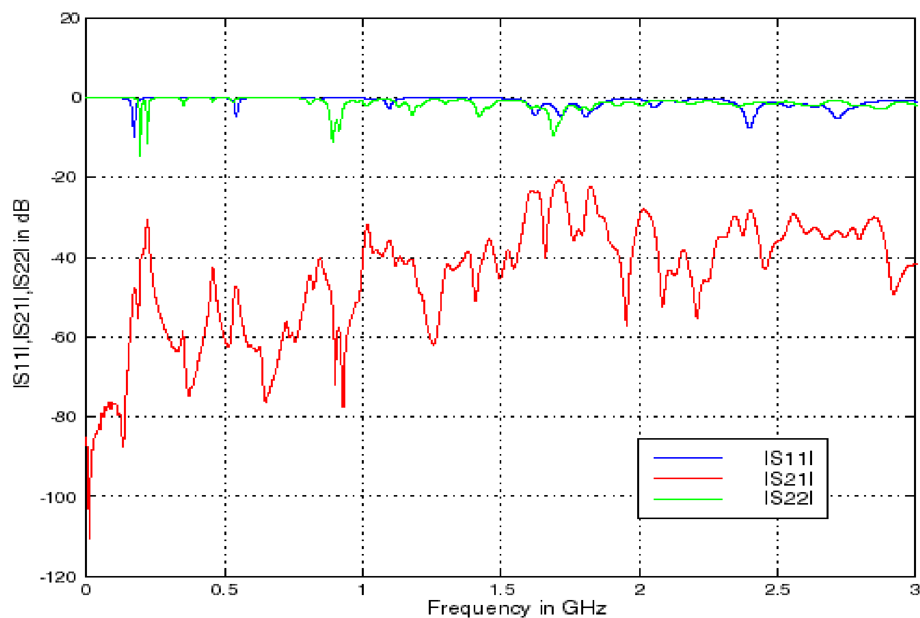


Figure 7.13. S Parameters of Gapped Board 3 with Ports at L2 and L3

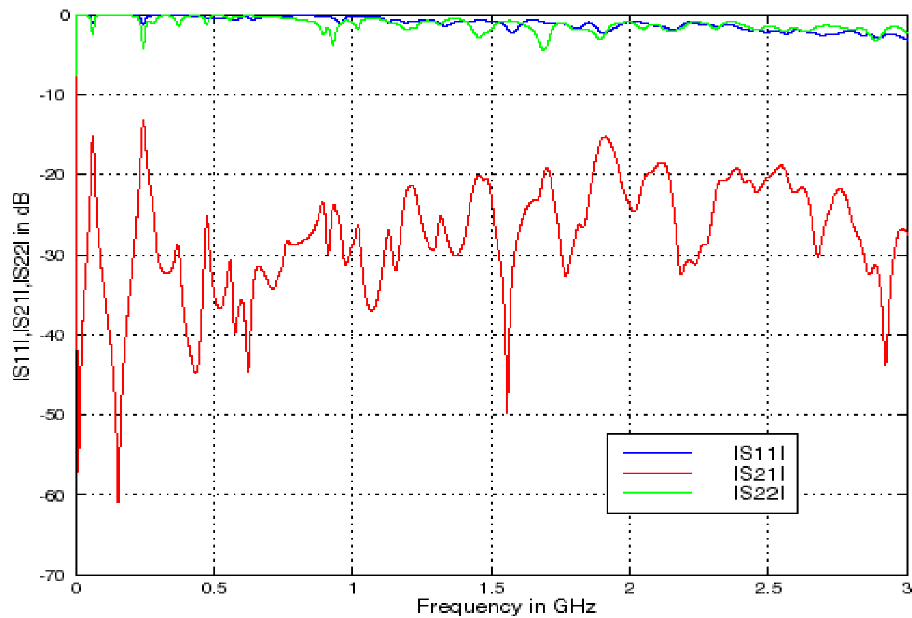


Figure 7.14. S Parameters of Solid Board 3 with Ports at L2 and L3

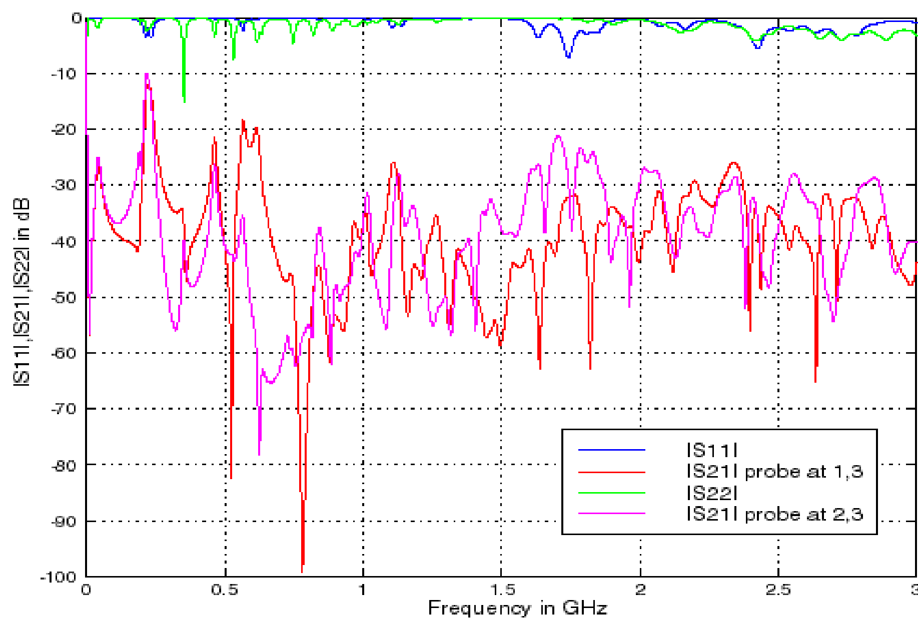


Figure 7.15. Board Isolation with a Copper Bridge at Location 3

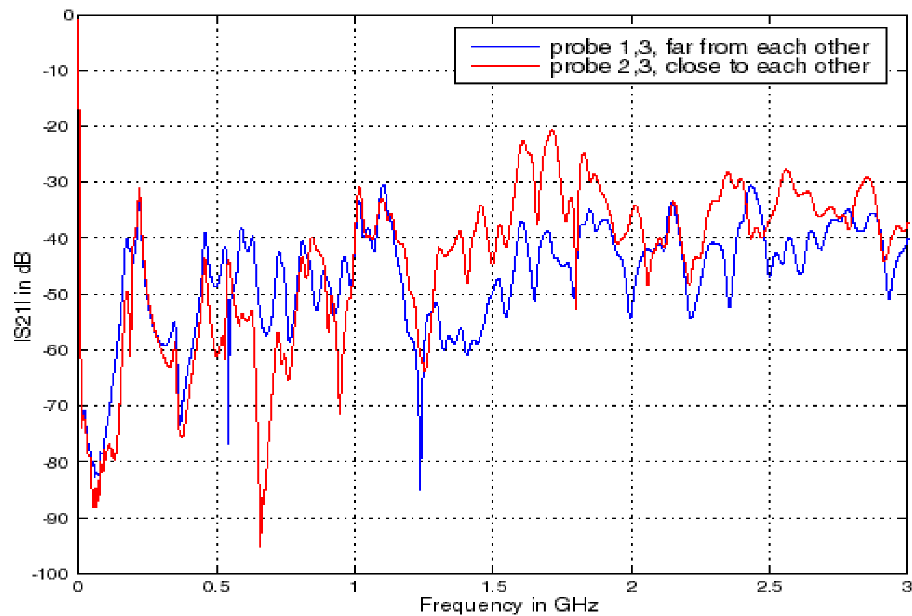


Figure 7.16. Board Isolation with a Ferrite Bead at Location 1

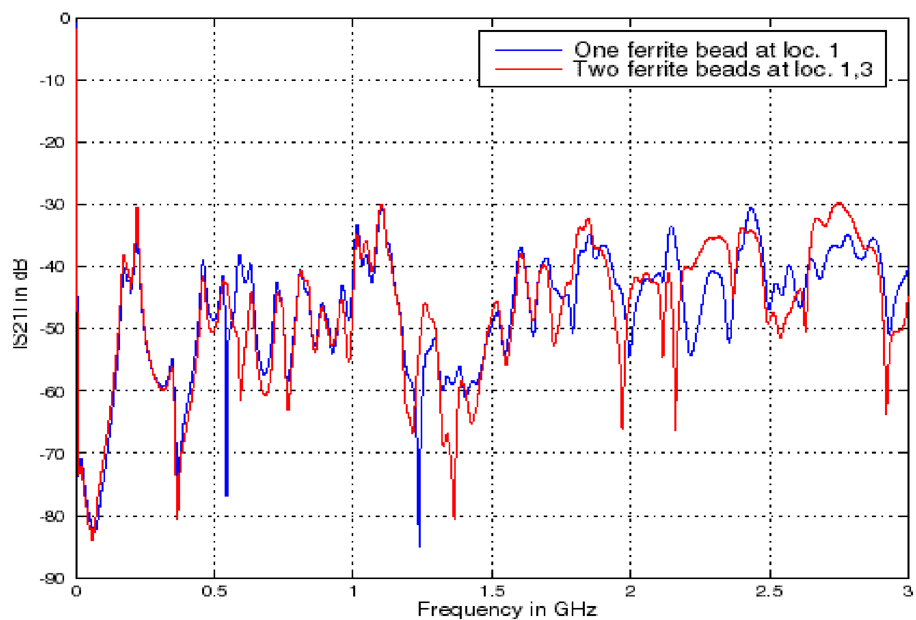


Figure 7.17. Board Isolation with One or Two Ferrite Beads at Locations 1, 3

7.4. Comparison of Isolation in Unpopulated and Populated Boards

The isolations in the unpopulated and the populated boards are compared as shown in Figure 7.18, Figure 7.19, and Figure 7.20. The ports were located at exactly the same locations in these two boards. For Figure 7.18, the ports were at C5L2 and C2D5. For Figure 7.19, the ports were at C5L2 and C4L3. For Figure 7.20, the ports were at C5L2 and C8L1.

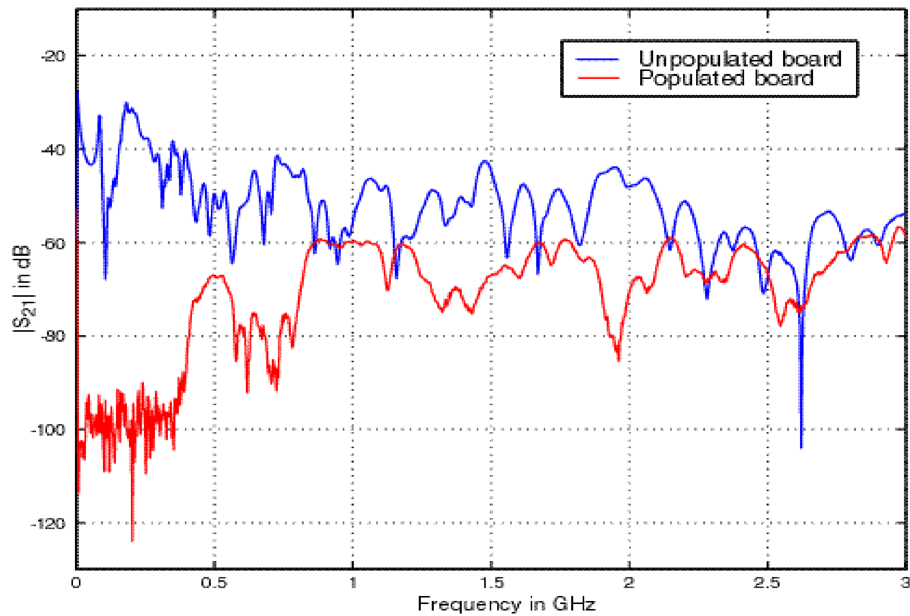


Figure 7.18. Isolation of Unpopulated and Populated Boards with Distant Ports

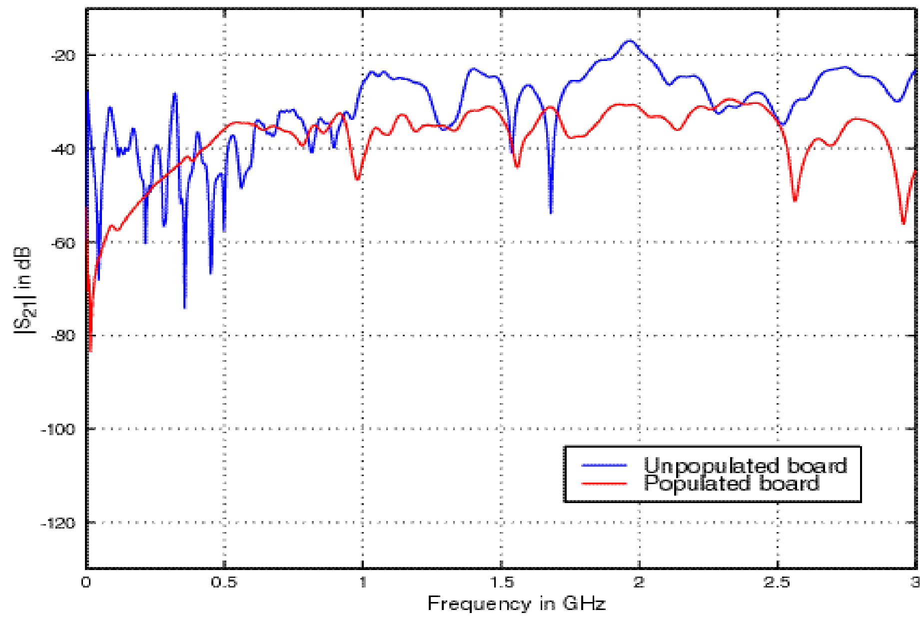


Figure 7.19. Isolation of Unpopulated and Populated Boards with Close Ports

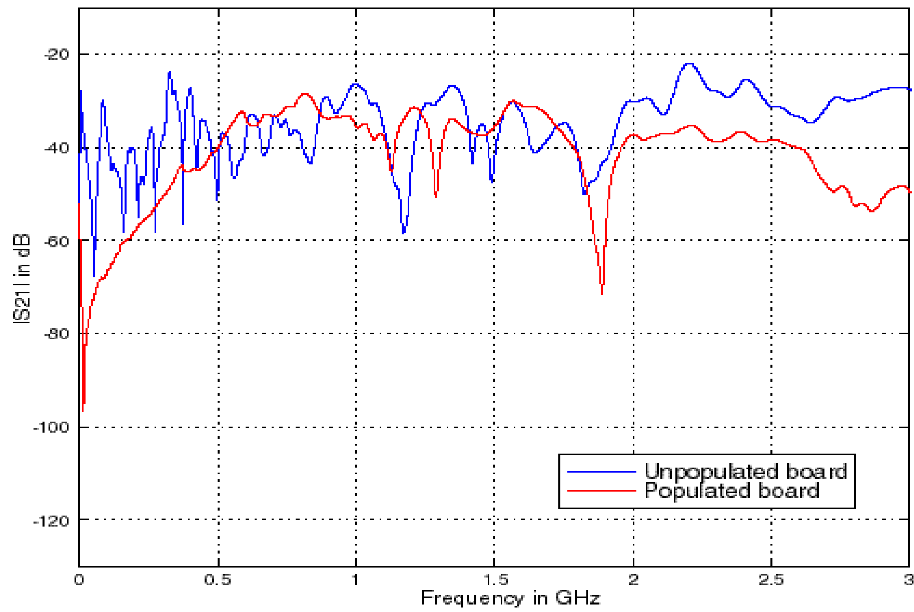


Figure 7.20. Isolation of Unpopulated and Populated Boards with Moderately-Spaced Ports

In the above three cases, the populated board achieves better isolation than unpopulated board. One possibility is the components on the populated board have vias connecting power and return planes, the array of the vias may provide a high frequency shorting path, so the isolation is better in the populated board. To investigate this idea, the chip area in the unpopulated board was sealed by a patch of copper tape, which was used to short the Vcc and ground pins of the chip. The results are shown Figure 7.21 and Figure 7.22. For Figure 7.21, ports were at C6G3 and C5L2 on Region 2. For Figure 7.22, ports were located at C5L2 on Region 2 and C3C2 in Region 1.

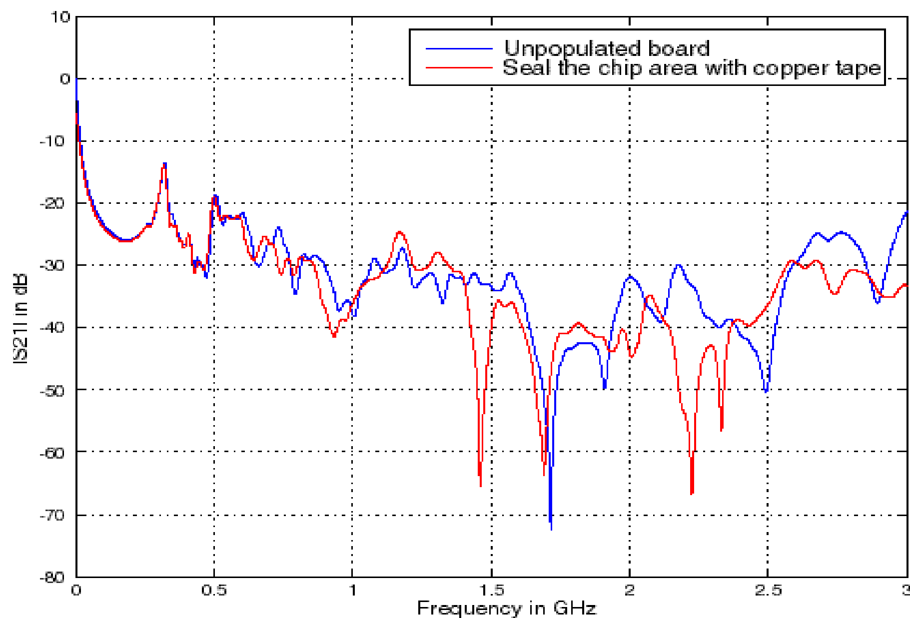


Figure 7.21. Effect of IC Component on Isolation

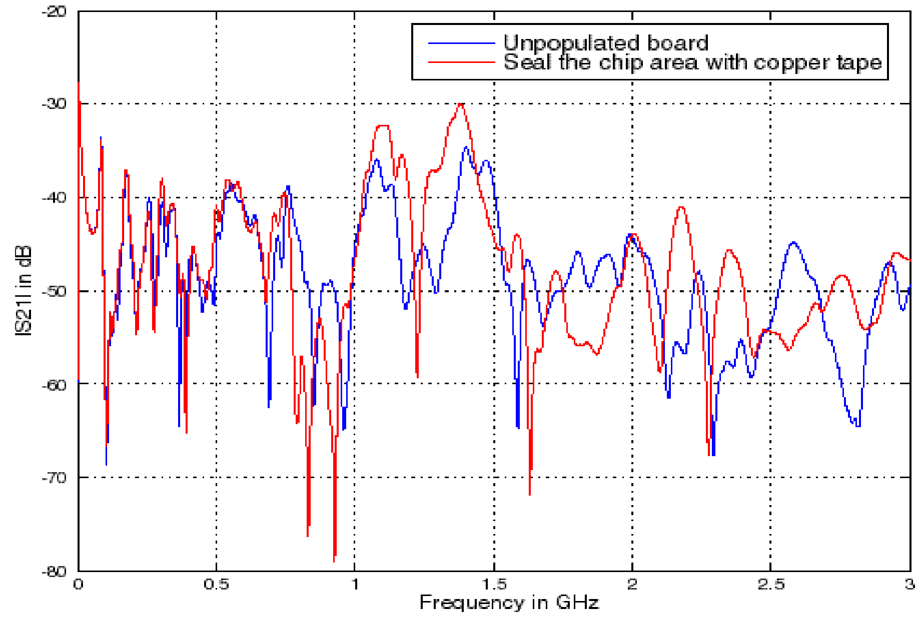


Figure 7.22. Effect of IC Component on Isolation

APPENDIX

Test Procedure for Measuring S Parameters Using HP8753D Network Analyzer

The test procedure for measuring the input impedance of the power bus structures is described below. The words in **bold** face indicate a button on the front panel; the words in *italics* indicate a submenu on the display screen.

1. Turn on the network analyzer, warm up 45 minutes.

2. Connect two precision cables to Ports 1 and 2.

3. Set up measurements: (This step must be done before calibration, since the settings cannot be changed after calibration.)

a). Set frequency range: Press **START**, then press **1**+**M/u** to set the start frequency to 1 MHz. Press **STOP** and **3**+**G/n** to set the stop frequency to 3 GHz.

b). Set the number of sampling points: Press **MENU**, select *NUMBER OF POINTS* in the submenu, then use the up arrow button below the knob to increase this number to 1601 points.

c). Reduce the IF bandwidth to get a stable curve: Press **AVG**, select *IF BW* in the submenu, then use the down arrow button below the knob to decrease the bandwidth to 1000 Hz.

4. Calibration:

a). Change the model of calibration kit: Press **CAL**, then press *CAL KIT[7mm]* in the submenu, select *3.5mmD* as the model of the calibration kit. ("7mm" is the default model.) Press *RETURN*.

b). Set calibration type: Press *CALIBRATE MENU*, then select *FULL 2-PORT* submenu, since S_{11}, S_{22}, and S_{21} will all be measured.

c). Calibrate: Press *REFLECTION*, connect the open termination to Port 1 and press *OPEN* in the *FORWARD* panel in the display. Do the same with the short and matched load terminations to Port 1. Disconnect the standards from Port 1 and connect it to Port 2. Do the same to calibrate Port 2. After calibration, press *STANDARDS DONE*.

Use an f-f connector to connect the two cables to form a through connection. Press *TRANSMISSION*, then press all its submenus in turn.

Press *ISOLATION*, then *OMIT ISOLATION*, then *ISOLATION DONE*.

Complete calibration: press *DONE 2-PORT CAL*. A "Cor" sign will appear at the left side of the screen.

d). Save the calibration: Press **SAVE/RECALL**, choose the first submenu *SAVE STATE* to save the settings and calibrations to the internal memory of the network analyzer.

5. Port extension:

a). Extend Port 1: Press **MEAS**, select *Refl: FWD S11 (A/R)*. Press **FORMAT**, then select *SMITH CHART*. Connect to Port 1 an open or short probe that has the same length as the probe used in DUT. Press **CAL**, select *MORE* in the submenu, then select *PORT EXTENSIONS*. Next, press *EXTENSIONS* submenu on the top to turn the extension on, then press *EXTENSION PORT 1.* Use the knob to increase the delay until the line in the Smith chart turn into a dot in the open or short position. Press *RETURN*, a "Del" sign will appear in the left side of the screen.

b). Extend Port 2: Press **MEAS**, select *Refl: REV S22 (B/R)*. Press **FORMAT**, then select *SMITH CHART*. Connect to Port 2 the same probe, press **CAL**, select *MORE* in the submenu, then select *PORT EXTENSIONS*. Next, press *EXTENSION PORT 2.* Use the knob to adjust the delay as before.

6. Display the results:

a). Remove the probe from the cable, connect the test board.

b). Press **FORMAT**, select *LOG MAG*. Press **MEASURE**, select *Refl: FWD S11 (A/R)* to measure $|S_{11}|$, or select *Trans: FWD S21(B/R)* to measure $|S_{21}|$, or select *Refl: REV S22(B/R)* to measure $|S_{22}|$.

c). Press **SCALE REF** then *AUTO SCALE* to get a good display.

d). Use LabVIEW® to record data.

For more information on how to use the HP8753D network analyzer, refer to the user's guide [1].

REFERENCES

[1] *HP 8753D Network Analyzer User's Guide*, Hewlett Packard, HP Part No. 08753-90257, September, 1995.