MODELING PRINTED CIRCUIT BOARDS WITH EMBEDDED DECOUPLING CAPACITANCE

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Abstract - Embedded capacitance is an alternative to discrete decoupling capacitors and is achieved by enhancing the natural capacitance between power and ground planes. New materials have recently been developed by competing companies that promise to reduce the cost and improve the performance of boards with embedded capacitance. This paper introduces simple models for embedded capacitance boards and examines the properties of these boards that have the greatest impact on their effectiveness.

I. INTRODUCTION

A sudden change in the amount of current drawn by a component on a printed circuit board can cause a momentary drop (or surge) in the voltage on the power distribution bus. This voltage transient can be sufficiently large to interfere with the normal operation of other components on the board. Ground bounce or delta-I noise, as this phenomenon is called, is a common problem in high-speed printed circuit board (PCB) and multi-chip module (MCM) designs. Decoupling capacitors connected to power and ground are typically added to mitigate this problem. Decoupling capacitors help to stabilize the power distribution bus by supplying current that opposes any change in the power bus voltage. However, decoupling capacitors take up space and add cost to printed circuit board designs.

Embedded decoupling takes advantage of the capacitance between the power and ground planes in a printed circuit board to reduce power bus noise. This natural capacitance can be enhanced by locating the power and ground planes very close to each other and by filling the space between the planes with a material that has a high relative permittivity.

II. LUMPED ELEMENT MODELS

Fig. 1 shows a lumped-element model for the power distribution impedance on a board with closely spaced[1] power and ground planes [1]. In general, the lower the impedance between the planes, the lower the voltage that is induced when a current is drawn from the power bus. This lumped element model is valid at frequencies where the planes are electrically small (i.e. small relative to a wavelength). At these frequencies, the plane inductance is negligible and the plane can be modeled with a single capacitor. The effectiveness of capacitors mounted on the surface of the printed circuit board is limited by their interconnect inductance. The model in Fig. 1 can be used to calculate the power bus impedance at frequencies well below the first board resonance. This model is fully explained and validated in [1].

At low frequencies, the impedance of the power bus is approximately equal to,

$$Z_{powerbus} = 1 \Big/ j\omega(C_B + C_1 + C_2 + \cdots + C_n) \qquad (1)$$

and all of the capacitors on the board help to decouple the power bus, although the larger-valued capacitors are most effective. At higher frequencies, some of the decoupling capacitors begin to look like inductors. The inductance of these capacitors forms a resonant circuit with the inter-plane capacitance and the capacitors that do not yet look like inductors. At resonant frequencies, the impedance of the power bus can be very high and the board will tend to ring at these frequencies if there is not sufficient loss to dampen these resonances. A procedure for selecting decoupling capacitors in order to reduce the power bus impedance over a wide band of frequencies is described in [3].

III. DISTRIBUTED MODELS

The lumped element model described in the previous section works very well for estimating the power bus impedance at frequencies below the first board resonance. However, at frequencies where the dimensions of the board are not electrically small, it is

[1] *"closely spaced" is a relative term that depends on how the decoupling capacitors are connected. For typical board designs, this model is valid for a power-ground spacing of 10 mils or less. Models for boards with wider plane spacing must account for the mutual inductance between vias [2].*

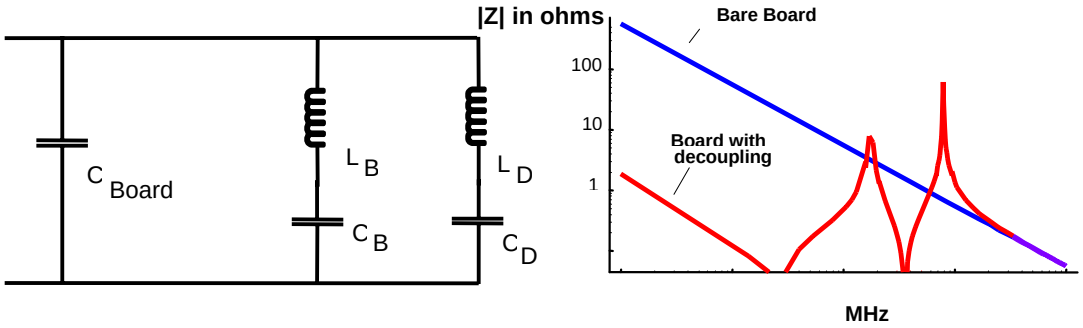

Fig. 1 - Lumped element model of power bus with decoupling capacitors.

necessary to employ more complex distributed models. Rubin and Becker [4] and others have modeled electrically large printed circuit boards using a grid of lumped resistors, capacitors and inductors. Novak [5] uses a grid of transmission lines to model power bus structures. Shi [6] developed a 2D integral equation code for analyzing power buses. Each of these techniques can be used in conjunction with SPICE models of active devices to model the behavior of power-ground plane pairs. However, these models are relatively complex and they require a significant amount of time and expertise to implement properly.

III.1 THE CAVITY MODEL

Although the cavity model described in this section is not particularly simple, it is reasonably intuitive. Conclusions drawn by modeling printed circuit board planes as rectangular resonant cavities, can be extended to develop design guidelines for complex PCB structures of arbitrary shape..

Since most boards are electrically thin, they can be modeled as TM_z cavities with two perfect electric conductor (PEC) walls representing the power and ground planes. The sides of rectangular boards can be modeled with four perfect magnetic conductor (PMC) sidewalls. For the lossless case, the input impedance of this geometry is given by [7]:

$$Z_{in} = j\omega\mu h \sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\left[\begin{array}{c}\dfrac{\chi_{mn}^2 \cos^2(k_{yn}y_i)\cos^2(k_{xm}x_i)}{ab\left(k_{xm}^2 + k_{yn}^2 - k^2\right)} \\ * \operatorname{sinc}^2\left(\dfrac{k_{yn}dy_i}{2}\right)\operatorname{sinc}^2\left(\dfrac{k_{xm}dx_i}{2}\right)\end{array}\right] \quad (2)$$

where:

$$k_{xm} = \frac{m\pi}{a}, \quad k_{yn} = \frac{n\pi}{b}, \quad k = \omega\sqrt{\varepsilon\mu}\,.$$

$\chi_{mn}^2 = 1$ for m=n=0; $\chi_{mn}^2 = 2$ for m=0 or n=0; $\chi_{mn}^2 = 4$ for m≠0, n≠0.

(x_i, y_i) is the center location of the feeding port.

(dx_i, dy_i) is the dimension of the feeding port

According to Eq. (1), beyond the first series resonance frequency, the input impedance of the power-ground structure is inductive except at cavity resonance frequencies given by,

$$f_{mn} = \frac{1}{2\pi\sqrt{\mu\varepsilon}}\sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2}\,. \quad (3)$$

When the plane spacing is not very thin at the highest frequency of interest, the effect of fringing fields must be taken into consideration by adjusting the dimensions of the structure to an effective length and width. Several formulas have been proposed to calculate the resonance frequencies in the presence of a fringing field [8]. However, most printed circuit boards employing embedded capacitance have very thin dielectric substrates, so the fringing effect can often be neglected.

The input impedance of a 15.2-cm by 10.2-cm FR-4 board was measured in the lab and calculated using Eq. (2). A comparison between the calculated and measured results from 0-2 GHz is shown in Fig. 2. In general, the calculation agrees fairly well with the measurement. The slight frequency shift between the calculated and measured resonance frequencies is mainly due to the fringing effect for this 100-μm thick board. The most significant difference between the two curves in Fig. 2 is the magnitude of the input impedance at resonance frequencies. The measured result has finite impedance values at resonance due to copper, dielectric and radiation losses. The cavity model, Eq. (2), predicts an infinite $|Z_{in}|$ at resonance frequencies, since it does not account for loss.

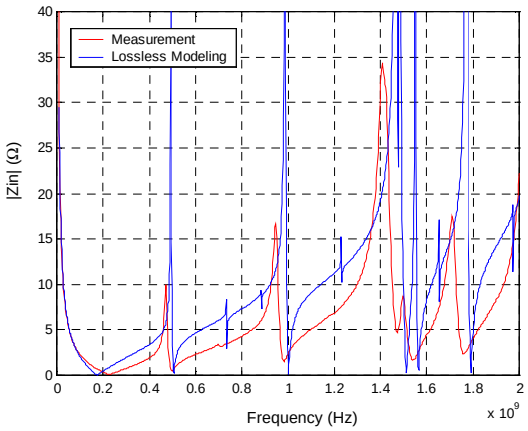

Fig. 2 - Input impedance of a 15.2-cm by 10.2-cm FR-4 board.

III.2 QUALITY FACTOR

At cavity resonance frequencies, the magnitudes of the input impedance are related to the quality factor (or Q factor) of the resonance. Real power-ground plane structures exhibit loss due to the finite resistance of the copper walls, conduction loss in the dielectric, radiation loss, and losses due to surface waves induced on the outer surface of the copper. Surface wave losses are usually small compared to the other losses in normal power-bus geometries.

Formulas for conductive loss and dielectric loss are well documented [8]. For very thin dielectric layers between power and ground planes, an approximate formula for the quality factor due to conductive losses in the top and bottom planes is given by,

$$Q_c \approx h\sqrt{\pi f \mu \sigma}\ . \qquad (4)$$

The quality factor due to dielectric losses is given by,

$$Q_d = 1 \big/ \tan\delta\ . \qquad (5)$$

In general, the quality factor due to the radiation loss has to be numerically evaluated for a specific mode. However, an approximate closed form expression is provided in [11] for the quality factor due to radiation loss at the dominant TM_{10} mode of structures with thin dielectric layers. The radiation quality factor is given by,

$$Q_{rad} = \frac{3}{16}\frac{\varepsilon_r L_e \lambda_0}{p c_1 w_e h} \qquad (6)$$

where:

$$p = 1 + \frac{a_2}{10}(k_0 w_e)^2 + \left(a_2^2 + 2a_4\right)\left(\frac{3}{560}\right)(k_0 w_e)^4 + c_2\left(\frac{1}{5}\right)(k_0 L_e)^2$$
$$+ a_2 c_2\left(\frac{1}{70}\right)(k_0 w_e)^2 (k_0 L_e)^2$$

$$a_2 = -0.16605 \qquad a_4 = 0.00761 \qquad c_2 = -0.0914153$$

$$c_1 = \frac{1}{n_1^2} + \frac{2/5}{n_1^4} \qquad n_1 = \sqrt{\varepsilon_r \mu_r}\ .$$

w_e and L_e are the effective dimensions of the structure after accounting for the fringing effect.

The overall quality factor can be approximated by,

$$\frac{1}{Q} = \frac{1}{Q_c} + \frac{1}{Q_d} + \frac{1}{Q_{rad}}\ . \qquad (7)$$

The input impedance around resonance frequencies is related to the quality factor of the structure. Formulas to calculate the quality factor associated with the conductive loss, the dielectric loss, and the radiation loss can be applied to estimate the overall quality factor at each resonant frequency. The input impedance around the resonance frequency can then be calculated from a narrow-band equivalent circuit of the cavity model. Plugging typical values of dielectric loss, copper conductivity and circuit board dimensions into Eqs. (3)-(5), suggests that copper losses will be the dominant loss mechanism in most embedded capacitance boards. This will be confirmed by the measurement results presented in the next section.

IV. MEASUREMENTS

A variety of board employing embedded capacitance were measured as part of a study led by the National Center for Manufacturing Sciences (NCMS) in Ann Arbor, Michigan [9]. Test boards with 4 kinds of embedded capacitance manufactured by various manufacturers were evaluated. Mechanical, electrical and reliability data was gathered for each embedded capacitance material.

Details of the measurements conducted for this study and the results obtained are provided in [9]. In the following sections, measured results for boards with and without embedded capacitance are compared to cavity model predictions.

IV.1 Resonant Frequency Analysis

The measured input impedance of an unpopulated printed circuit board is plotted in Fig. 4.

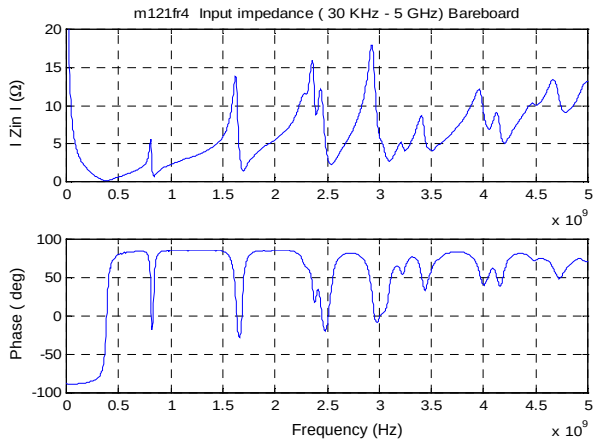

Fig. 4 - Input impedance of an FR-4 board.

This test board was 7.6 cm long and 5 cm wide. It was a six-layer board with ground and power planes on layers 2 and 5, respectively. Between the two solid planes, there was a 500-µm FR-4 dielectric layer. The relative permittivity of the dielectric layer was about 5 and the total board capacitance was about 350 pF. The structure was fed by an SMA jack located at (1.1", 1.0"). The radius of the center conductor of the SMA jack was 640 µm. Fig. 4 indicates that the test board behaved like a capacitance at very low frequencies. It exhibited a series resonance at 387 MHz and at higher frequencies the input impedance was inductive except at the resonance frequencies.

At low frequencies, the lumped circuit model for the unpopulated board is simply the board capacitance. As the frequency approaches the series resonance at 387 MHz, the length of the test board is more than one-fifth of a wavelength. To characterize the input impedance at

frequencies above 387 MHz, we can switch from the lumped element model to the cavity model. The first few cut-off frequencies predicted by the cavity model are listed in Table 1.

Table I – Resonance Frequencies Calculated for the 7.6-cm x 5.0-cm FR-4 Board

Mode	Frequency in MHz
TM10	883
TM01	Not excited
TM11	1584
TM20	1765
TM21	2201
TM02	2631
TM30	2648

Due to the location of the measurement port, some modes were not excited and do not appear in the measured input impedance. In addition, a frequency shift is observed between the calculated cut-off frequencies and the measured results. For example, the first cavity resonance was measured at 825 MHz, while the cavity model prediction was 883 MHz. These shifts are primarily due to fringing effects. Fringing fields at the board edge make the board appear slightly larger than it really is resulting in a downward shift in the resonance frequencies. Fringing is more of a factor in boards that have greater plane spacing or smaller board areas.

IV.2 Populated Board Measurements

Fig. 5 shows the input impedance of two 7.6-cm x 5-cm FR-4 boards with a 100-µm spacing between the power and ground planes. The board without decoupling capacitors has a sharp resonance peak below 200 MHz. This is not a board resonance, but rather a resonance between the board's inter-plane capacitance and the inductance of the connections to devices mounted on the surface. At low frequencies, the decoupling capacitors do a good job of eliminating this resonance. However, above 100 MHz, the decoupling capacitors have too much connection inductance to be effective. There is no significant difference between these two curves above 100 MHz other than a slight shift in the resonance frequencies.

Fig. 6 compares the input impedance of an FR-4 board that has a 500-µm plane spacing to that of an EmCap board with a 100-µm plane spacing. Resonant peaks in the power impedance are significantly damped in the EmCap board.

Fig. 7 compares the input impedance of a 100-µm EmCap board to that of a board made with a new material called C-Ply that has a plane spacing of approximately 6 µm. The input impedance curve for the C-Ply board is smoother than that of the EMCAP board. All of the cavity resonances are effectively damped.

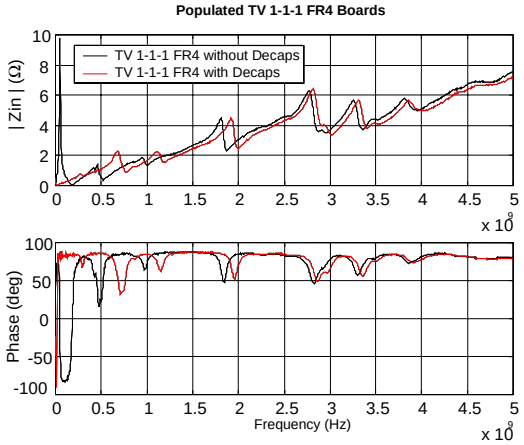

Fig. 5 - Input impedance of FR-4 boards with and without decoupling capacitors.

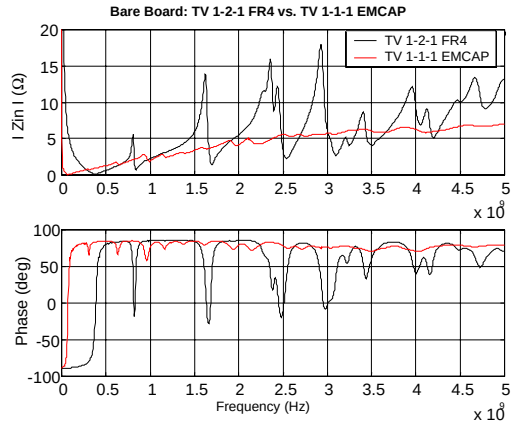

Fig. 6 - Input impedance of unpopulated boards with 500-mm FR-4 and 100-mm EmCap materials.

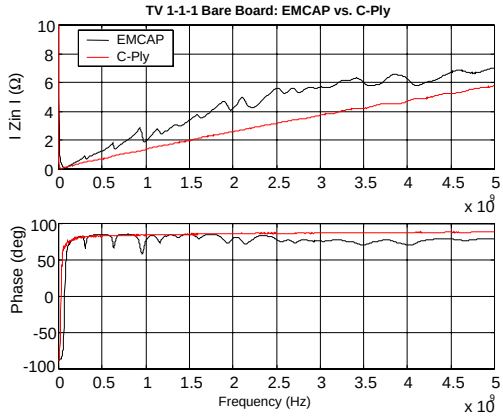

Fig. 7 - Input impedance of unpopulated boards with 100-µm EmCap and ~6-µm C-Ply materials.

V. QUALITY FACTOR ANALYSIS

For test boards employing embedded capacitance materials, the input impedance curves were relatively smooth. The FR-4 boards exhibited significant peaks at power bus resonant frequencies. As discussed in Section III.2, the magnitude of input impedance near resonance frequencies is related to the quality factor of the power-ground plane structure. The relative permitti-

vities and loss tangents of the embedded capacitance materials evaluated during the NCMS study were measured by NIST at several frequencies.

Table II – Calculated Quality Factors

Samples	f_{10} (MHz)	Q_d	Q_c	Q_{rad}	Total Q
(2” x 3”) 500-µm FR-4	997	48	235	1582	39
(2” x 3”) 100-µm FR-4	997	48	55	6819	25
(4” x 6”) 100-µm FR-4	470	44	28	21312	17
(8” x 9”) 100-µm FR-4	310	44	22	25265	15
(2” x 3”) 50-µm BC2000	1002	48	26	14302	17
(4” x 6”) 50-µm BC2000	482	42	18	29713	12
(8” x 9”) 50-µm BC2000	318	42	14	35790	11
(2” x 3”) 100-µm EmCap	328	66	28	7.17E+05	20
(4” x 6”) 100-µm EmCap	159	60	19	1.47E+06	15
(8” x 9”) 100-µm EmCap	104	55	16	1.77E+06	12
(2” x 3”) 30-µm Hi-K	567	919	13	2.23E+05	11
(4” x 6”) 30-µm Hi-K	277	122	9.0	4.36E+05	8
(8” x 9”) 30-µm Hi-K	183	122.0	7.3	5.25E+05	7
(2” x 3”) ~6-µm C-Ply	426	22.9	4.0	2.00E+06	3
(4” x 6”) ~6-µm C-Ply	206	22.9	2.8	4.04E+06	2

Using these material parameters and Eqs. (4)-(6), the quality factors related to the copper loss, dielectric loss, and radiation loss were calculated for the dominant TM_{10} mode of several test boards. The total quality factor was then calculated using Eq. (7). The results are summarized in Table II.

As the data in Table II indicates, the radiation loss is relatively small compared to the dielectric loss and conductive loss for all sample configurations (i.e. Q_{rad} was much higher than Q_d or Q_c). Radiation loss had little effect on the total quality factor for the TM_{10} mode.

The dominant loss mechanism depends on the thickness of the dielectric. Q_c is proportional to the thickness of the dielectric layer while Q_d is independent of thickness. For power-ground plane structures with very thin dielectric layers, especially at low frequencies, conductive loss is the dominant factor. In thicker materials, the quality factor is generally dominated by the dielectric loss of the material. Higher loss equates to more effective dampening of the power-ground structure resonances.

According to Table II, all test boards employing embedded capacitance materials have smaller quality factors (higher loss) than the corresponding FR-4 version for the dominant TM_{10} mode. The quality factor of the 6-µm C-Ply board is about one-eighth that of the 500-µm FR-4 board. This low quality factor results in the smooth input impedance curves in Fig. 7.

VI. EFFECT OF BOARD SIZE

It is clear from the expressions in Eqs. (4) and (5) that the Q due to conductor and dielectric loss is not dependent on the board area. The small differences in the Q of boards with different areas in Table II is due to the slightly different values of loss tangent and skin depth associated with the different resonant frequencies of the various sized boards.

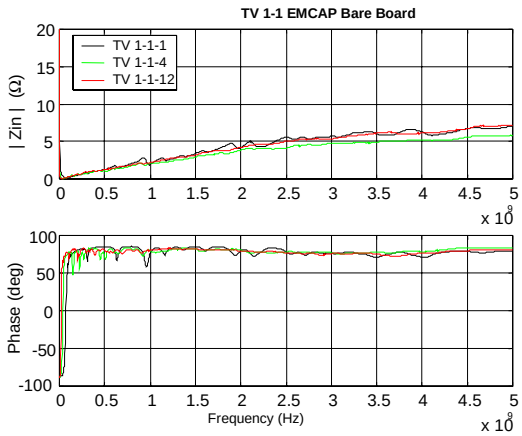

Fig. 8 - Input Impedance of Unpopulated 100-µm EmCap Boards with Different Sizes

Fig. 8 shows the input impedance measured for three sizes of EmCap boards. There is relatively little difference in the Q of the resonances in these curves.

VII. CONCLUSION

At frequencies above 1 GHz, discrete decoupling capacitors lose their effectiveness due to the inductance associated with their connection to the power bus. Embedded capacitance on the other hand is effective at frequencies well above 1 GHz.

At low frequencies, the current supplied by embedded capacitance is at least as high as the current supplied by discrete capacitors with the same total capacitance value. At higher frequencies the current supplied by embedded capacitance is greater because the inductance of the connections to the discrete capacitors limits the amount of charge they can supply is a very short time.

At very high frequencies (typically above a few hundred megahertz), the inductance of the connections to the local decoupling capacitors makes them relatively ineffective. Current is initially drawn from the planes. The frequency at which the discrete capacitors become ineffective depends on the relative inductance of their connections as compared to the impedance of the planes. For most practical board geometries, with planes spaced 250 μm apart or less, discrete capacitors are ineffective at frequencies greater than about 1 GHz.

At frequencies where the board is not electrically small, board resonances (if not sufficiently damped) are the most significant problem. Boards without sufficient loss in the power bus will tend to "ring" at the frequencies at which the power planes resonate. If a source harmonic happens to occur at a board resonance, the power bus noise voltage may be excessive.

A simple cavity model for the power-ground plane pair in embedded capacitance boards reveals that a key factor affecting the value of the input impedance is the Q-factor. Q-factors much greater than 1 imply that the board impedance will peak at certain frequencies resulting in higher levels of power bus noise when the board is excited at those frequencies.

Boards with embedded capacitance are more immune to board resonance problems than boards with widely spaced power and ground planes. Relatively simple calculations show that when the dielectric spacing is on the order of a skin depth in the copper, the board resonances will be dampened by the conductive loss in the planes.

In general, all of the materials evaluated as part of the NCMS project did a fair job of dampening power bus resonances. However, the C-Ply material, with its ~6-μm plane spacing, was the only material to essentially eliminate these resonances. The modeling suggests that the dielectric constant and the loss tangent of this material had relatively little to due with its ability to suppress power bus resonances. The reason this material performed so well was due to the very small plane spacing.

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