An improved model for representing current waveforms in CMOS circuits

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Abstract— **A resistance-inductance-capacitance (RLC) model is described for estimating current waveforms in digital CMOS circuits. The model is based on parameters that are readily derived from information available in board layout files and component data sheets or IBIS (I/O buffer information specification) files. Compared with the simpler triangular waveform traditionally used to approximate current in CMOS circuits, the RLC model more accurately estimates the shape of the current waveform in the time domain and the amplitudes of the upper harmonics in the frequency domain.**

I. INTRODUCTION

Estimating the radiated electromagnetic emissions or crosstalk due to signals on a printed circuit board requires an estimate of the signal current. Normally, more emphasis is placed on modeling and controlling the signal voltage in digital circuits. For binary digital signals, the voltage waveform alternates between a high and low level. However the current waveform can look very different, particularly in CMOS circuits with a capacitive load. T. Van Doren introduced a simple triangular pulse waveform model for estimating power-bus noise currents in CMOS circuits for an expert system evaluating emissions from PCB designs [1], which is shown in Figure 1.

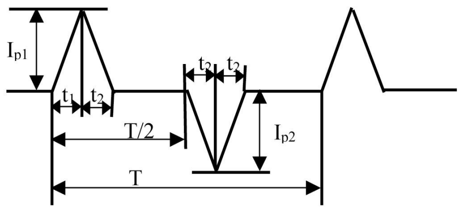

Fig.1 Triangular model waveform for switching current.

J. Chen [2] and J. Mao [3] have applied this model to estimate power-bus noise due to multiple devices switching simultaneously. A similar model has been used by other researchers to estimate both signal and power currents [4]-[18]. For example, N. Na used triangular waveforms to model core switching currents [8][10]; L. Bouhouch used a similar waveform to model controller I/O switching currents [9]; and Kriplani employed a triangular waveform to model capacitive load currents [15].

The triangular waveform model has the advantage that it is based only on the amplitude and risetime of the voltage waveform. These parameters are generally readily available. However, this simple model does not do a good job of estimating the amplitude of the upper harmonics that are often very important when trying to anticipate or model a radiated emissions problem. Furthermore, with the advent of IBIS models and better simulation tools, information about the source and load impedances is often readily available. This makes it possible to obtain reasonably accurate current waveforms directly from voltage waveforms. This paper explores the possibility of replacing triangular waveform current estimates with estimates based on a series RLC model for CMOS circuits.

Simple formulas are derived for the current based on parameters that are normally available or readily estimated for CMOS circuits. The paper is organized as follows: Sections II and III describe the derivation of the new model. In Section IV, the measured current spectrum from a test board is compared with the new model and triangular model calculations.

II. RLC MODEL

The transient current drawn from a CMOS IC by a nearby CMOS load can be estimated using an RLC series equivalent circuit as shown in Figure 2.

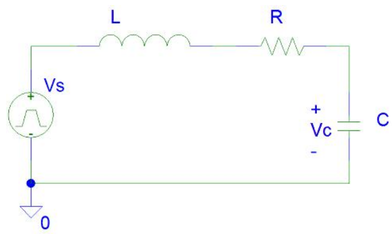

Fig.2 Equivalent RLC circuit for a CMOS output gate and its load.

The voltage source and resistance represent the Thevenin equivalent model for the CMOS source. L represents the connection inductance between the source and load and C is the input capacitance of the receiving device.

$$R \sim \frac{V_{CC} - V_{OH}}{I_{OUT}} \tag{1}$$

R can be obtained from IBIS voltage-current plots or estimated from the device data sheet as [19], L depends on the geometry of the connection between the source and load. It can generally be estimated using simple closed-form formulas [20]. The voltage across the capacitor, V_C , can be determined by solving the second-order differential equation,

$$\frac{d^2V_C}{dt^2} + 2\xi\omega_n \frac{dV_C}{dt} + V_C = \omega_n{}^2 V_s \tag{2}$$

where ξ is the damping factor of the circuit, and ω_n is the intrinsic resonance angular frequency of the circuit,

$$\xi = \frac{1}{2Q} = R_l \Big/ 2\sqrt{L_l / C_l} \tag{3}$$

$$\omega_n = \frac{1}{\sqrt{L_l C_l}} \tag{4}$$

The load current is then given by

$$i_C = C\frac{dV_C}{dt} \tag{5}$$

and the step response of (5) is given by

$$i_C(t) = \begin{cases} \Delta V \dfrac{C_l\omega_n}{2\sqrt{\xi^2-1}}\left(e^{-(\xi-\sqrt{\xi^2-1})\omega_n t} - e^{-(\xi+\sqrt{\xi^2-1})\omega_n t}\right)u(t), & \xi > 1, \\ \Delta V \dfrac{1}{L_l} t e^{-t/\omega_n} u(t), & \xi = 1, \\ \Delta V \dfrac{C_l\omega_n}{\sqrt{1-\xi^2}} e^{-\xi\omega_n t} \sin\sqrt{1-\xi^2}\,\omega_n t\, u(t), & \xi < 1, \end{cases} \tag{6}$$

where $u(t)$ is the unit step function and ΔV is the amplitude of the source. The spectrum of the load current can be expressed in a simple closed form,

$$I(f) = \frac{2\Delta V}{j\omega} \frac{1}{R_l + j\omega L_l + 1/j\omega C_l} \tag{7}$$

III. Effect of Finite Rise Time

The transient current drawn by an IC device is also influenced by the source risetime. At high frequencies, finite risetimes cause harmonics of the source to fall off more rapidly. Practical models to estimate the current spectrum from CMOS sources above a few hundred MHz must take into account the finite risetime of the CMOS driver. The finite risetime of the voltage step supplying the RLC equivalent circuit can be accounted for in the frequency domain by simply multiplying by the source spectrum. For periodic trapezoidal waveforms, where T is the period of the voltage source and t_r is the rise and falltime of source; the magnitude of the current spectrum can be expressed as,

$$|I(nf_0)| = \frac{|V_S(nf_0)|}{\left|R_l + j2\pi n f_0 L_l + 1/j2\pi n f_0 C_l\right|} \tag{8}$$

where f_0 is the fundamental frequency of the voltage source and $V_S(nf_0)$ is the magnitude of the source spectrum which is given by,

$$|V_S(nf_0)| = \begin{cases} \dfrac{2\Delta V}{n\pi}, & n < \dfrac{T}{\pi t_r} \\ \dfrac{2\Delta V}{(n\pi)^2}\dfrac{T}{t_r}, & n > \dfrac{T}{\pi t_r} \end{cases} \tag{9}$$

where n is an odd integer ≥ 1. We can obtain expressions for the envelope of the load current and source voltage by replacing nf_0 with f in Equations (8) and (9) respectively,

$$|I(f)| = \frac{|V_S(f)|}{\left|R_l + j2\pi f L_l + 1/j2\pi f C_l\right|} \tag{10}$$

$$|V_S(f)| = \begin{cases} \dfrac{2}{T}\dfrac{\Delta V}{\pi f}, & f < \dfrac{1}{\pi t_r} \\ \dfrac{2}{T}\dfrac{\Delta V}{(\pi f)^2}\dfrac{1}{t_r}, & f > \dfrac{1}{\pi t_r} \end{cases} \tag{11}$$

Generally, it is better to calculate the envelope (maximum value) when estimating currents for EMC calculations, because small variations in the duty cycle can have a significant effect on the amplitude of individual upper harmonics.

IV. Model Results vs. Measurements and Triangular Approximation Results

The expression for maximum estimated current in Equations (10) and (11) was evaluated experimentally and compared to the triangular approximation. Fig. 3 shows the equivalent circuit used for these comparisons. A CMOS clock buffer was driven by a signal source (a 50-MHz oscillator) and was loaded with capacitors of different values. A 2-ohm resistor was connected in series with the load capacitor in order to measure the load current. The parasitic inductance of the load interconnect was about 10 nH. The turn-on resistance of the CMOS buffer was about 4 ohms; therefore the total series resistance was about 6 ohms. The circuit was implemented on a 7.6-cm by 5.0-cm six-layer circuit board.

Figure 4 shows the measured load current waveform (obtained by measuring the voltage across the 2-ohm resistor with an oscilloscope and dividing the voltage by 2-ohms) when the load capacitance was 10 pF. The quality factor of the circuit was about 5.3 (i.e. under damped). Fig. 5 shows the spectrum of the measurement (obtained using a spectrum analyzer) and envelope estimates obtained using Equations (10) and (11) and the triangular waveform model. The pulse width is approximated as a half of the ringing period in the triangular model calculation, $\Delta t = \pi\sqrt{LC}$. In the RLC model calculation, the risetime of the source signal ($t_r \cong 0.8$ ns) was obtained from an IBIS model [21].

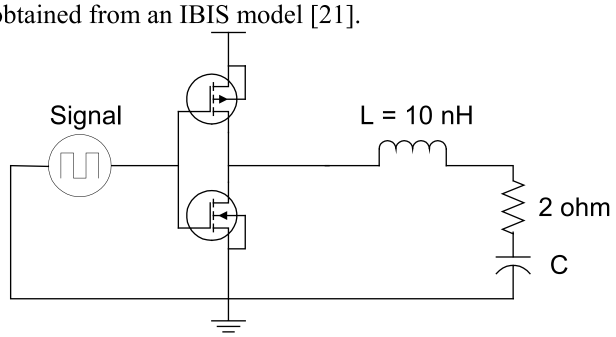

Fig. 3. Equivalent circuit of the measurement setup.

The figure shows that the RLC calculation provides a better estimate of the envelope of the measured current spectrum than the triangular model. This is especially true at the upper harmonic frequencies. Fig. 5 shows that both the measurement and RLC model calculation show a 60-dB/decade slope at high frequencies, while the triangular model predicts a 40-dB/decade slope at high frequencies. The triangular model is not able to account for the combined effect of the finite source risetime and LC filtering.

Fig. 6 shows the measured current waveform when the load capacitance was 100 pF. In this case, the quality factor of the circuit was about 1.7 and the circuit was only slightly underdamped. Fig. 7 compares the measurement to the calculations using the RLC and triangular models. Again, the new model provides a better estimate of the envelope than the triangular model.

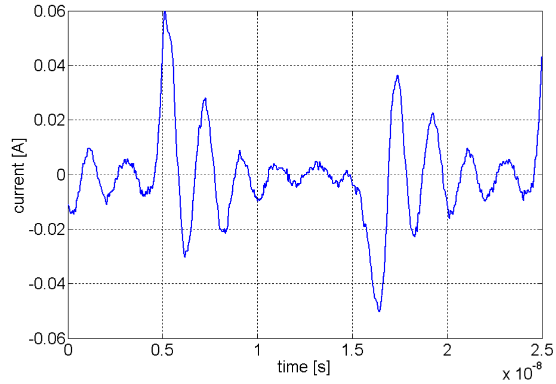

Fig.4. Current waveform when C = 10 pF and R = 5 ohms.

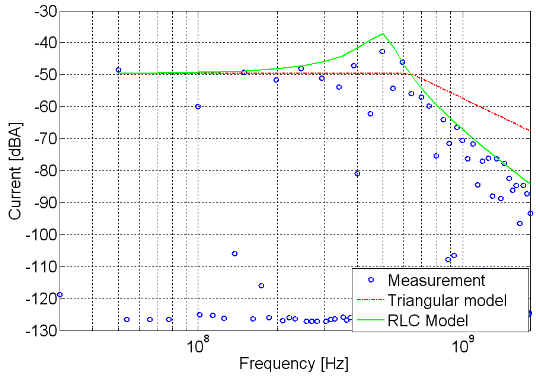

Fig.5. Comparison of measurement, RLC model and triangular model calculation when C = 10 pF and R = 5 ohms.

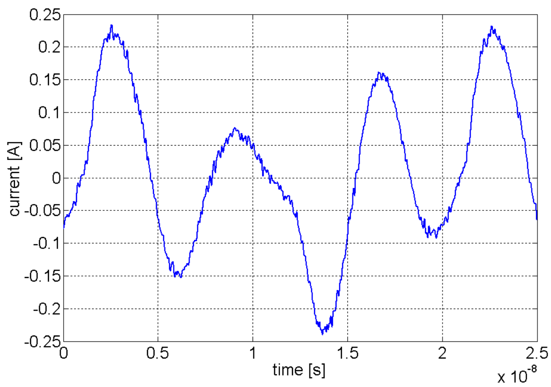

Fig.6. Current waveform when C = 100 pF and R = 5 ohms.

Figure 8 shows the measured current waveform when the load capacitance was 10 pF and the damping resistance was 100 ohms. In this case, the quality factor of the circuit was about 0.32. This is a slightly over-damped case. Figure 9 shows spectrum of the measurement and estimations using the RLC and triangular waveform models. For the triangular model, the risetime of the current was estimated as *2.2RC* (about 2.2 ns). The new model provides a better estimate of the envelope of the measured current spectrum than the triangular model estimation. The triangular estimate cut-off frequency is a little low, causing the upper harmonics to be under-estimated.

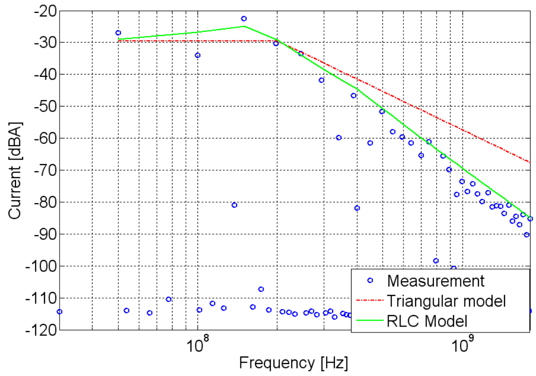

Fig.7. Comparison of measurement, RLC model and triangular model calculation when C = 100 pF and R = 5 ohms.

The current delivered to an actual CMOS device was also measured. The Philips 74LCX16244 line driver IC has 16 outputs, which were connected in parallel and it is driven by the output of another 74LCX16244 line driver IC. The input capacitance of each line driver (~ 7 pF) was obtained from the data sheet. Therefore, the total input capacitance of the buffer IC was about 112 pF. The interconnect inductance associated with the trace between the driver and receiver was estimated to be 6 nH using the technique described in [20]. The total resistance was about 16 ohms. In this case, the quality factor of the circuit was about 0.45. Figure 10 shows the current waveform. Figure 11 shows spectrum of the measurement and estimates of the envelope obtained using the RLC and triangular waveform models. For the triangular model, the risetime of the current was estimated as *2.2RC* (about 4 ns). The RLC model provides a better estimate of the envelope of the measured current spectrum than the triangular model estimation.

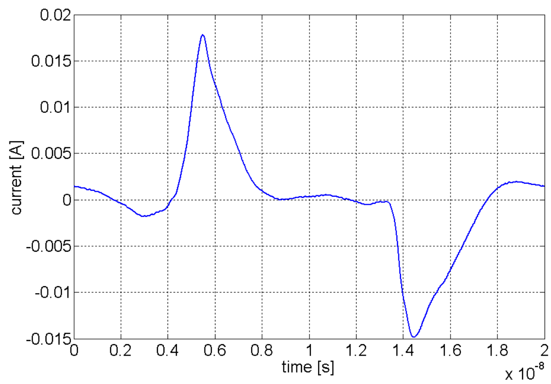

Fig.8. Current waveform when C = 10 pF and R = 100 ohms.

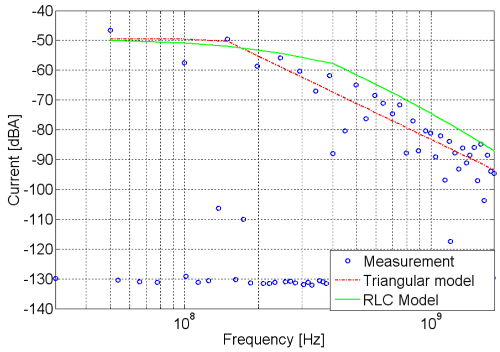

Fig.9. Comparison of measurement, RLC model and triangular model calculation when C = 10 pF and R = 100 ohms.

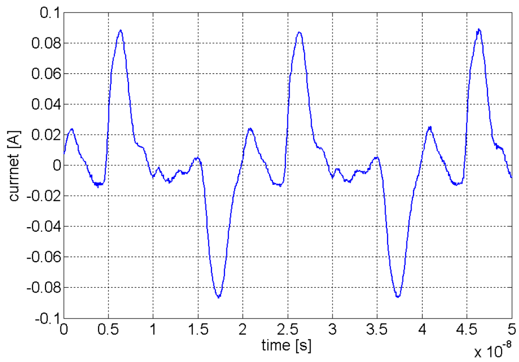

Fig.10. Current waveform for an active device.

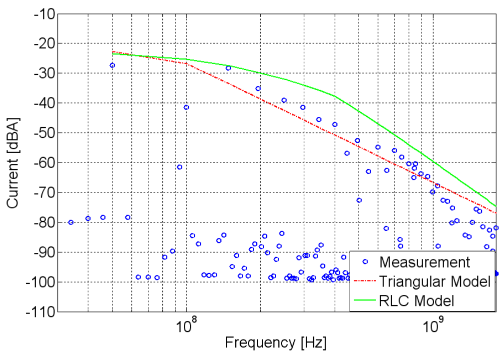

Fig.11. Comparison of measurement, RLC model and triangular model for active device current when C = 112 pF, L = 6 nH and R = 16 ohms.

V. Conclusions

The current spectrum calculated using closed-form formulas based on an RLC model was compared to simulations, measurements and triangular waveform model results. The RLC model provides a better estimate of the current spectrum than the triangular model, especially at upper harmonics. The RLC model predicts the 60dB/decade fall-off of the upper harmonics shown in both simulations and measurements, while the triangular model predicts a 40-dB/decade fall-off. Parameters required for the RLC model calculations are readily obtained from information available in board layout files and component data sheets or IBIS files.

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